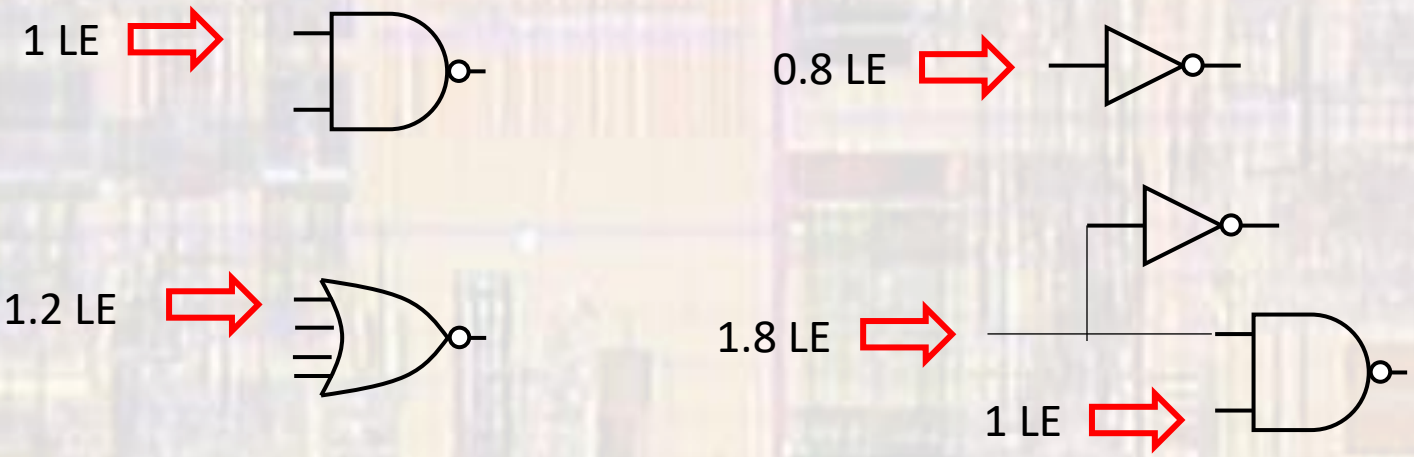
CMOS Timing

Last updated 12/23/23

CMOS Timing

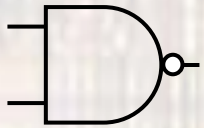
- Gate level timing
  - Each gate **input** has an equivalent input load factor
    - Models the input capacitance
    - Load equivalent (LE)
    - Technology / Process dependent



CMOS Timing

- Gate level timing
  - Each gate has internal delay
    - Assumes no external load (just parasitics)
    - Circuit dependent – but fixed
    - Technology / Process dependent

$t_{pd_{inv}}$

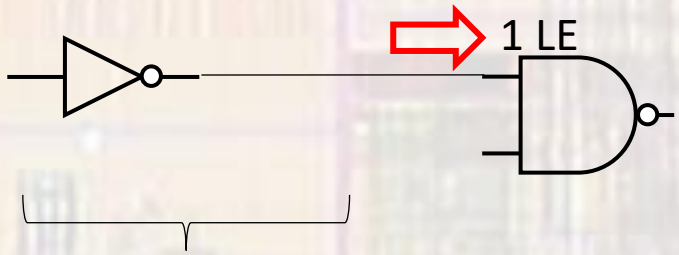


$t_{pd_{nand}}$

CMOS Timing

- Gate level timing
  - Each gate has a variable delay factor - r
    - Function of the gate's drive capability
    - Modifies the circuit delay based on the amount of loading
    - Circuit dependent

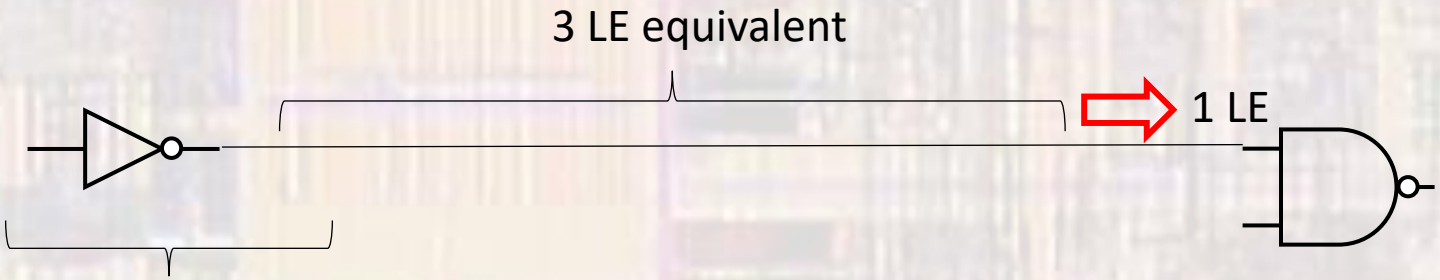
$$t_{pd} = t_{pd_{gate}} + (r \text{ X } \# \text{ of LEs})$$



$$t_{pd} = t_{pd_{inv}} + r \text{ x } 1 \text{ LE}$$

CMOS Timing

- Gate level timing
  - Long wires have enough capacitance to impact delays
    - Model long wires in terms of load equivalents (LEs)
    - Modifies the circuit delay based on the amount of loading
    - Circuit dependent



$$t_{pd} = t_{pd_{inv}} + (r \times (3\ LE + 1\ LE))$$

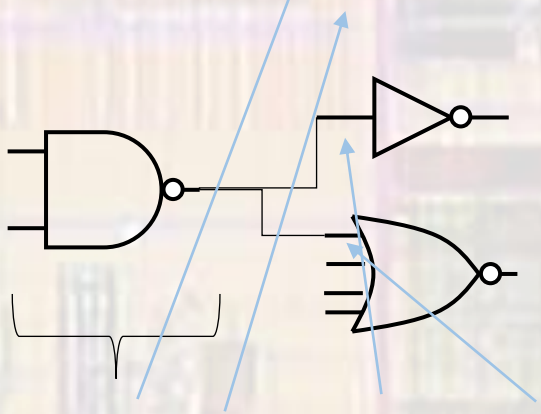
CMOS Timing

- Gate level timing

$t_{pd} = t_{fixed\_delay} + r_{variable\_delay\_factor} * \text{Load Equivalents}$

Standard

Gate	INV	2-NAND	2-NOR	4-NAND	4-NOR
Input load factor (LE)	0.8	1.0	2.0	1.66	3.33
Fixed delay factor	50ps	65ps	65ps	80ps	80ps
Variable delay factor	5ps/LE	8ps/LE	8ps/LE	12ps/LE	12ps/LE



$t_{pd} = 65ps + 8ps/LE*(0.8LE + 3.33LE) = 98ps^{**}$

** we are assuming interconnect capacitance is negligible

CMOS Timing

- Gate level timing

$t_{pd} = t_{fixed\_delay} + r_{variable\_delay\_factor} * \text{Load Equivalents}$

Standard

Gate	INV	2-NAND	2-NOR	4-NAND	4-NOR
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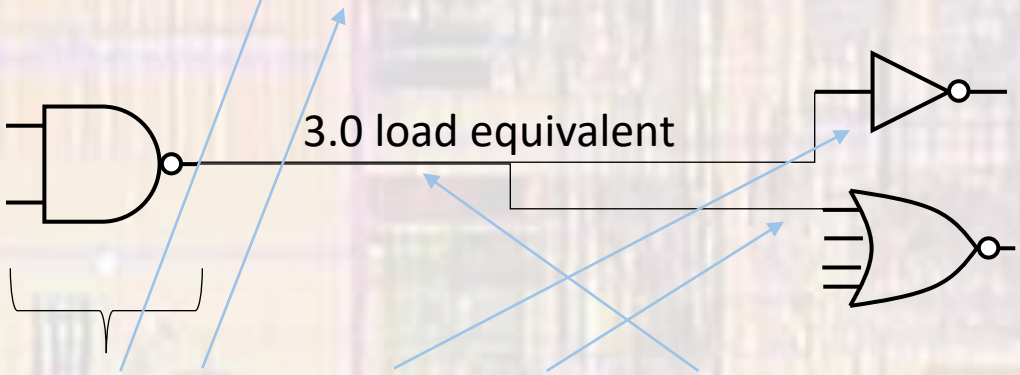
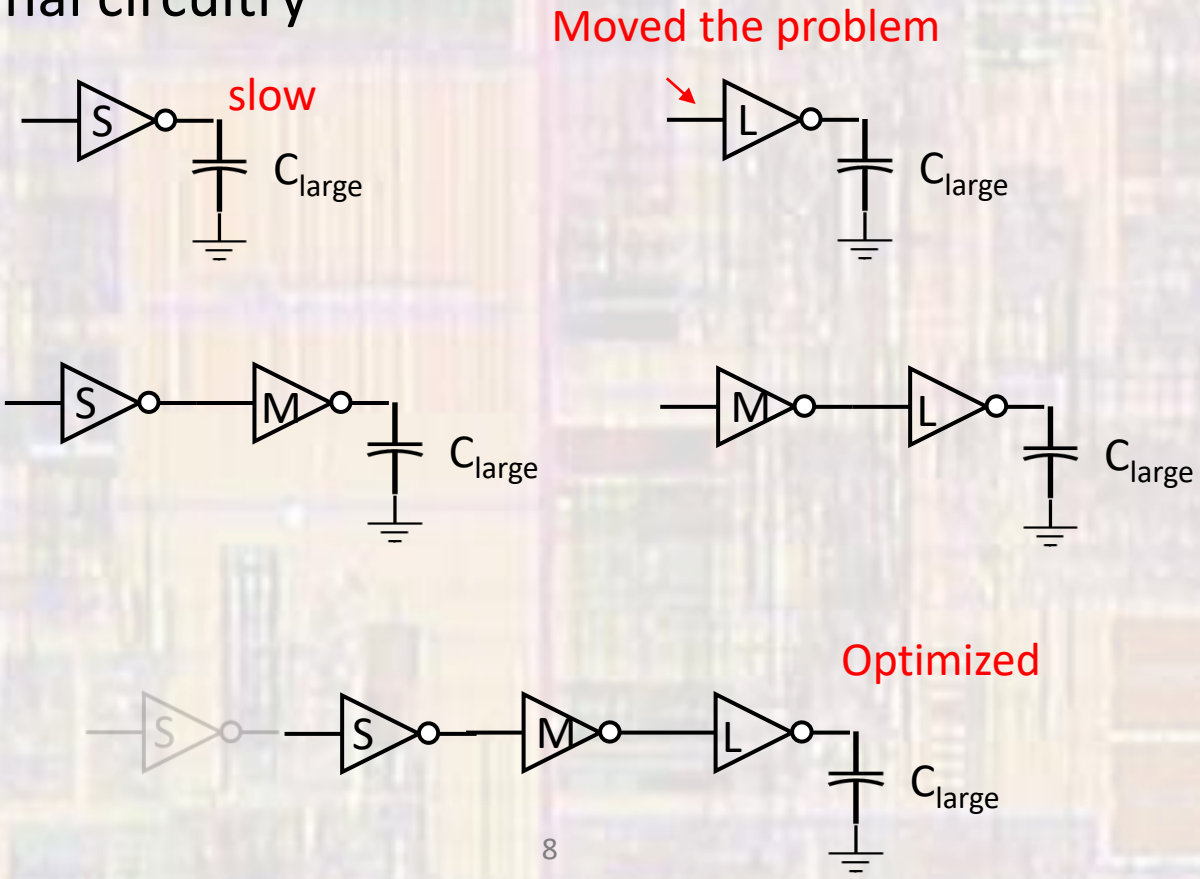


$t_{pd} = 65ps + 8ps/LE*(0.8LE + 3.33LE + 3.0LE) = 122ps$

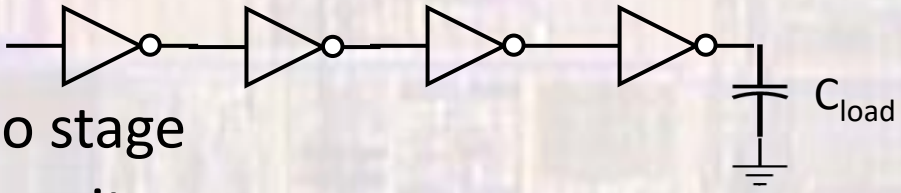
CMOS Timing

- Driving a Large Capacitive Load
  - Clk signals
  - Long wires
  - External circuitry



CMOS Timing

- Driving a Large Capacitive Load
  - N – number of stages
  - s – scale factor from stage to stage
  - C_{inv} – base inverter input capacitance
  - C_{load} – load capacitance
  - γ – Ratio of an inverters output capacitance to input capacitance (Typically ≤ 1)
  - t_{p0} – base inverter delay

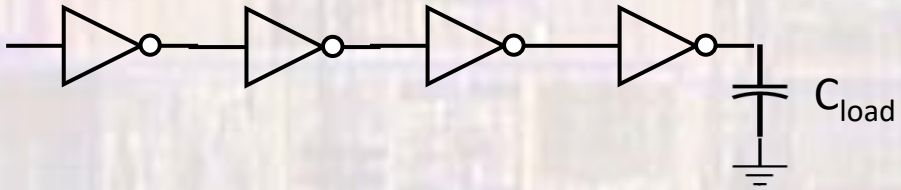


$$s = \sqrt[N]{C_{load}/C_{inv}}$$

$$t_{pd} = N t_{p0}\left(1 + \frac{\sqrt[N]{C_{load}/C_{inv}}}{\gamma}\right)$$

CMOS Timing

- Driving a Large Capacitive Load
  - How many stages?



$$s_{opt} = exp\left(1 + {}^{\gamma}/_{s_{opt}}\right)$$

  - Only has an analytic solution for $\gamma = 0$

$$s_{opt} = e = 2.718 \qquad N_{opt} = ln\left({}^{C_{load}}/_{C_{inv}}\right)$$

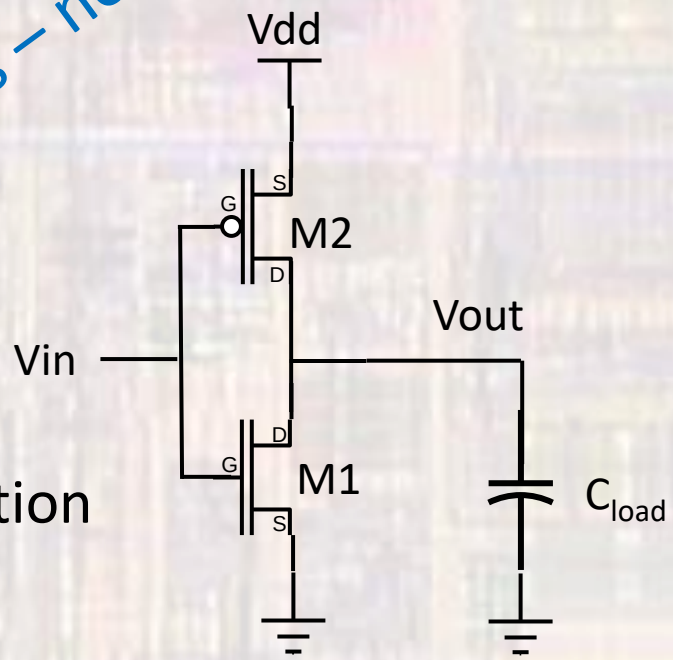
  - For the more realistic value of $\gamma = 1$

$$s_{opt} \approx 3.6 \qquad N_{opt} = log_{3.6}\left({}^{C_{load}}/_{C_{inv}}\right)$$

C-MOS Timing

- Switching speeds
  - Midpoint in, to midpoint out
    - tphl, tplh
  - Assume only one device active
    - Charging/discharging the capacitor
  - Devices start in saturation and transition to non-saturation

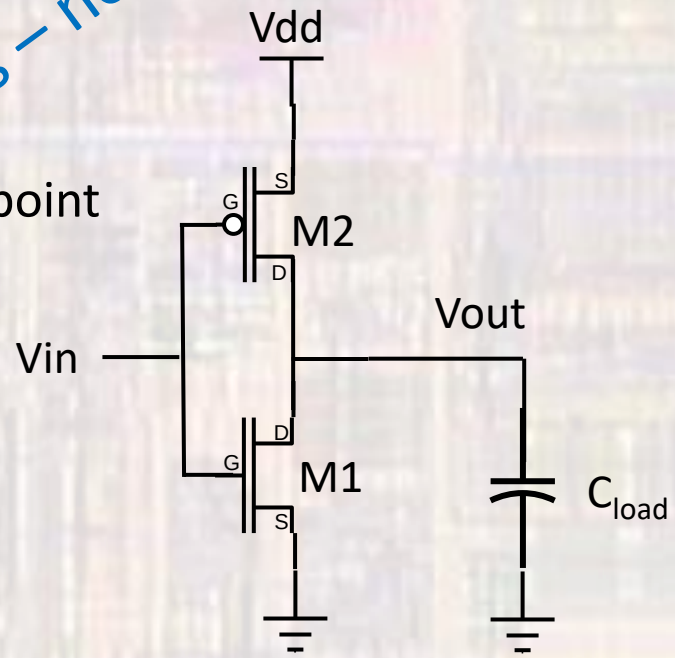
Details – not required



C-MOS Timing

- Switching speeds
  - Super simple estimation
    - Assume in saturation up to the switching point

Details – not required



$$I = C\frac{dv}{dt} = \frac{k'_n}{2}\frac{W}{L}(V_{gs} - V_t)^2$$

$$I = C\frac{dv}{dt} = \frac{k'_n}{2}\frac{W}{L}(V_{dd} - V_t)^2$$

$$dt = C\frac{1}{\frac{k'_n}{2}\frac{W}{L}(V_{dd} - V_t)^2}dv$$

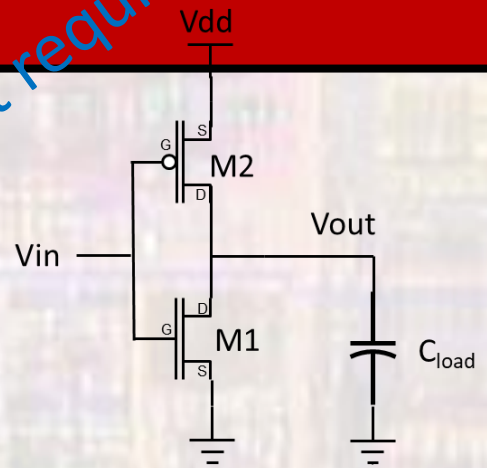
$$t_{hl} = C\frac{1}{\frac{k'_n}{2}\frac{W}{L}(V_{dd} - V_t)^2}\frac{Vdd}{2}$$

$$t_{lh} = C\frac{1}{\frac{k'_p}{2}\frac{W}{L}(V_{dd} - V_t)^2}\frac{Vdd}{2}$$

$$t_{pd} = t_{hl} + t_{lh}$$

C-MOS Timing

Details – not required



- Switching speeds
  - Super simple estimation
    - Assume in saturation up to the switching point

$$t_{hl} = C\frac{1}{\frac{k'_n}{2}\frac{W}{L}(V_{dd}-V_t)^2}\frac{Vdd}{2} \qquad t_{lh} = C\frac{1}{\frac{k'_p}{2}\frac{W}{L}(V_{dd}-V_t)^2}\frac{Vdd}{2}$$

$$t_{pd} = t_{hl} + t_{lh}$$

- Assuming N and P matched for switching point

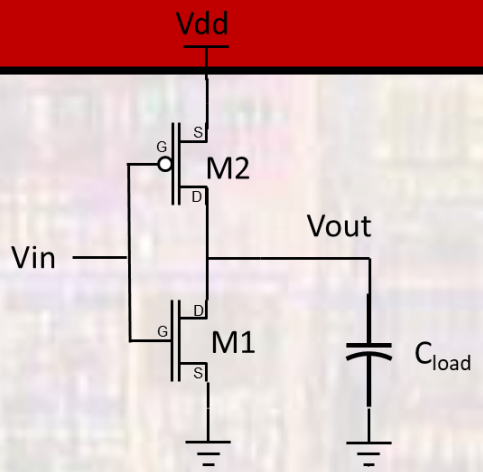
$$t_{pd} = \frac{C\,V_{dd}}{\frac{k'_n}{2}\frac{W}{L}(V_{dd}-V_t)^2}$$

C-MOS Timing

- Switching speeds
  - Super simple estimation
    - Assume in saturation upto the switching point
    - Matched devices

$$t_{pd} = \frac{C_{load}\, V_{dd}}{\frac{k'_n}{2}\frac{W}{L}(V_{dd} - V_t)^2}$$

    - Reduce tpd
      - Increase V_{dd}
      - Increase W/L
      - Decrease C_{load}



Increasing Vdd reduces gate delays
→ higher operating frequency