Domain Crossing

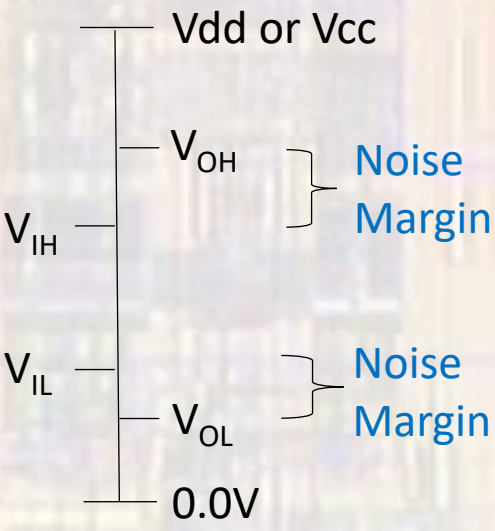
Last updated 1/25/24

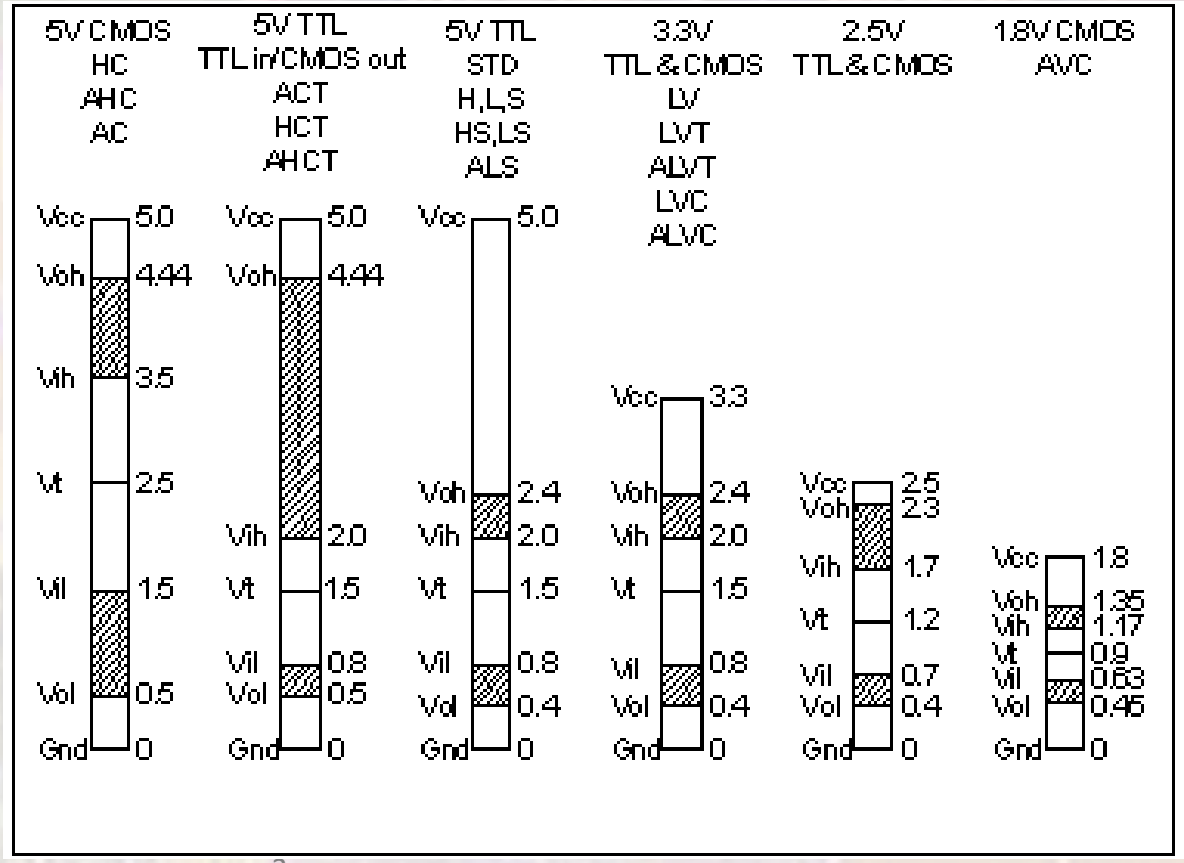
Domain Crossing

- Primary (Modern) Logic Domains
  - Supply voltage (logic levels)
  - Clock Frequency and/or synchronicity
  - Single vs. Differential signaling

Domain Crossing

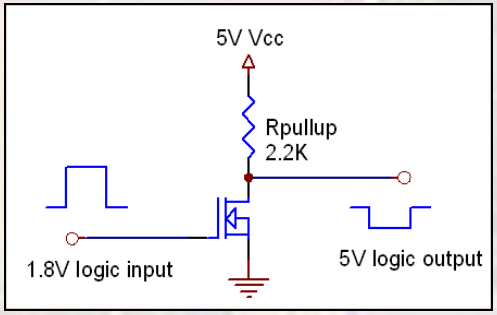
- Logic Level Review
  - V_{OH}, V_{OL} must be 'outside' V_{IH}, V_{IL} for guaranteed signal transfer between gates





Domain Crossing

- Voltage Domain Crossing
  - 3.3V CMOS or LVTTL → 5V TTL
    - No issues
  - 5V TTL → 3.3V CMOS or LVTTL
    - Overdrive inputs
    - Need a buffer
  - 3.3V CMOS <-> 2.5V CMOS <-> 1.8V CMOS
    - Level mismatches
    - Need a buffer
  - Example buffer circuit

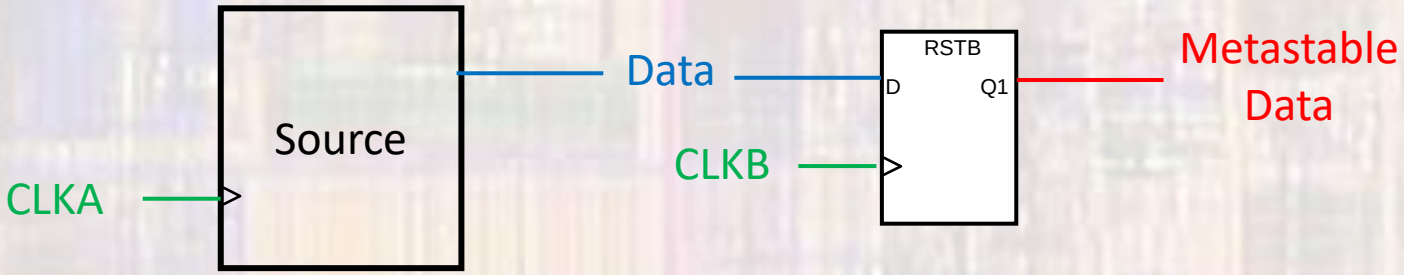


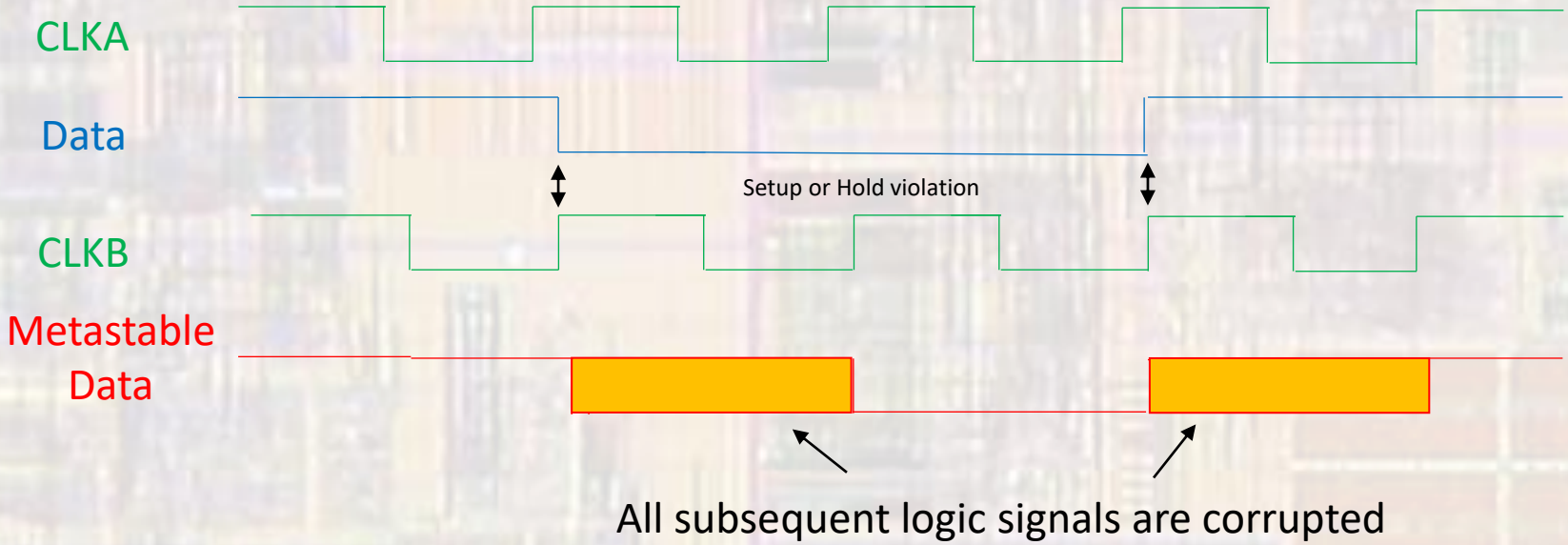
Domain Crossing

- Clock Domain Crossing
  - No design level guarantee that the asynchronous data coming from the source will not violate the sink's setup or hold time
    - Output from the sink's receiver flip-flop is unpredictable
    - Called Metastability
    - Output may switch states multiple times due to failed setup/hold timing

Domain Crossing

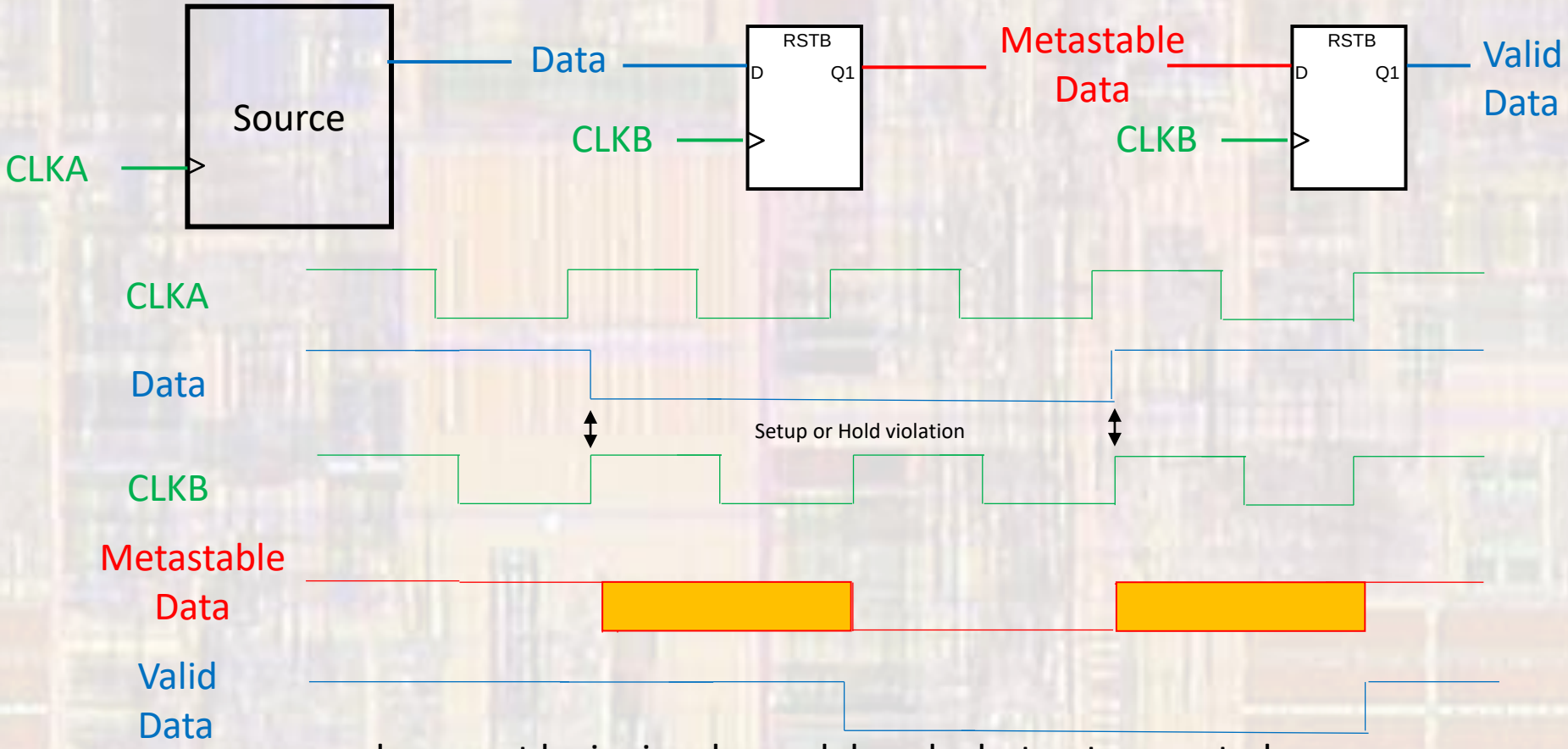
- Clock Domain Crossing
  - Metastability





Domain Crossing

- Clock Domain Crossing
  - Metastability



subsequent logic signals are delayed – but not corrupted