FPGA Basics

Last updated 7/19/23

FPGA Basics

- Field Programmable Gate Array
  - Long history
    - PROM, PAL, CPLD
    - Gate Array, Standard Cells
- Why FPGAs
  - Rapid prototyping
  - In field test / modification
  - Rapidly changing technology / standard
  - Low / mid volume production
    - High volume → ASIC or ASSP

FPGA Basics

- Advantages
  - Flexibility
  - Speed to market
  - Well characterized
- Disadvantages
  - COST
  - Maximum clock frequency
  - Power

FPGA Basics

- Basic Concept
  - Many small fixed circuits

    +
  - Multiple levels of interconnect

    +
  - Programmable connections

- Enhancements
  - Fixed IP blocks
    - Memory
    - Processors
    - Interfaces

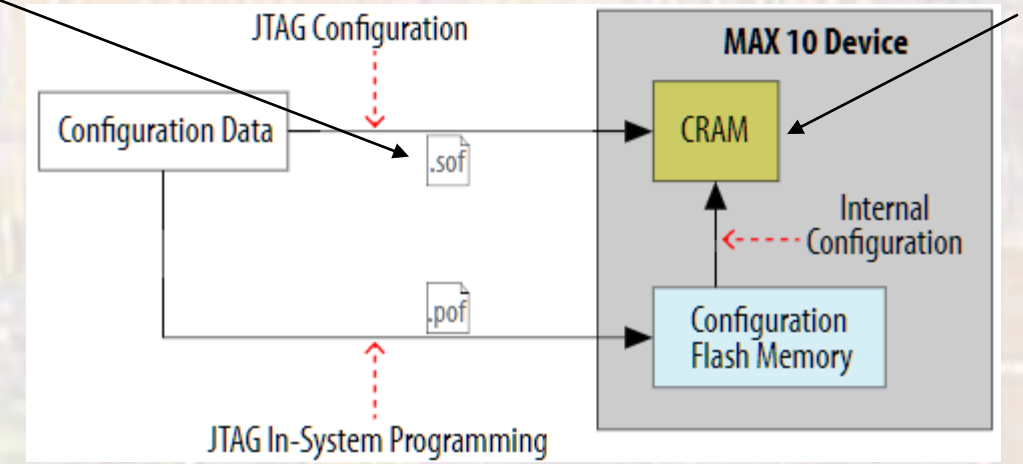
FPGA Basics

- FPGA – programmable
  - 3 primary programming methods
    - RAM
      - Volatile
      - Must be loaded on power-up
      - Most common
    - Electrically erasable (flash)
      - Non-volatile
      - Expensive
    - Fuse / Anti-fuse
      - Non-volatile

FPGA Basics

- FPGA – programmable
  - JTAG Programming Configurations
    - On power-up, the contents of the Configuration Flash Memory (default program) are loaded into the Configuration RAM
      - Flashing lights and numbers we see on power up
    - Load programming information (xx.sof file) directly into the Configuration RAM via the JTAG interface (Programmer)
      - Our configuration is loaded

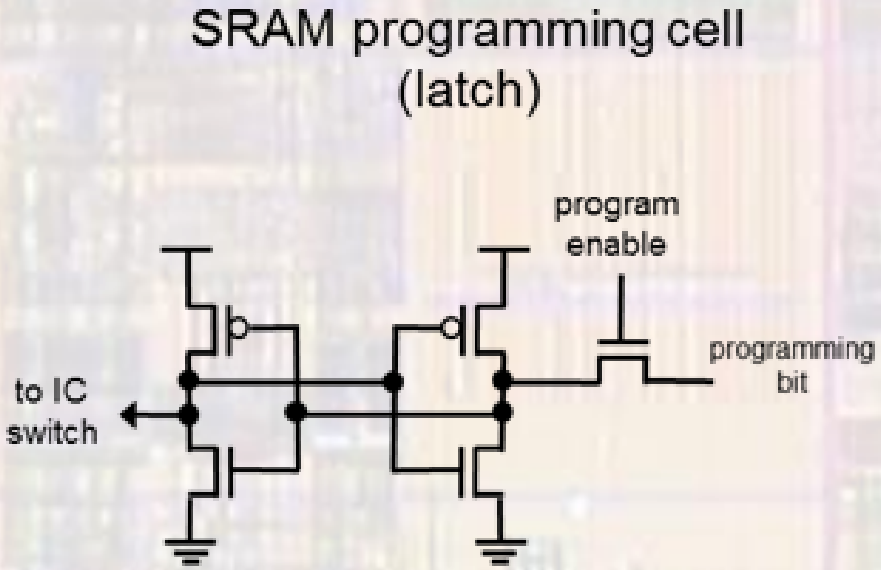
xx.sof file
SRAM Object File



Configuration RAM

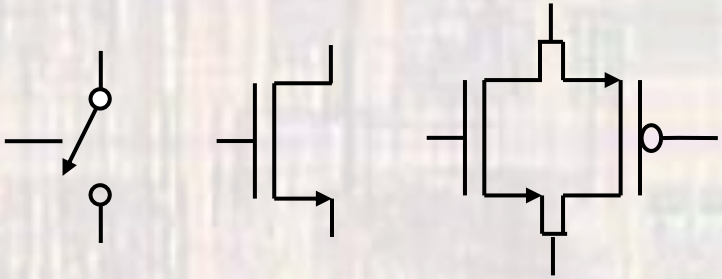
FPGA Basics

- FPGA – programmable
  - SRAM based



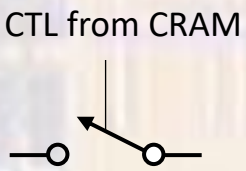
Src: Altera - PLDBasics_FPGA_Architecture

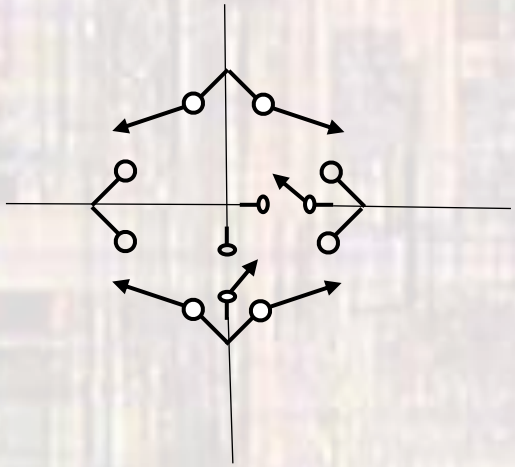
Switches



FPGA Basics

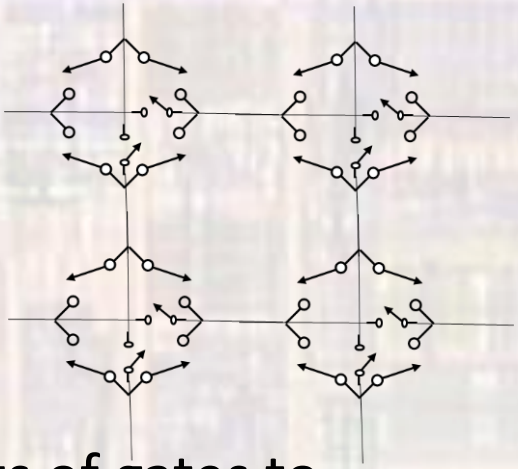
- FPGA – programmable
  - Switches are programmed (On or Off) by connecting their control inputs to C-RAM bit cells
  - Switch configurations



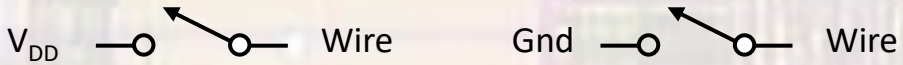


FPGA Basics

- FP**GA** – programmable
  - Switches connect a series of horizontal and vertical wires
    - Connect wires to logic block inputs/outputs
    - Allow connections to span across the chip



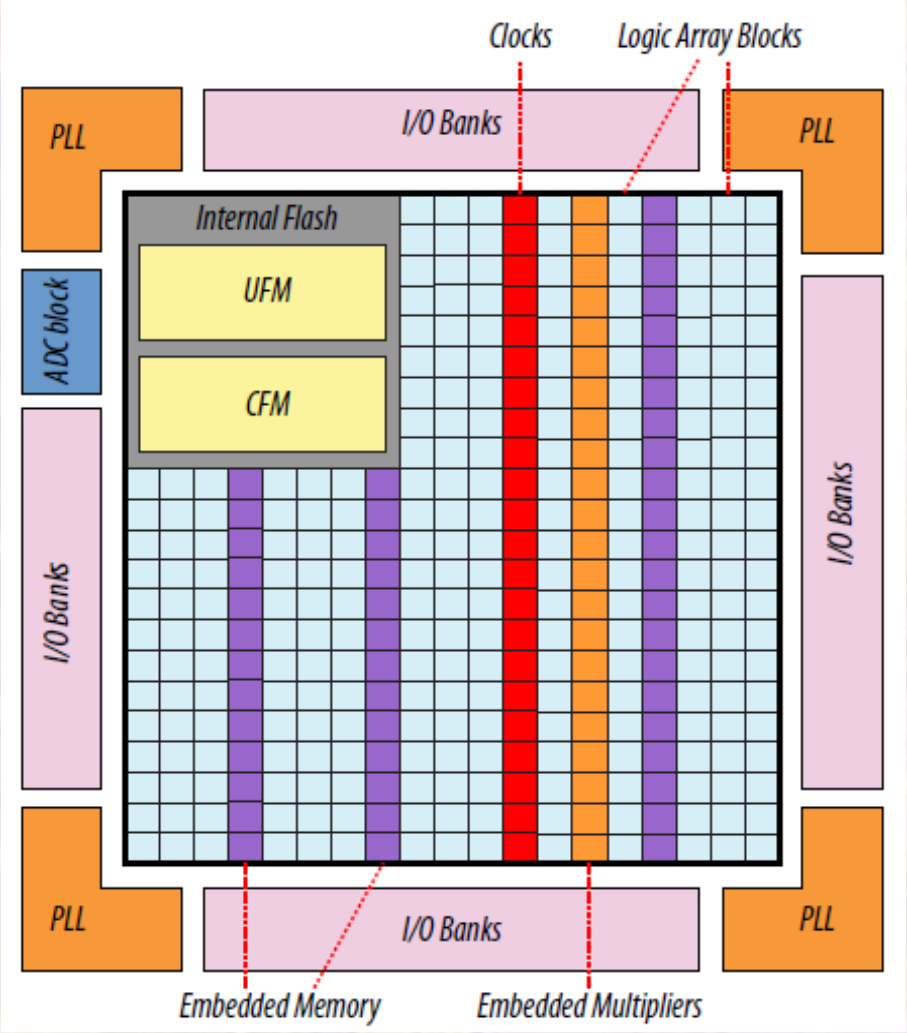
  - Switches connect V_{DD} and Gnd to the inputs of gates to force 1/0 inputs



  - Switches connect external pins to block inputs/outputs

FPGA Basics

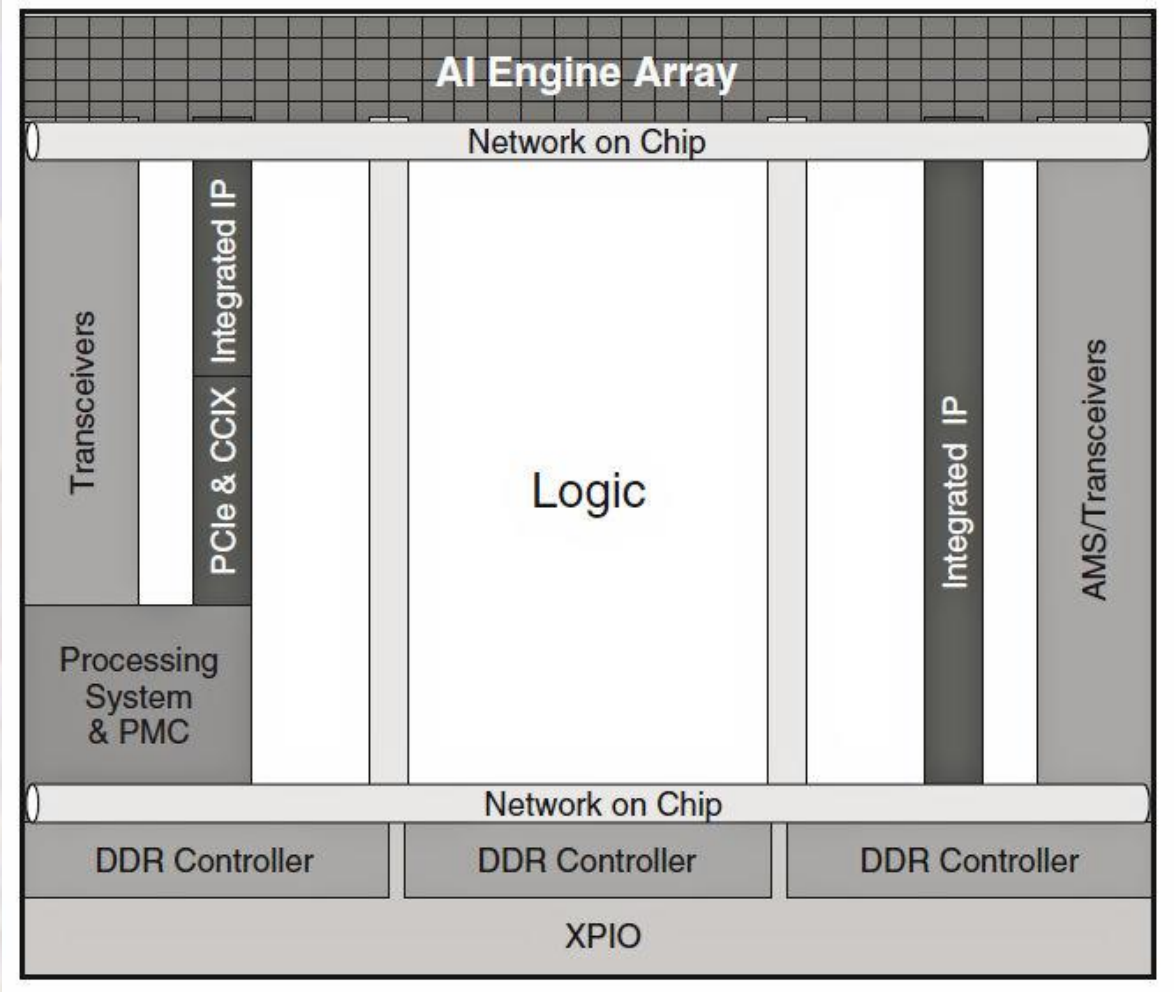
- Intel/Altera Max 10



Src: MAX 10 Device Handbook

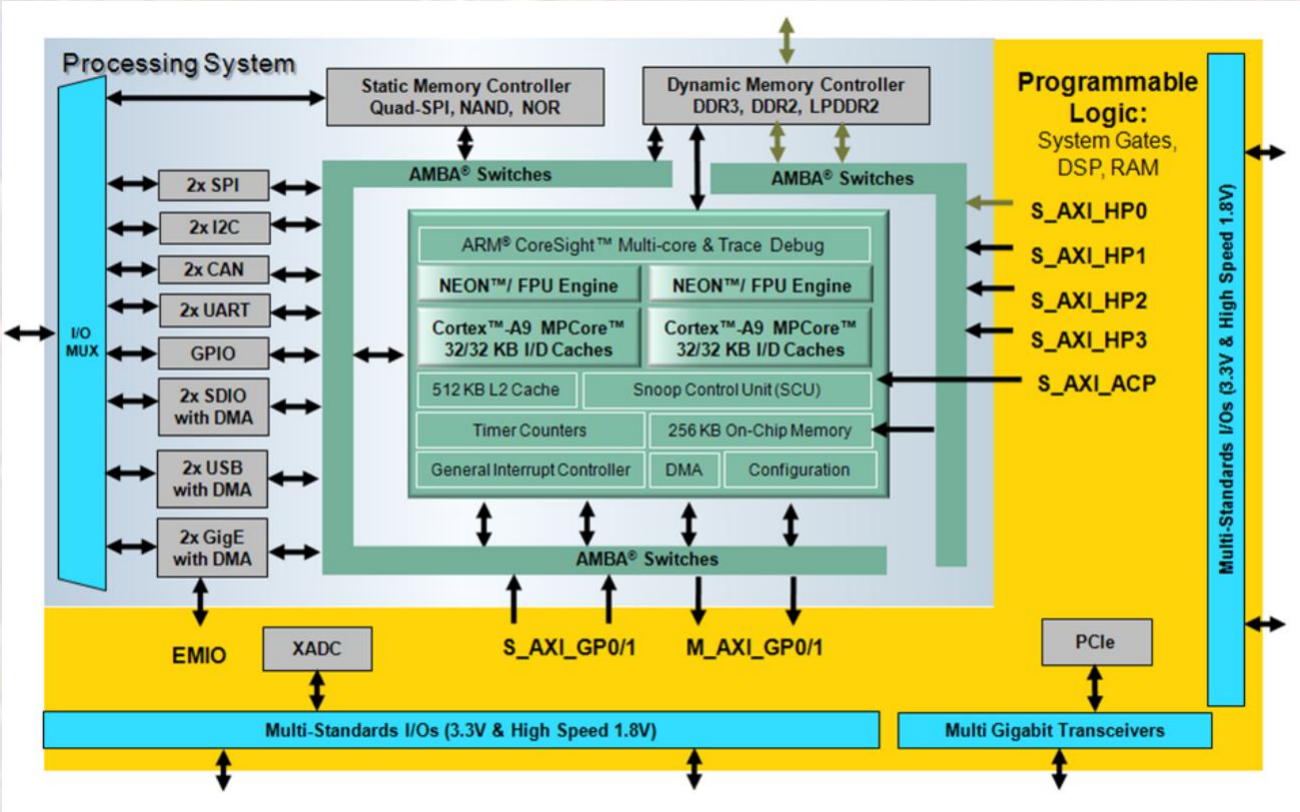
FPGA Basics

- Xilinx Versal



FPGA Basics

- Xilinx Zynq



FPGA Basics

- Intel/Altera Stratix 10