

1A – How many onboard memory blocks would be required to support a 1K word, 16b/word SRAM memory? 10 pts

$$1KW \times 16b/W = 16Kb \rightarrow 2 \text{ M9K blocks}$$

1B – What is the largest size 32bit word memory that can fit in a single on chip memory block? 10 pts

M9K has extra 1K bits attached to the word width, not the # of words \rightarrow 8Kb \rightarrow 1KB \rightarrow 256W in x32 configuration

Feature	M9K Block
Configurations (depth \times width)	8192 \times 1
	4096 \times 2
	2048 \times 4
	1024 \times 8
	1024 \times 9
	512 \times 16
	512 \times 18
	256 \times 32
	256 \times 36

Parity used as memory

2 - Implement a dual clock 8KB single port SRAM in by-32 configuration using the

MCPL

```

-- sram_8KB_in_by32_mega.vhd1
-- created 4/25/17
-- tj
-- rev 0
-----
-- 8KB in x32 dq RAM from mega library
-----
-- Inputs: clk, addr, data_in, we_b
-- Outputs: data_out
-----
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity sram_8KB_in_by32_mega is
    port(
        i_clk_in:    in std_logic;
        i_clk_out:   in std_logic;
        i_we_b:      in std_logic;
        i_addr:      in std_logic_vector(10 downto 0);
        i_data_in:   in std_logic_vector(31 downto 0);
        o_data_out:  out std_logic_vector(31 downto 0)
    );
end;
    
```

```

architecture behavioral of sram_8KB_in_by32_mega is
-- invert we
--
    signal we_sig: std_logic;

    component SRAM_8KB_in_by32
    PORT(
        address      : IN STD_LOGIC_VECTOR (10 DOWNTO 0);
        data         : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
        inclock      : IN STD_LOGIC := '1';
        outclock     : IN STD_LOGIC ;
        wren         : IN STD_LOGIC ;
        q            : OUT STD_LOGIC_VECTOR (31 DOWNTO 0)
    );
    end component;

    begin
        we_sig <= not i_we_b;

        SRAM_8KB_in_by32_inst : SRAM_8KB_in_by32
            PORT MAP (
                address => i_addr,
                data    => i_data_in,
                inclock => i_clk_in,
                outclock => i_clk_out,
                wren    => we_sig,
                q       => o_data_out
            );
    end behavioral;
    
```

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Flow Summary	
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Flow Status	Successful - Fri Jun 26 11:5
Quartus Prime Version	18.1.0 Build 625 09/12/20
Revision Name	hw6
Top-level Entity Name	sram_8KB_in_by32_mega
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	1 / 49,760 (< 1 %)
Total registers	0
Total pins	78 / 360 (22 %)
Total virtual pins	0
Total memory bits	65,536 / 1,677,312 (4 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)