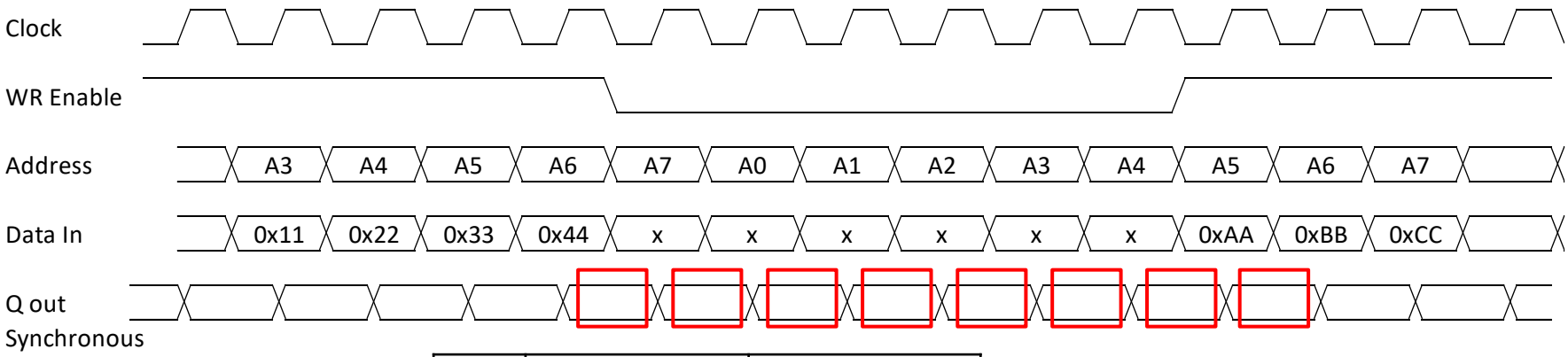
ELE 3510 HW12 Name_____

1 - Simple single port memory: Given the timing diagram below for the simple single port memory, fill in the values for the empty boxes on the diagram and the final memory values. Assume a new data output model 40 pts



	Mem Hex BEFORE	Mem Hex AFTER
A0	0x1A	
A1	0x1B	
A2	0x1C	
A3	0x1D	
A4	0x1E	
A5	0x1F	
A6	0x20	
A7	0x21	

ELE 3510 HW12 Name_____

2 - Review the Max10 spec and provide the ranges for n and m in the PLLs. Calculate the greatest multiply possible, the greatest divide possible, and the closest frequency to the original clock that can be created (that is not the same as the original clock) Note – assume the C dividers =1 10 pts

N:	
M:	

Biggest multiple	
Biggest Divide	
Closest value	

ELE 3510 HW12 Name_____

3 - Create a 7bit x 9bit multiplier using the Mega Wizard

a) Provide your module code 10 pts

b) Provide an RTL schematic 10 pts

c) Create a testbench that runs all input combinations (do not create an exhaustive list – use a loop or similar construct 20 pts

d) Provide simulation results for 4x286 and 127x511 10 pts