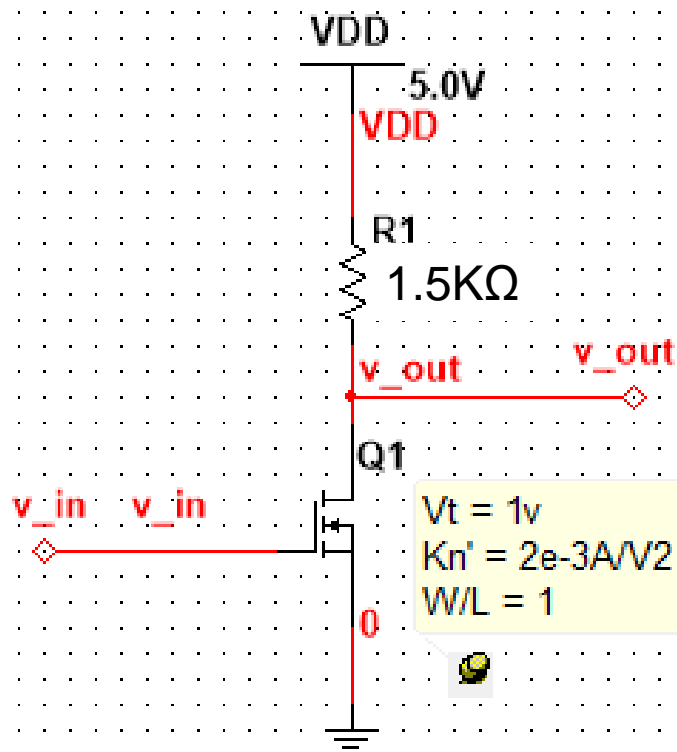


- 1 – Analysis: Create a table of the **calculated** expected output voltages for v_{in} from 0V to 5V in 0.5V increments. 40pts
- Note: be sure to confirm the NMOS operating region



- 3 – Use DeMorgan's theorem to reduce the logic equation in problem 2. Implement the solution with NANDs, NORs, and Inverters. Compare the 6-transistor solution in problem 2 to your solution above with respect to area and speed 30pts