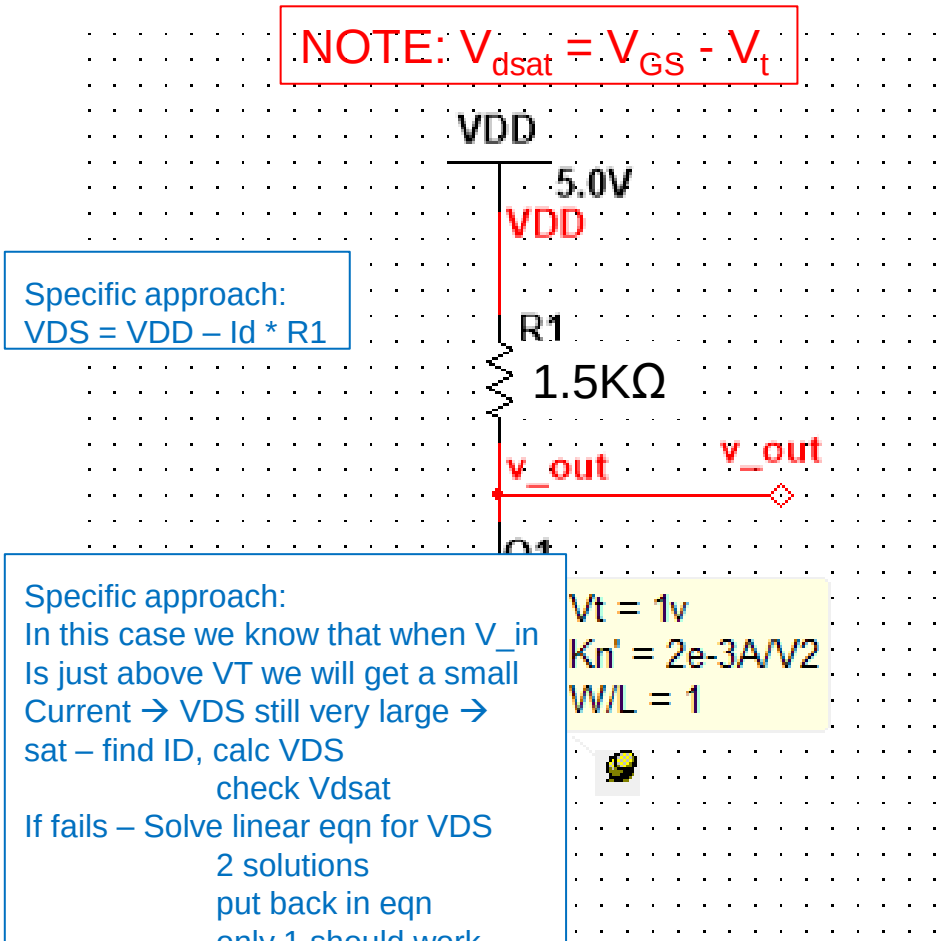
ELE 3510 HW2 Name_____

1 – Analysis: Create a table of the calculated expe v_in
from 0V to 5V in 0.5V increments. pts
Note: be sure to confirm the NMOS operating

General approach:
Check for cutoff
Assume sat – find ID, calc VDS
check Vdsat
If fails – Solve linear eqn for VDS
2 solutions
put back in eqn
only 1 should work

NOTE: $V_{dsat} = V_{GS} - V_t$



Specific approach:
VDS = VDD – Id * R1

Specific approach:
In this case we know that when V_in
Is just above VT we will get a small
Current → VDS still very large →
sat – find ID, calc VDS
check Vdsat
If fails – Solve linear eqn for VDS
2 solutions
put back in eqn
only 1 should work

Vin	ID	VDS	Mode
0	0.00E+00	5.000	cutoff
0.5	0.00E+00	5.000	cutoff
1	0.00E+00	5.000	cutoff
1.5	2.50E-04	4.625	sat
2	1.00E-03	3.500	sat
2.5	2.25E-03	1.625	sat
3	2.75E-03	0.880	lin
3.5	2.89E-03	0.667	lin
4	2.97E-03	0.544	lin
4.5	3.02E-03	0.463	lin
5	3.06E-03	0.403	lin

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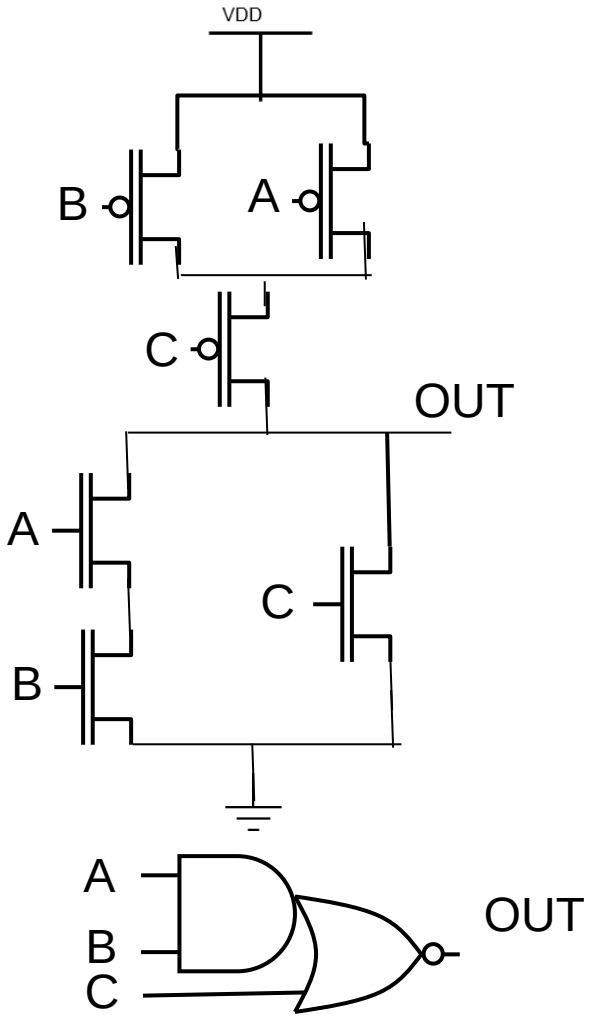
2 – Create a truth table and a SOP or POS logic equation for the circuit below .
This is called a compound gate. 30pts



A	B	C	OUT
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

a’b’c’ + a’bc’ + ab’c’

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3 – Use DeMorgan's theorem to reduce the logic equation in problem 2. Implement the solution with NANDs, NORs, and Inverters. Compare the 6-transistor solution in problem 2 to your solution above with respect to area and speed 30pts

a'b'c' + a'bc' + ab'c'

a'c'(b + b') + ab'c'

a'c' + ab'c'

c'(a'+ ab')

$\overline{c + \overline{(a' + ab')}}$

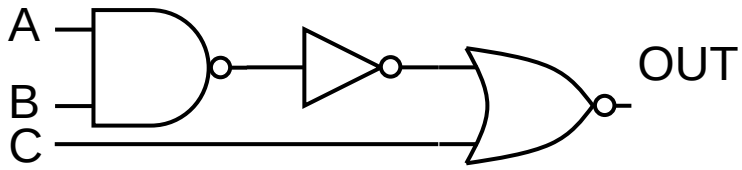
$\overline{c + a\overline{(ab')}}$

$\overline{c + a(a' + b)}$

$\overline{c + aa' + ab}$

$\overline{c + ab}$

$\overline{c + \overline{ab}}$



Compound gate is:

Faster (1 delay vs. 3 delays)
Smaller (6T vs. 10T)

Most logic libraries include a large number of compound gates