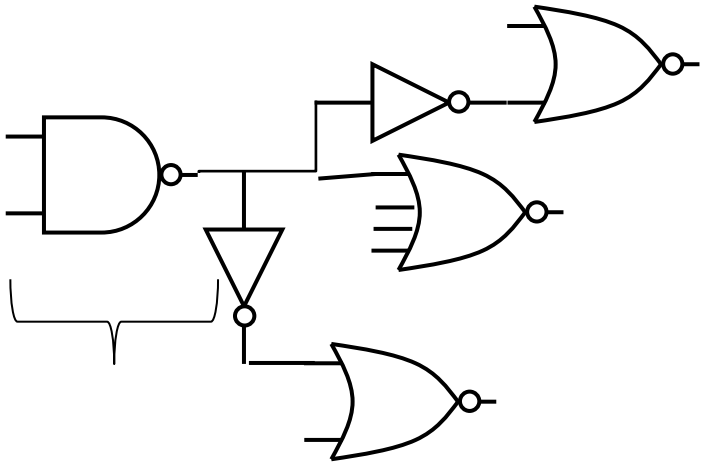
ELE 3510 HW3 Name_____

1 – Given the gate information below, calculate the t_{pd} for the 2 input nand gate

** we are assuming interconnect capacitance is negligible

30pts

Gate	INV	2-NAND	2-NOR	4-NAND	4-NOR
Input load factor	0.8	1.0	1.0	1.75	1.75
Fixed delay factor	50ps	65ps	65ps	80ps	80ps
Variable delay factor	5ps	8ps	8ps	12ps	12ps



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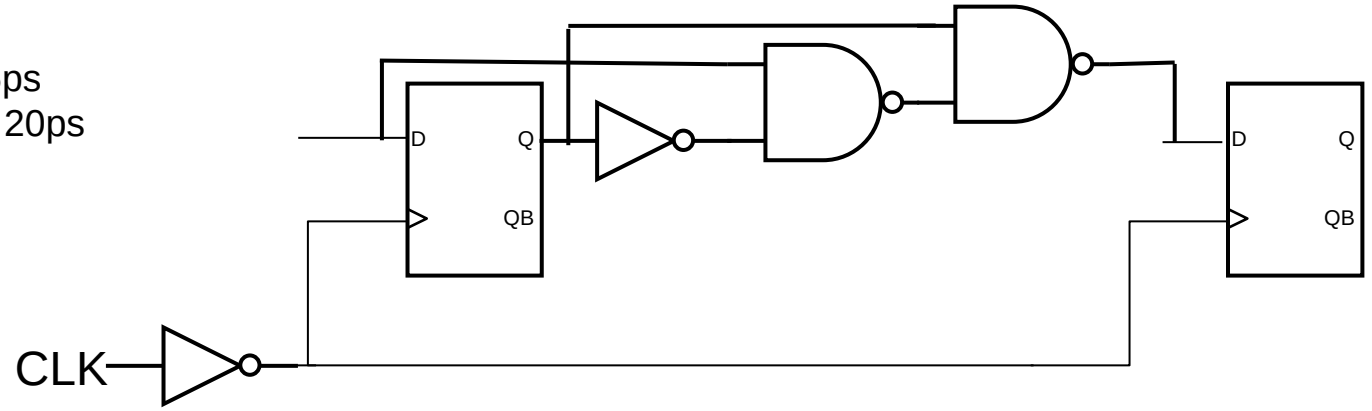
2 – Calculate the fastest possible clock frequency 30pts

t_{PD} INV = 15ps
t_{PD} NAND = 20ps
t_{CQ} = 25ps
t_{setup} = 5ps
t_{hold} = 2ps



ELE 3510 HW3 Name_____

3 – You are designing a new system that can operate at 1.2V, 2.4V or 3.3V with one-time programmable clock frequencies of 50% max, 75% max and 100% max. The system has 2 operating modes. Mode 1 requires 10M clk cycles and must execute every 100ms. Mode 2 requires 25M clk cycles and must execute every second. The system has the following characteristics.

VDD	**Max Clk freq**	**I_{Static}**	**$I_{Dynamic}$**
1.2V	120MHz	10uA	1pA/clk
2.4V	180MHz	20uA	3pA/clk
3.3V	240MHz	40uA	6pA/clk

Determine the optimal operating conditions with respect to total power 40pts