ELE 3510 HW4 Name_____

1 – Create VHDL code and RTL for a D-FF with asynchronous resetb and synchronous set. Follow all best practices. 20pts

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2 – Create VHDL code and RTL for a JK-FF with synchronous resetb and asynchronous set. Follow all best practices. 30pts

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3 – Create VHDL code and RTL for a special new FlipFlop you have conceived of – this is a normal D-FF (with async rstb) but has a second data input called Toggle(T). When T is low, the DFF operates normally, when T is high, the DFF ignores the D input and synchronously toggles the output. Follow all best practices. 50pts