ELE 3510 HW5 Name_____

1 – Create the 2 test processes described below and provide a simulation. Assume an existing clk process running with period PER and a resetb process that releases reset on the 2nd falling clock edge 50pts

You can use any existing design as the top level block for compiling the code

Periodic input “foo” with period 4 times the clock period and a 25% duty cycle that runs for 7 “foo” periods then stops. Synchronized to the falling clock edge.

8 bit signal “boo” that increments every 6th cycle and repeats infinitely

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2 – Create the testbench and simulation for the JK Flip-Flop from problem 2 of HW 4. Be sure you can clearly see and identify each mode of operation 50pts