

- 1) Determine the total number of bits in each memory – assume digital values for K, M, G 25pts
 - a) 256Mb SRAM in a x4 configuration

 - a) 64GB x 16 NAND Flash

- 2) Determine the total number of address lines required for each memory – assume no address line sharing and digital values for K, M, G 25pts
 - a) 128KB ROM in a x8 configuration

 - a) 32Gb NOR Flash in a x16 configuration

- 3) Assuming a square memory cell, shared address lines for the row and column decoders and a square overall memory footprint, determine the best address bus width – assume digital values for K, M, G 25pts

256Mb SRAM in a x4 configuration

- 4) Create a state transition diagram for 5 speed automatic transmission with P and R 25pts

inputs: engine RPM, Shifter (P, D, R)

outputs: gear (1-5, Pk, Rvs)

Notes: upshifts at 3500rpm, downshifts at 1100 rpm