ELE 3510 HW7 Name_____

1) Determine the total number of bits in each memory – assume digital values for K, M, G 25pts

   a) 256Mb SRAM in a x4 configuration

   256Mb → 2^8 2^{20} bits → 256Mb →268,435,465 bits

   b) 64GB x 16 NAND Flash

64GBx16 → 2^6 2^{30} 2^3 2^4 bits → 2^{43} bits → 8Tb → 8,796,093,022,208 bits

2) Determine the total number of address lines required for each memory – assume no address line sharing and digital values for K, M, G 25pts

   a) 128KB ROM in a x8 configuration

Bytes in a x8 → 1 address / byte
128KB in a x8 → 128K addresses → $2^7 2^{10}$ addresses → 17 address lines

   b) 32Gb NOR Flash in a x16 configuration

32Gb in a x16 → 2G addresses → $2^1 2^{30}$ addresses → 31 address lines

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3) Assuming a square memory cell, shared address lines for the row and column decoders and a square overall memory footprint, determine the best address bus width – assume digital values for K, M, G 25pts

256Mb SRAM in a x4 configuration

256Mb in x4 → 64M addresses → $2^6\ 2^{20}$ addresses → 26 address lines

in x4 , 4 rows for every column → 4x as many row addresses as col addresses to make the overall footprint square
→ 2 more row address bit than column address bits

→ 2 more row address lines than column address lines
26 = rows + cols = (cols + 2) + cols
→ 12 column address lines and 14 row address lines

→ address bus of 14 lines (16 if you include CAS and RAS)

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4) Create a state transition diagram for 5 speed automatic transmission with P and R 25pts

inputs: engine RPM, Shifter (P, D, R)

outputs: gear (1-5, Pk, Rvs)

Notes: upshifts at 3500rpm, downshifts at 1100 rpm