ELE 3510 Lab 1: RC Circuits

2 dedicated lab periods, 2 lab periods to complete

Objectives

- Review MultiSim schematic entry and simulation
- Review timing calculations
- Review power calculations

Prelab	**student check off**
• Setup MultiSim using the MultiSim Setup slides	☐

In lab Activities – MSOE Library Setup (do not do this on your own)	**check off**
• Setup the MSOE MultiSim Template	☐
• Setup the MSOE 45nm MOSFET Library	☐

Assignment

Part 1: RC time constants and simulation measurements

1) Using the circuits from the Part 1 Schematic – calculate the expected delay times t_{pdr}, t_{pdf}, and the expected rise and fall times t_r, t_f (This requires you to use equations)
   These measurements are defined in the Common Waveform Measurements slides
2) Create the Part 1 Schematic in MultiSim
   (be sure to put it in your personal MultiSim project directory)
3) Using the circuits from the Part 1 Schematic – simulate and measure the delay times t_{pdr}, t_{pdf}, and the rise and fall times t_r, t_f
4) Compare your calculations to the simulated results
5) Discuss the impact of output impedance (the R) and the load capacitance (the C) on these results

Part 2: CMOS Inverter Current

1) Create the Part 2 Schematic in MultiSim
   Carefully note the direction of the MOSFETs
2) Perform the simulations a-g as outlined in the Part 2 appendix
3) Provide explanations for each plot and answer the questions in red.

Check Off

You must demonstrate 1 working simulation from each part prior to the beginning of the lab following the second lab (all simulations should be in your report)

- Part 1 – RC time constant (Simulation) 40%
- Part 2 – Inverter Currents (Simulation) 40%

Lab Report (informal)

- Due at 4:00 pm, the day of the lab following the second lab – in the box
- Include a properly documented informal lab report. 20%

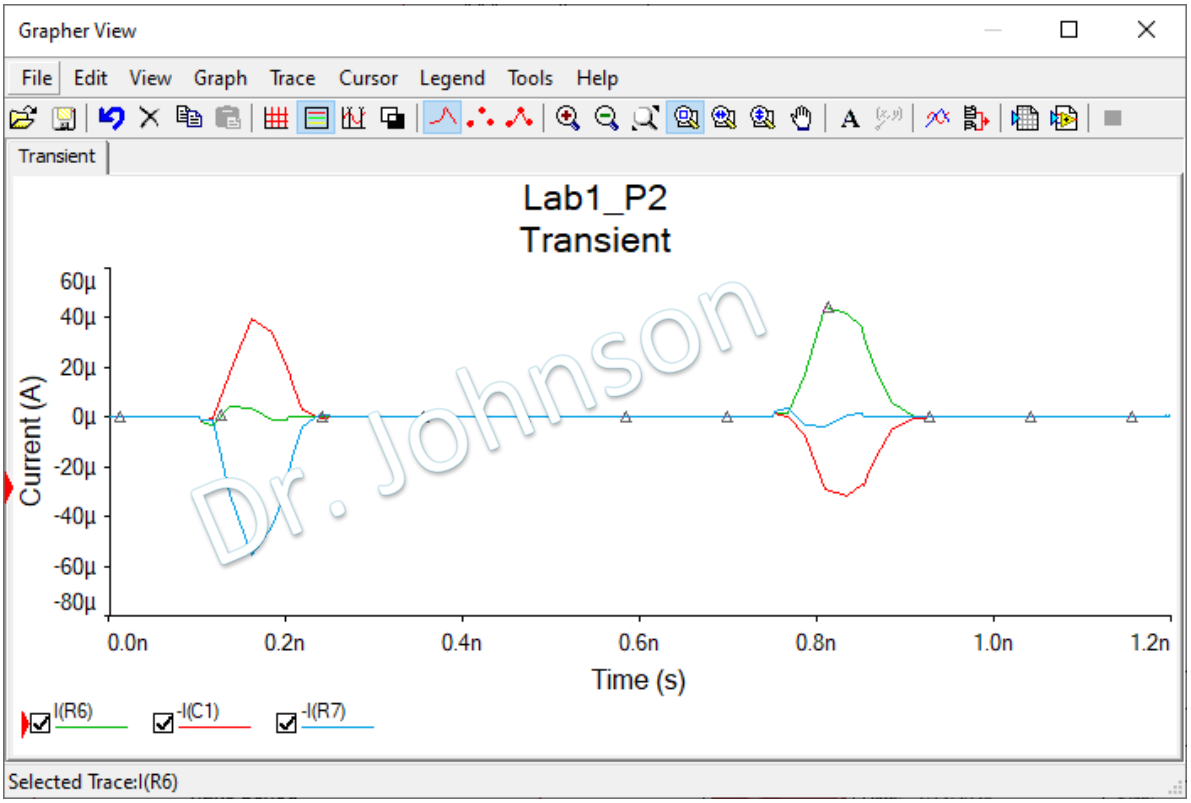
Part 2 Appendix

a) Run a transient simulation and plot vin and vout to verify connections.

b) Temporarily disconnect the load capacitor and rerun the simulation from part a

Why are the transition delays reduced?

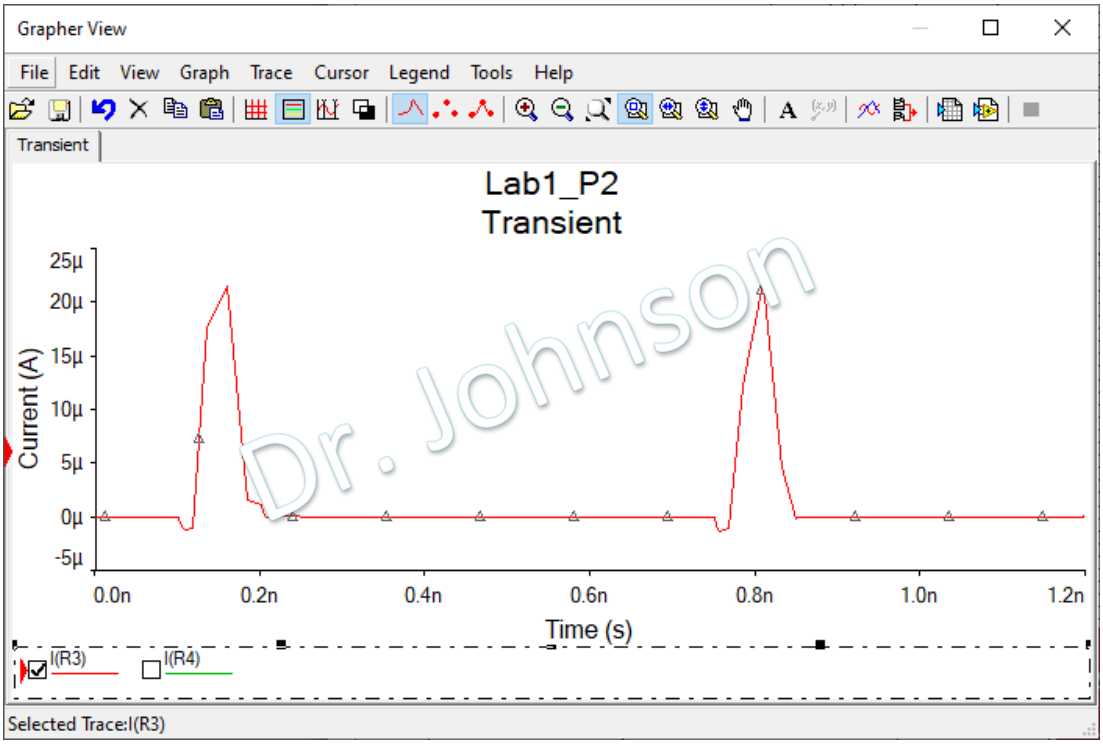
c) Reconnect the load capacitor. Run a transient simulation and plot -I(C), I(R6), -I(R7)
Note: The currents do not sum to 0, where is the missing current going?



d) Disconnect the load capacitor and rerun the simulation from part c
Note: The currents do not sum to 0, where is the missing current going?

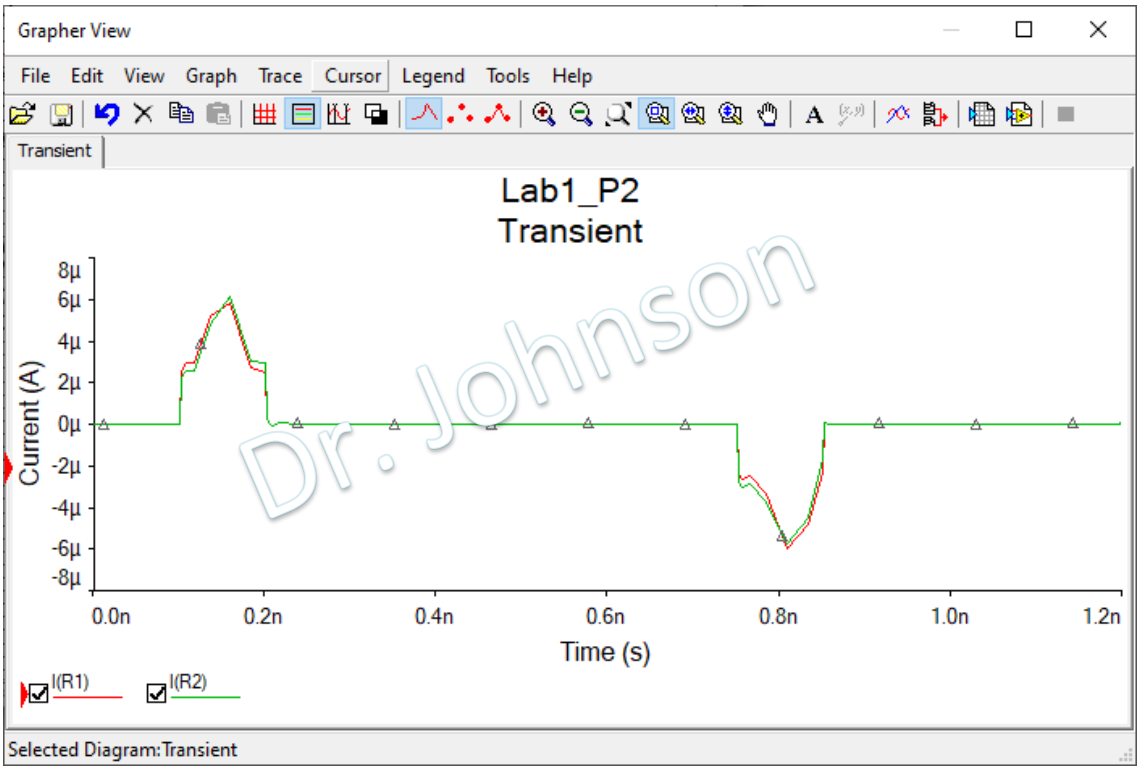
e) With the load capacitor disconnected plot I(R3) or I(R4).
Zoom in on the small spike near 0.15ns.
This is the shoot-through current in the inverter.

f) With the load capacitor disconnected plot I(R3) or I(R4).
Zoom in on the small spike at 0.8ns.
This is the shoot-through current in the inverter.



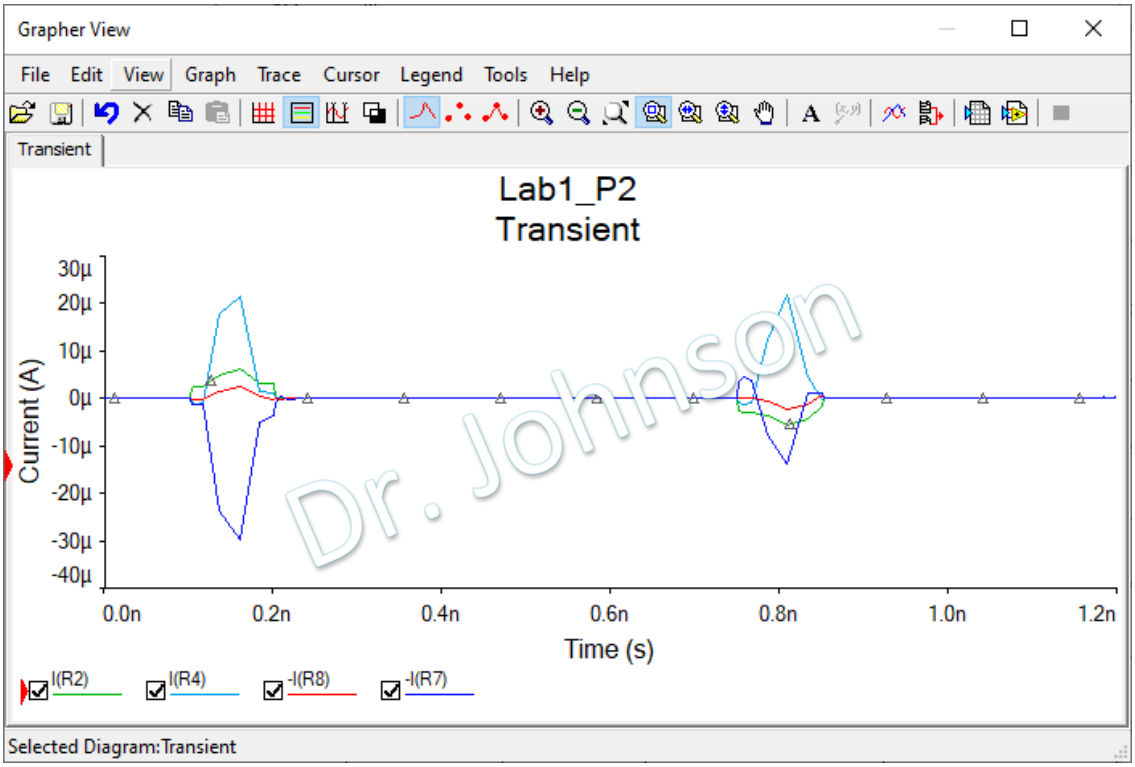
g) With the load capacitor disconnected plot the I(R1) and I(R2)

Note: Though we often think of CMOS gates as having zero input current, there is clearly a significant current here, why?



h) With the load capacitor disconnected, plot the 4 terminal currents for each transistor

Note: The sum of these should equal 0 for each transistor


Grapher View
File Edit View Graph Trace Cursor Legend Tools Help
Transient
Lab1_P2
Transient
30µ
20µ
10µ
0µ
-10µ
-20µ
-30µ
-40µ
Current (A)
0.0n
0.2n
0.4n
0.6n
0.8n
1.0n
1.2n
Time (s)
I(R2)
I(R4)
-I(R8)
-I(R7)
Dr. Johnson
Selected Diagram:Transient