ELE 3510 Lab 2: CMOS Gates

1 dedicated lab period, 1 lab period to complete

Objectives

- Design a CMOS gate
- Optimize for performance
- Remove simulation artifacts

Prelab

student check off

- Review the CMOS Circuits Notes ☐

Assignment

Part 1: **Design a 2 input CMOS NAND gate**

Optimize for matching delays and rise/fall times

Part 2: **Simulate your 2 input NAND gate**

Use the Measuring Gate Delays notes:

verify operation

Quantify the delays (0-1, 1-0) and rise and fall times

Part 3: **Design a 2 input CMOS NOR gate**

Optimize for minimum size

Part 4: **Simulate your 2 input NOR gate**

Use the Measuring Gate Delays notes:

verify operation

Quantify the delays (0-1, 1-0) and rise and fall times

Check Off

You must demonstrate your working design(s) prior to the beginning of the next lab period

- Demo the part 2 results 40%
- Demo the part 4 results 40%

Lab Report (informal)

- Due at 4:00 pm, the day of the next lab period – in the box
- Include a properly documented informal lab report. 20%