ELE3510 Lab 4: Registers, Counters, and Clocks – Oh My!

1 dedicated lab period, 1 lab period to complete

Objectives

- Review Register, Counter, and Clock concepts
- Utilize the switches and seven segment displays

Prelab

	student check off
• Review the SSEG display info from CE1911/CPE1500	☐
• Review the Register, Counter and Clock class notes	☐

Assignment

Part 1: Further the genericization of the clock divider – "third try" code

Specifications:

1) Create an additional constant to replace the vector range values (xx downto 0) that is calculated based on the divide factor (used 3 times)
2) Implement 3 clock dividers on the DE10: 1Hz, 4Hz, 16Hz
3) Tie the output of each divider to a single LED
4) Generics:
   a. at least 1 additional
5) Input signals:
   a. rstb
   b. clk
6) Output signals:
   a. LED for each clock divider

Part 2: Create a simple pipeline (No DE10)

Specifications:

1) Create a Modulo N counter (N < 16)
2) Feed the output of the counter to a 4 bit register (Reg _1)
3) Feed the output of Reg_1 to a 4 bit register (Reg _2)
4) Feed the output of Reg_2 to a 4 bit register (Reg _3)
5) Feed the output of Reg_3 to a 4 bit register (Reg _4)
6) Create a testbench and simulate your design for N = 12
   a. Watch the count ripple through the pipeline

Check Off

You must demonstrate your working design(s) prior to the beginning of the next lab period

- Demo the Clock Divider (DE10) 40%
- Demo the Pipeline (Simulation) 40%

Lab Report (informal)

- Due at 4:00 pm, the day of the next lab period – in the box
- Include a properly documented informal lab report. 20%