ELE3510 Lab 5: Registers, Counters, and Clocks – Oh My!

1 dedicated lab period, 1 lab period to complete

Objectives

- Review Register, Counter, and Clock concepts
- Utilize the switches, LEDs and seven segment displays

Prelab

student check off

- Review the Register, Counter and Clock class notes ☐

Assignment

Part 1: Further the genericization of the clock divider – "third try" code

Specifications:

1) Create an additional constant to replace the vector range values (xx downto 0) that is calculated based on the divide factor (used 3 times)
2) Implement 3 clock dividers on the same DE10 design: 1Hz, 4Hz, 16Hz
3) Tie the output of each divider to a 7-seg display
4) Generics:
   a. at least 1 additional
5) Input signals:
   a. rstb
   b. clk
6) Output signals:
   a. 4, 7-segs flashing the number 1,4,16 at the attached clock rate

Part 2: Create and simulate a Register File

Specifications:

1) 8 – 8bit registers
2) 2 – data outputs, 2 data sel inputs
3) 1 – write data input, 1 write select input
4) clk, we_b

Create a testbench and simulate your design

Show unknowns at beginning of the sim

Write 1010 0101 into the even number registers and 0101 1010 into the odd number registers.

Output all 8 registers to both data outputs

Check Off

You must demonstrate your working design(s) prior submission of your report

- Demo the Clock Divider (DE10) and informal report 50%
- Demo the Register File (Simulation) and informal report 50%
- Due at 3:00 pm, 6 days following the lab period – in the box