

# MAX 10 – Toolkit ADC Example

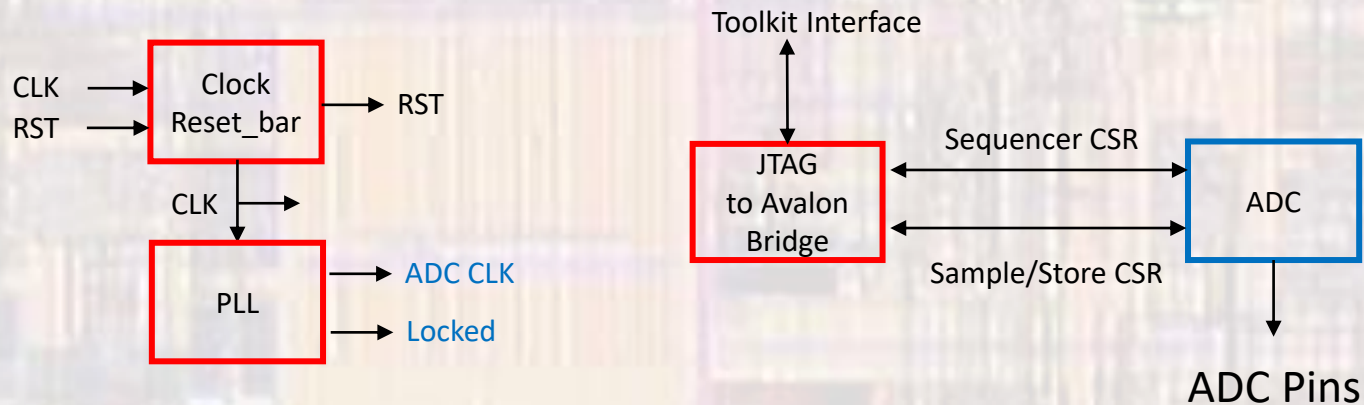
Last updated 7/20/23

# Max10 ADC Example - Toolkit

- ADC Configuration
  - 3 approaches to using the ADCs
    - Used as part of a NIOS system
      - Avalon interface built in by Platform Designer
    - Used with a hand built interface
      - Emulate the Avalon interface
    - Used with the Quartus ToolKit (Inside System Console) to verify operation
      - Avalon interface built into the toolkit

# Max10 ADC Example - NIOS

- Nios ADC
  - Create a system to use the ADC with the Toolkit



# Max10 ADC Example - Toolkit

- ADC Example – using ADC Toolkit
  - Platform Planner

Clk driver required for PLL

10MHz PLL output

ADC Block

Debug interface for Toolkit

Toolkit controls the Avalon Interface through this module

Use	Connections	Name	Description	Export	Clock	Base
<input checked="" type="checkbox"/>		<b>clk_0</b>	Clock Source			
		clk_in	Clock Input	<b>clk</b>	<b>exported</b>	
		clk_in_reset	Reset Input	<b>reset</b>		
		clk	Clock Output	<i>Double-click to export</i>	clk_0	
		clk_reset	Reset Output	<i>Double-click to export</i>		
<input checked="" type="checkbox"/>		<b>altpll_0</b>	ALTPLL Intel FPGA IP			
		indk_interface	Clock Input	<i>Double-click to export</i>	<b>clk_0</b>	
		indk_interface_reset	Reset Input	<i>Double-click to export</i>	[indk_interf...	
		pll_slave	Avalon Memory Mapped Slave	<i>Double-click to export</i>	[indk_interf...	
		c0	Clock Output	<i>Double-click to export</i>	altpll_0_c0	
		locked_conduit	Conduit	<i>Double-click to export</i>		
<input checked="" type="checkbox"/>		<b>modular_adc_0</b>	Modular ADC core Intel FPGA IP			
		clock	Clock Input	<i>Double-click to export</i>	<b>clk_0</b>	
		reset_sink	Reset Input	<i>Double-click to export</i>	[clock]	
		adc_pll_clock	Clock Input	<i>Double-click to export</i>	<b>altpll_0_c0</b>	
		adc_pll_locked	Conduit	<i>Double-click to export</i>		
		sequencer_csr	Avalon Memory Mapped Slave	<i>Double-click to export</i>	[clock]	<input checked="" type="checkbox"/> 0x0000
		sample_store_csr	Avalon Memory Mapped Slave	<i>Double-click to export</i>	[clock]	<input checked="" type="checkbox"/> 0x0000
		sample_store_irq	Interrupt Sender	<i>Double-click to export</i>	[clock]	
<input checked="" type="checkbox"/>		<b>master_0</b>	JTAG to Avalon Master Bridge			
		clk	Clock Input	<i>Double-click to export</i>	<b>clk_0</b>	
		clk_reset	Reset Input	<i>Double-click to export</i>		
		master	Avalon Memory Mapped Master	<i>Double-click to export</i>	[clk]	
		master_reset	Reset Output	<i>Double-click to export</i>		

# Max10 ADC Example - Toolkit

- ADC Example – using ADC Toolkit
  - ADC Module

Configuration

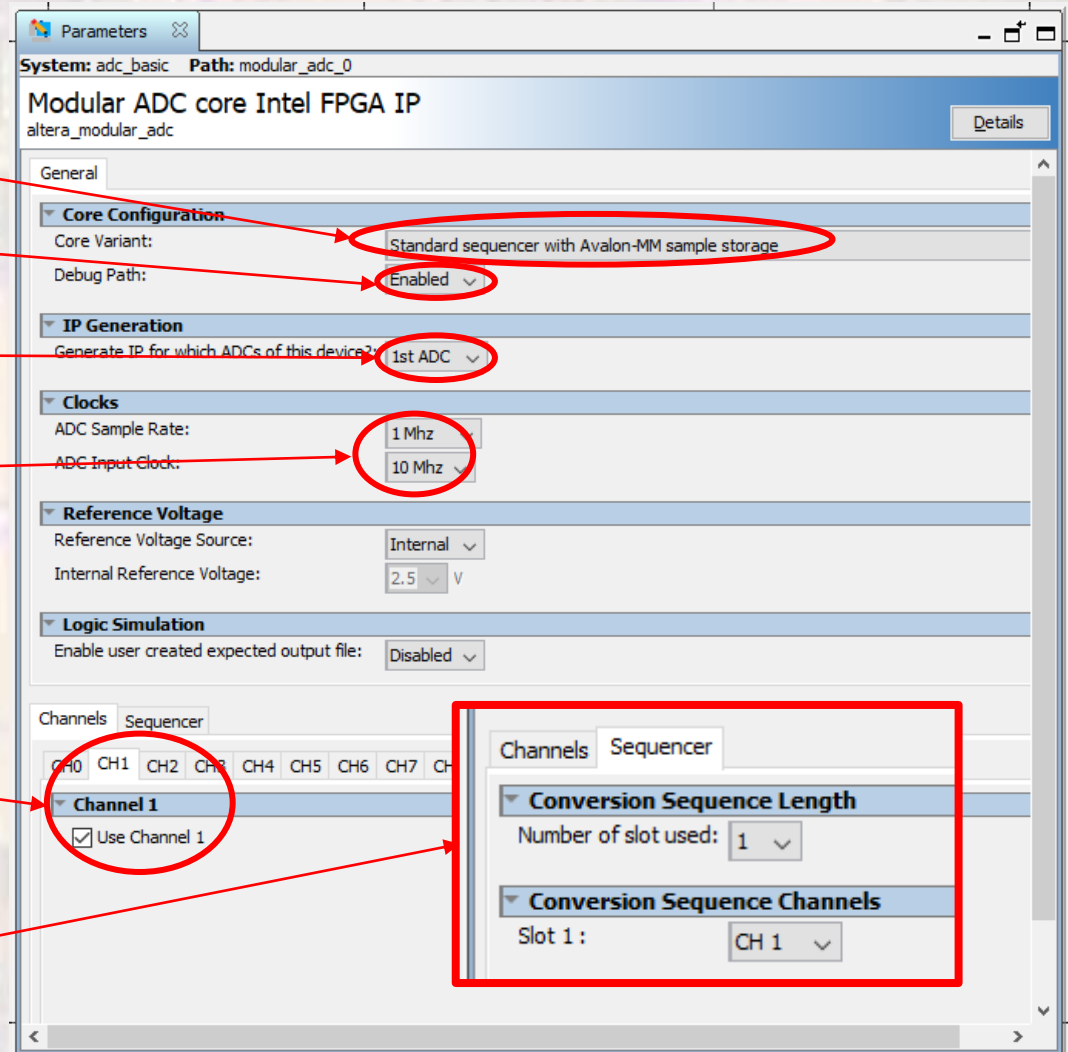
Enabled for the Toolkit

Only ADC1 available on DE10-Lite

Max Sample Rate  
Required Clock

Channel 1  
Arduino A0 pin

Sequencer Setup



# Max10 ADC Example - Toolkit

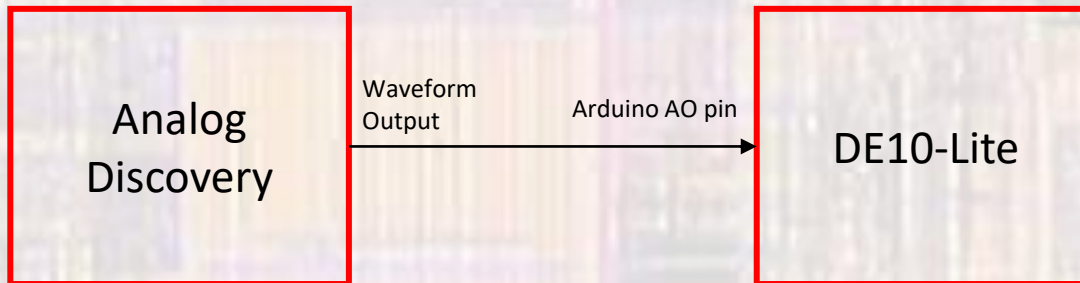
- ADC Example – using ADC Toolkit
  - DE10 top level design

```
-----  
-- adc_basic_de10.vhdl  
-- by: johnsontimoj  
-- created: 6/28/2018  
-- version: 0.0  
-----  
--  
-- ADC example - de10 implementation  
-- inputs: CLK, ADCin 1 (via IP)  
-- outputs: none  
-- Use System Console - ADC Toolkit for validation  
-----  
library ieee;  
use ieee.std_logic_1164.all;  
use ieee.numeric_std.all;  
entity adc_basic_de10 is  
    port ( CLOCK_50:      in std_logic  
          );  
end entity;
```

```
architecture topLevel of adc_basic_de10 is  
    component adc_basic is  
        port (  
            clk_clk      : in std_logic := 'X'; -- clk  
            reset_reset_n : in std_logic := 'X'; -- reset_n  
        );  
    end component adc_basic;  
begin  
    u0 : component adc_basic  
        port map (  
            clk_clk      => CLOCK_50,      -- clk.clk  
            reset_reset_n => '1',          -- reset.reset_n  
        );  
    -- no activity  
end architecture;
```

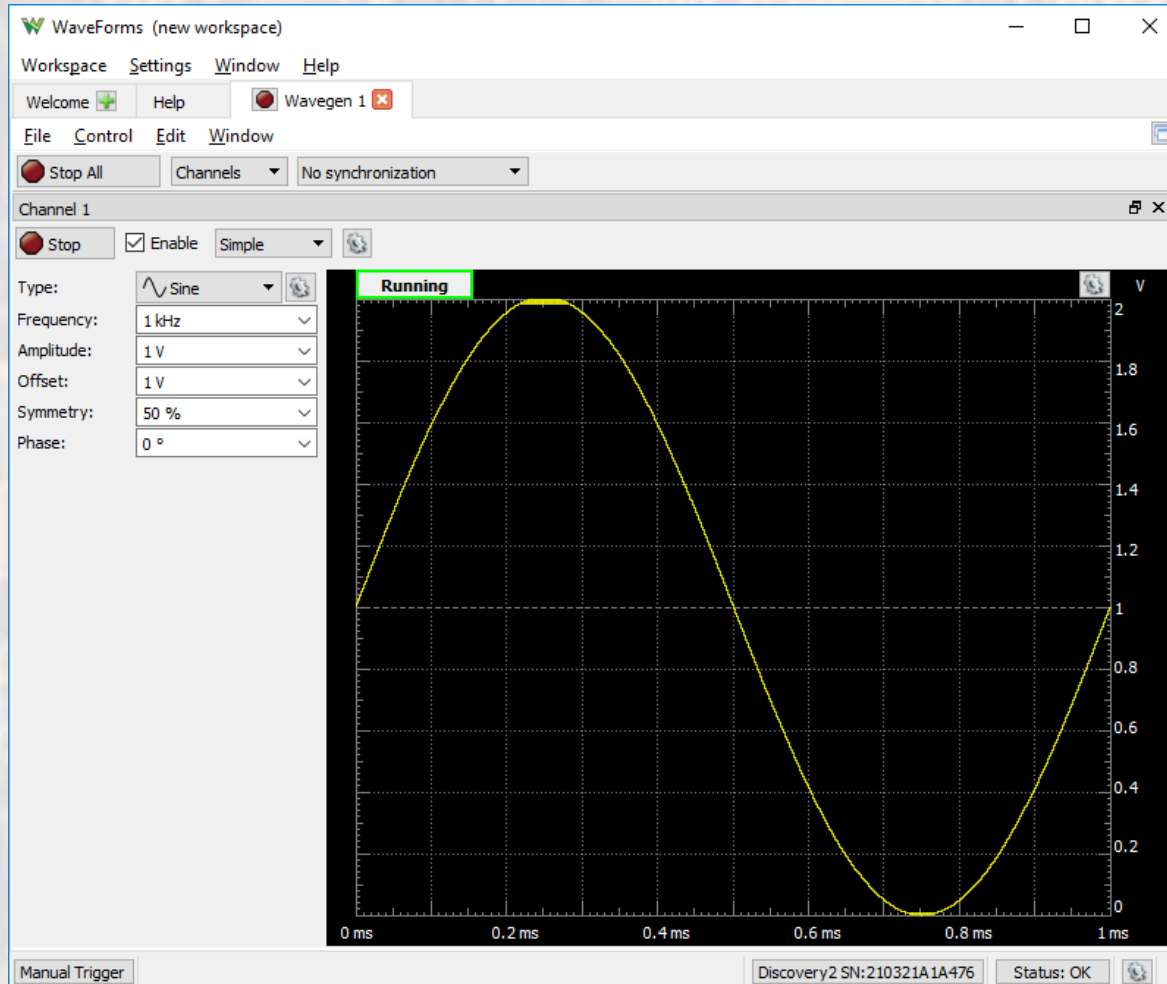
# Max10 ADC Example - Toolkit

- ADC Example – using ADC Toolkit
  - Setup



# Max10 ADC Example - Toolkit

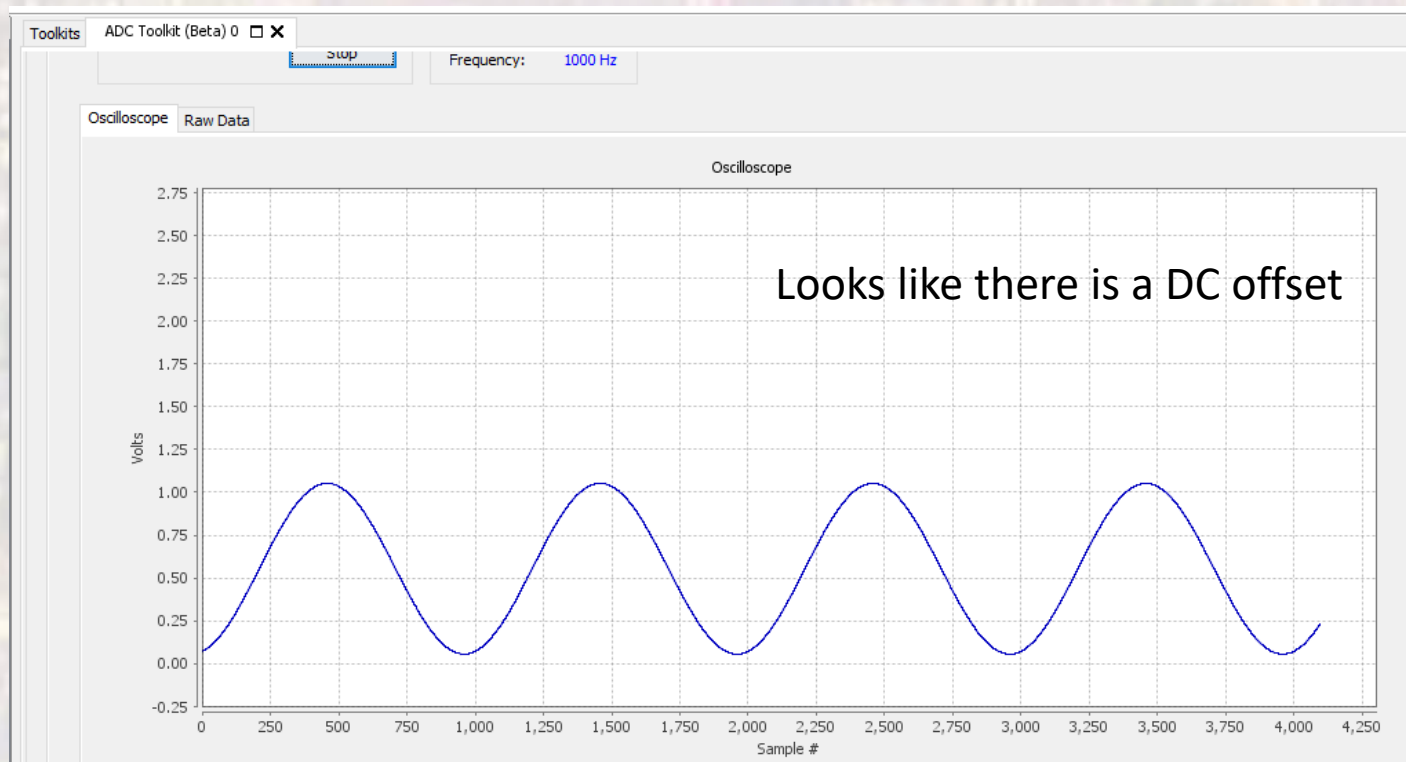
- ADC Example – using ADC Toolkit





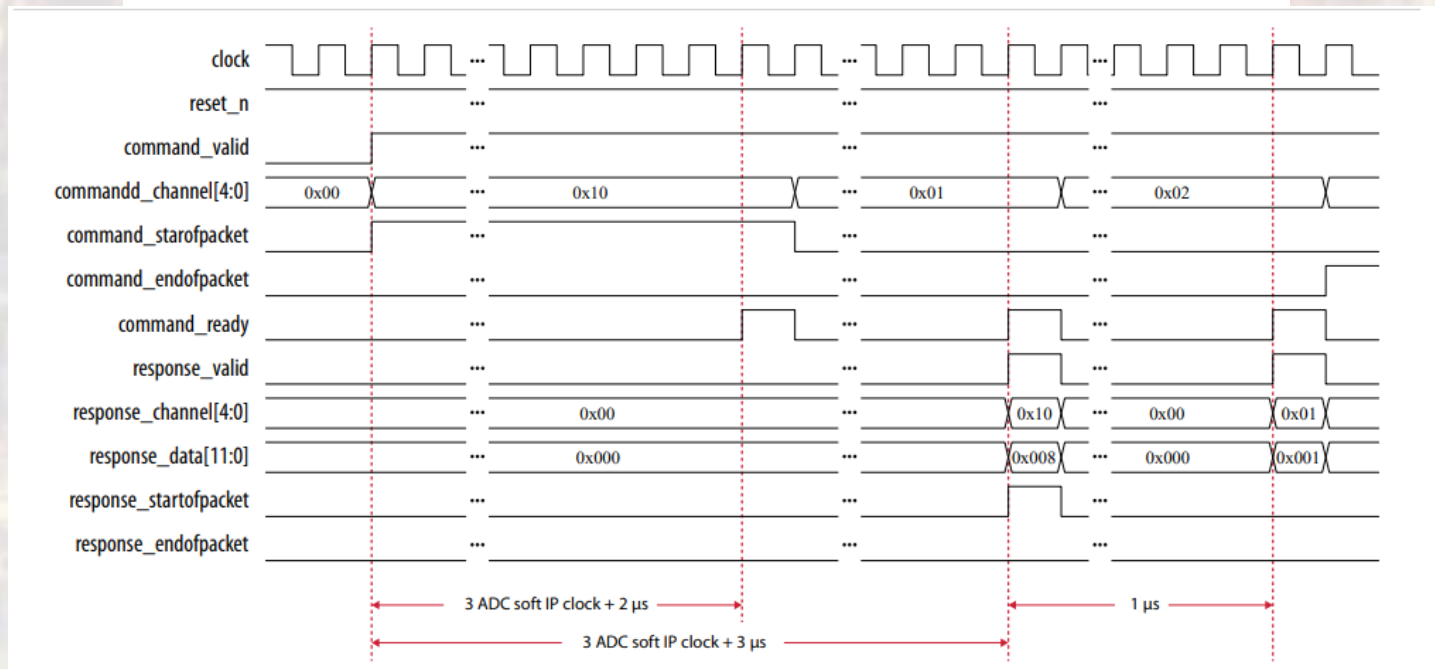
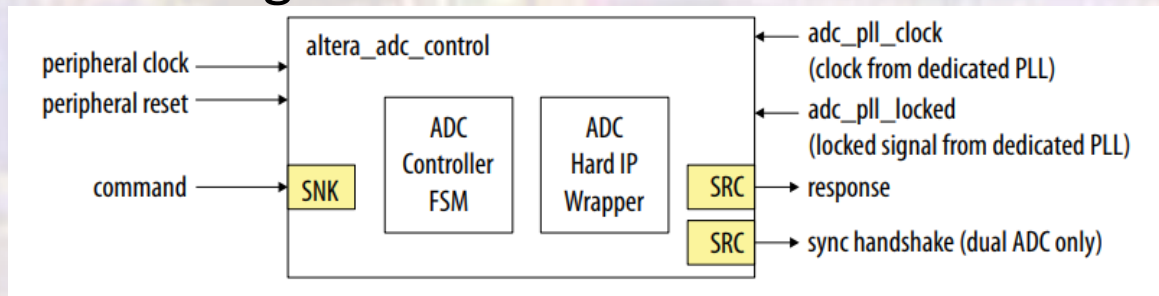
# Max10 ADC Example - Toolkit

- ADC Example – using ADC Toolkit
  - In Platform designer – Tools – System Console – ADC Toolkit
  - ADC Toolkit results



# Max10 ADC Example - Toolkit

- ADC Control Interfaces
  - To create a logic controller



# Max10 ADC Example - Toolkit

- DE10-Lite – ADC **WARNINGS**
  - Only ADC1 is brought out to pins
    - No access to ADC2 inputs at the FPGA pins
  - The pin #s are shifted
    - Arduino A0 is mapped to ADC1\_in1
    - ...
    - Arduino A5 is mapped to ADC1\_in6
  - No other ADC inputs are pinned out