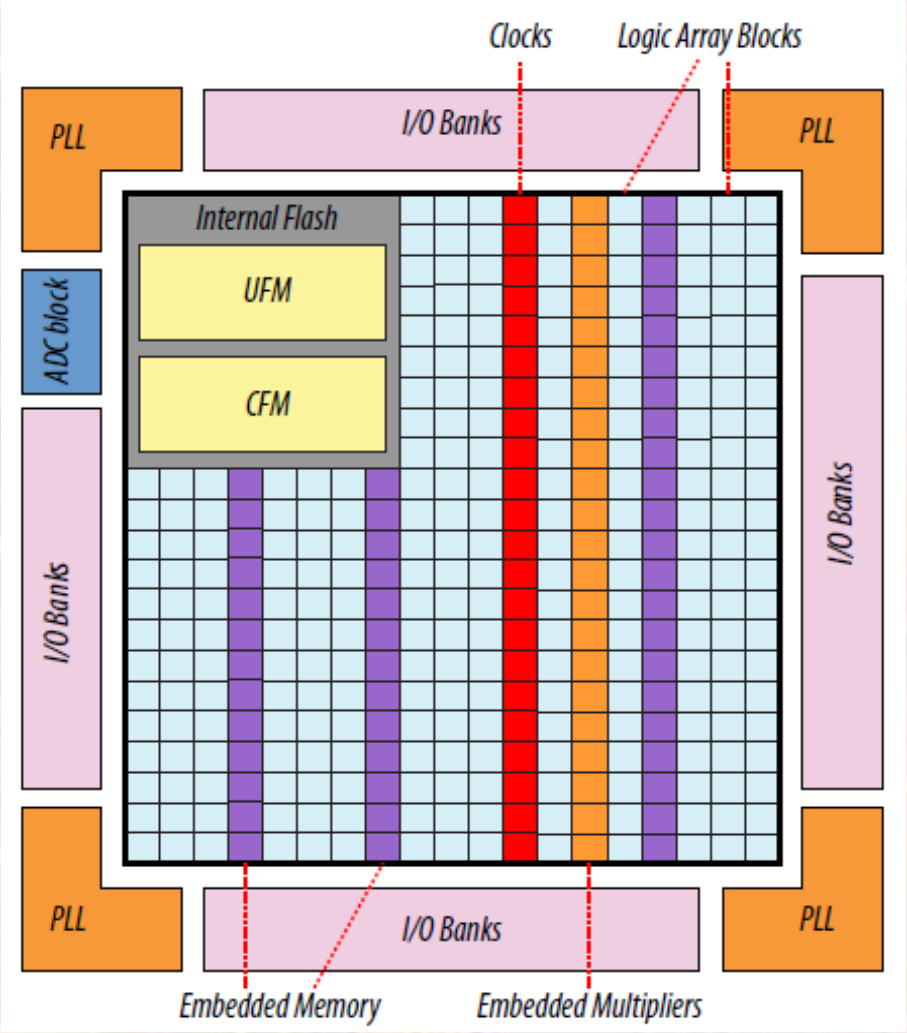
MAX10 - Architecture

Last updated 7/19/23

FPGA MAX10

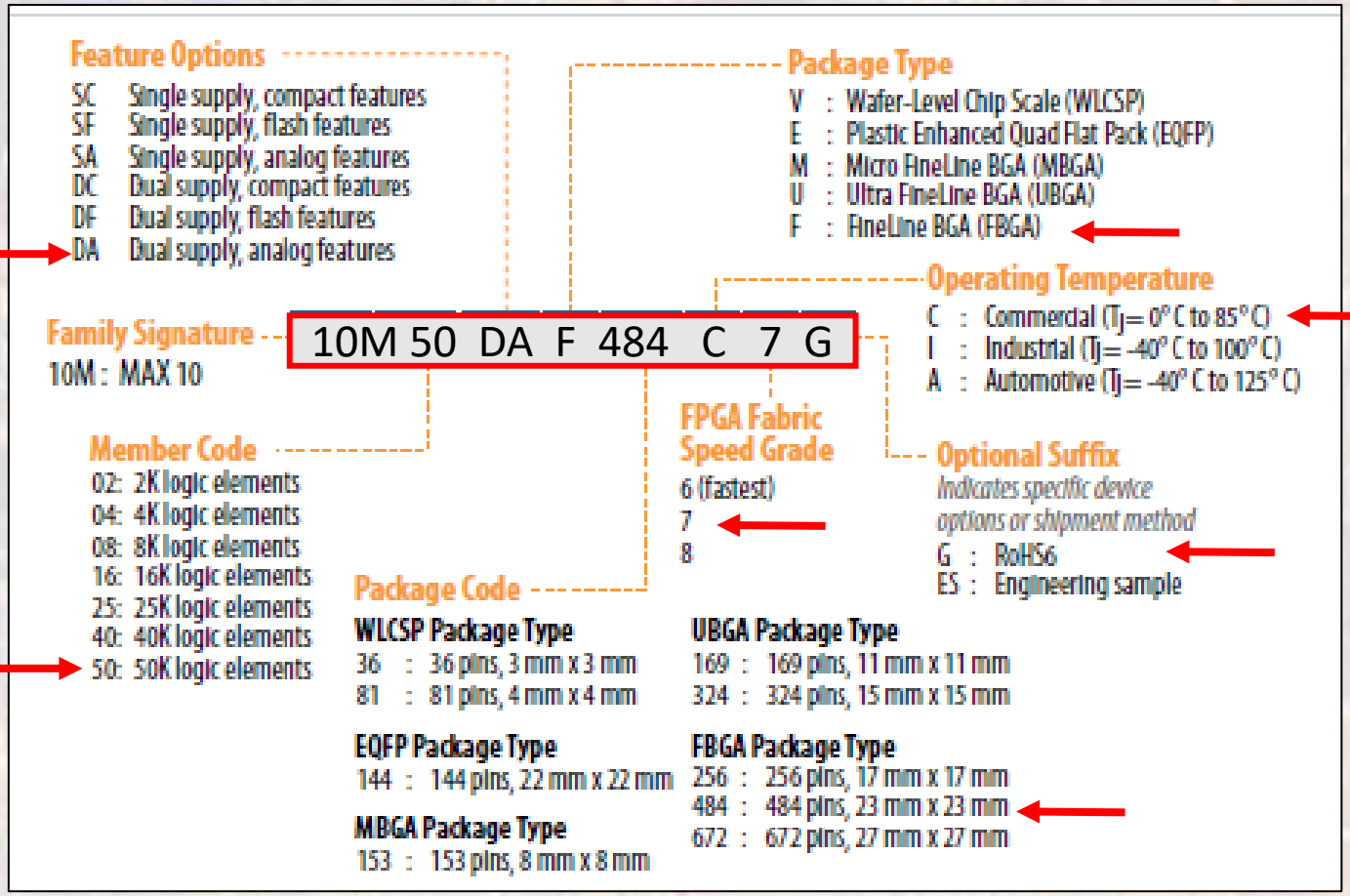
- Top Level View



Src: MAX 10 Device Handbook

FPGA MAX10

- Top Level View
  - 10M50DAF484C7G



Src: MAX 10 Device Overview

FPGA MAX10

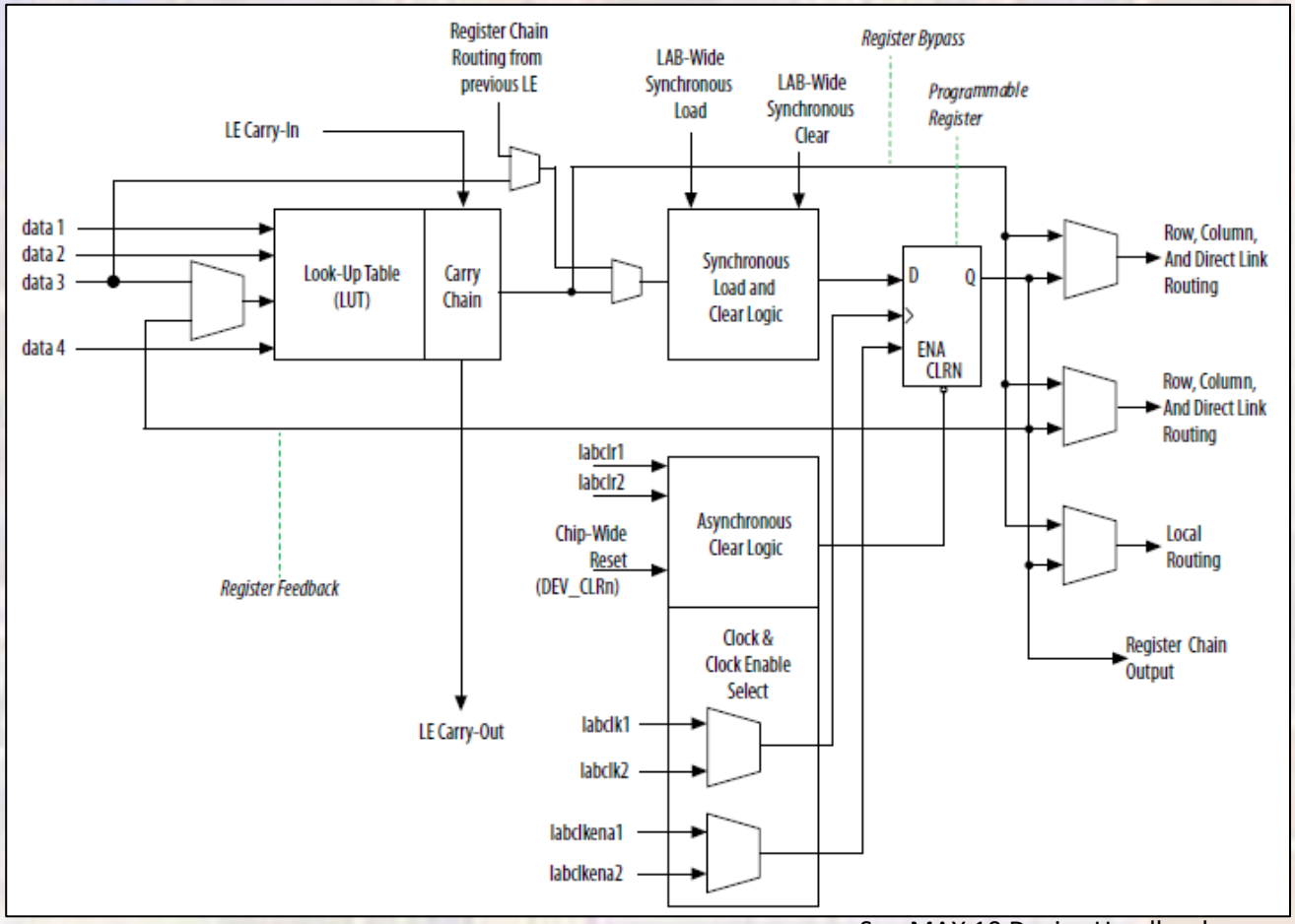
- Top Level View
  - 10M50DAF484C7G

Resource		Device						
		10M02	10M04	10M08	10M16	10M25	10M40	10M50
Logic Elements (LE) (K)		2	4	8	16	25	40	50
M9K Memory (Kb)		108	189	378	549	675	1,260	1,638
User Flash Memory (Kb) (1)		96	1,248	1,376	2,368	3,200	5,888	5,888
18 × 18 Multiplier		16	20	24	45	55	125	144
PLL		2	2	2	4	4	4	4
GPIO		160	246	250	320	380	500	500
LVDS	Dedicated Transmitter	10	15	15	22	26	30	30
	Emulated Transmitter	73	114	116	151	181	241	241
	Dedicated Receiver	73	114	116	151	181	241	241
Internal Configuration Image		1	2	2	2	2	2	2
ADC		—	1	1	1	2	2	2

Src: MAX 10 Device Overview

FPGA MAX10

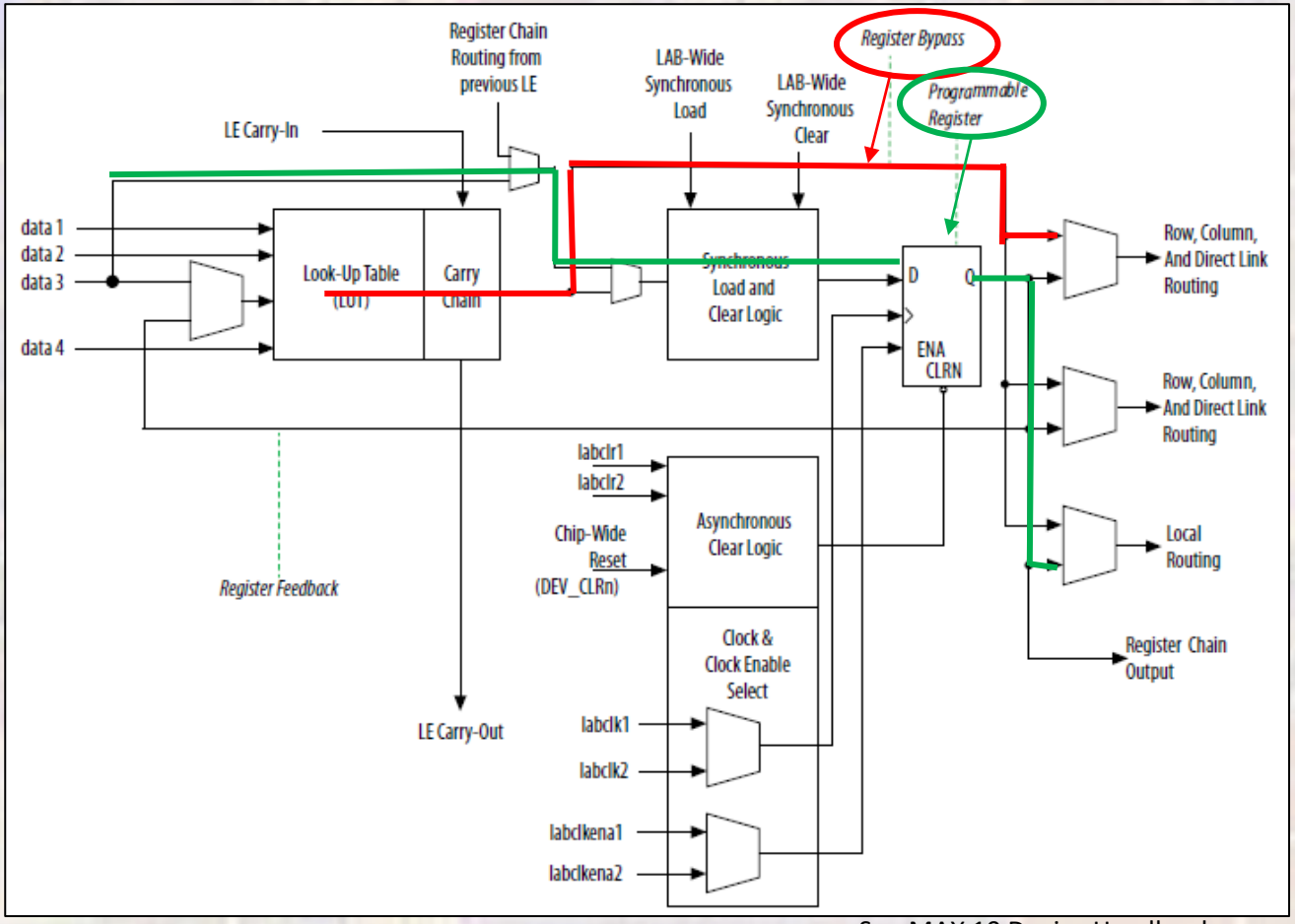
- Logic
  - Array of Logic Elements (LEs) – 50K LEs



Src: MAX 10 Device Handbook

FPGA MAX10

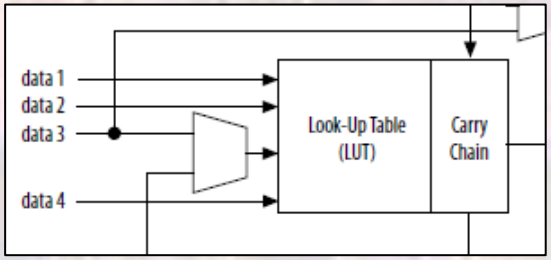
- Logic Element
  - 1 LE can have both an asynchronous and synchronous path

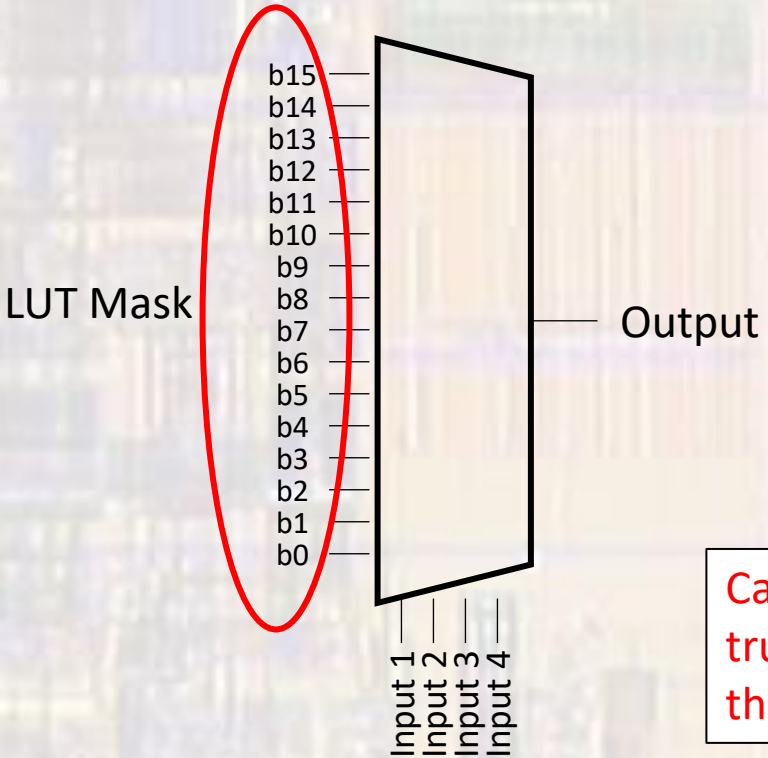


Src: MAX 10 Device Handbook

FPGA MAX10

- Logic Element
  - Look-Up Table (LUT)
    - Multiplexor





Inputs				
4	3	2	1	OUT
0	0	0	0	b0
0	0	0	1	b1
0	0	1	0	b2
0	0	1	1	b3
0	1	0	0	b4
0	1	0	1	b5
0	1	1	0	b6
0	1	1	1	b7
1	0	0	0	b8
1	0	0	1	b9
			0	b10
			1	b11
			0	b12
			1	b13
			0	b14
1	1	1	1	b15

Can create any 4 input truth table by choosing the desired LUT Mask

FPGA MAX10

- Logic Element
  - Look-Up Table (LUT) - example

    (In1 | In2) & (In2 | In3) & !(In4)

There are not groups of logic gates on the FPGA – logic is implemented by the LUTs

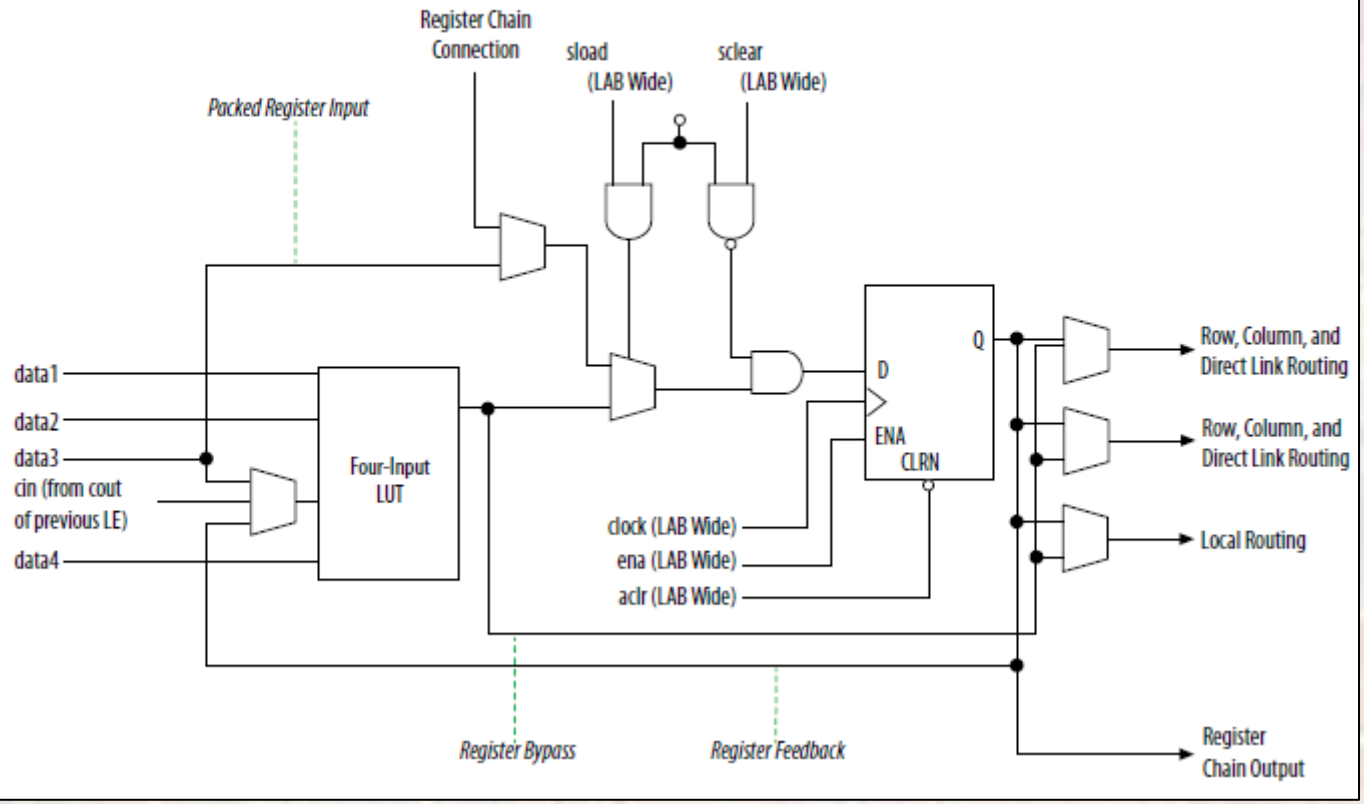
Inputs				OUT
4	3	2	1	
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

LUT Mask = 0x00EC

FPGA MAX10

- Logic Element
  - Normal Mode

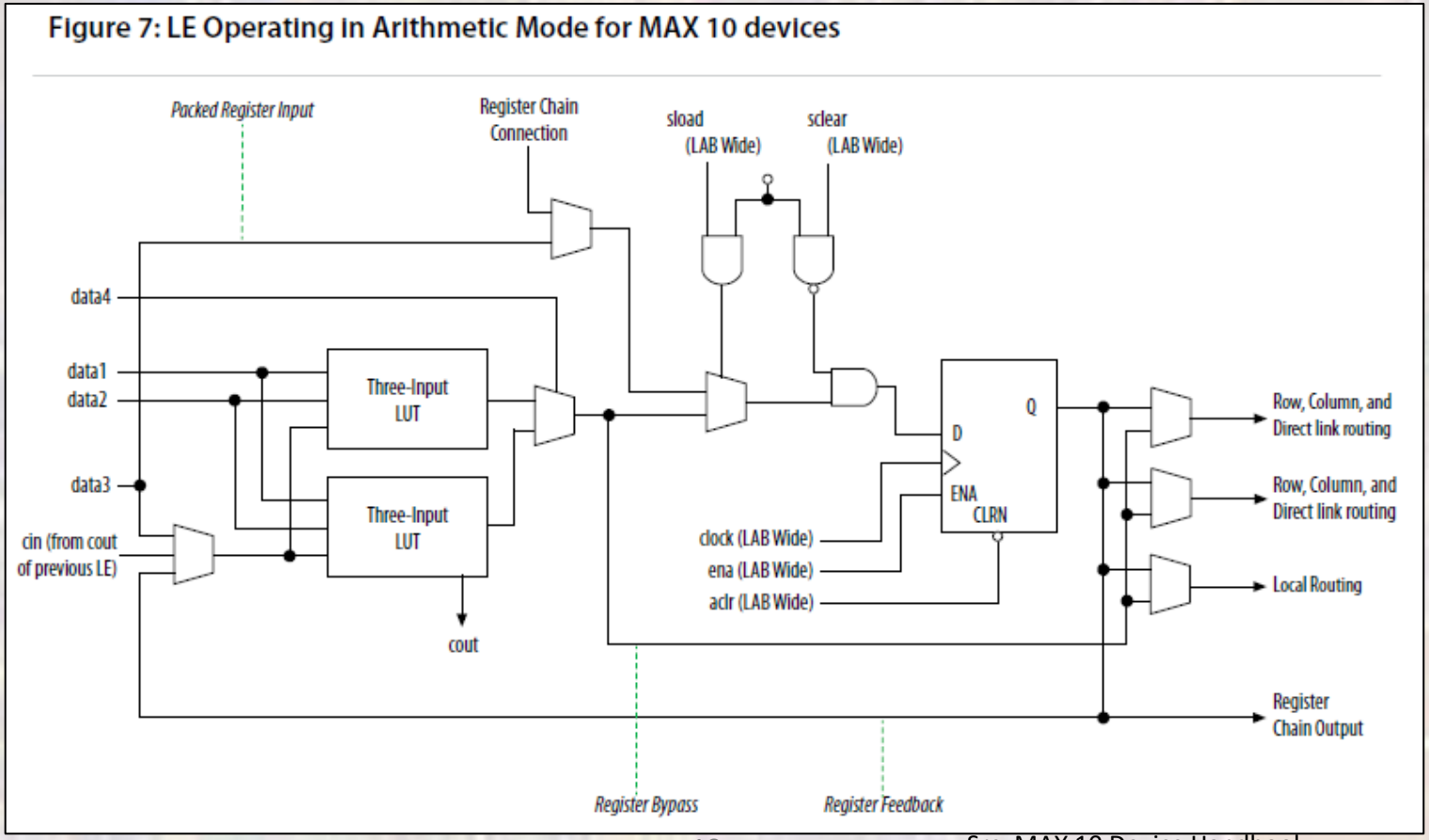
Figure 6: LE Operating in Normal Mode for MAX 10 devices



Src: MAX 10 Device Handbook

FPGA MAX10

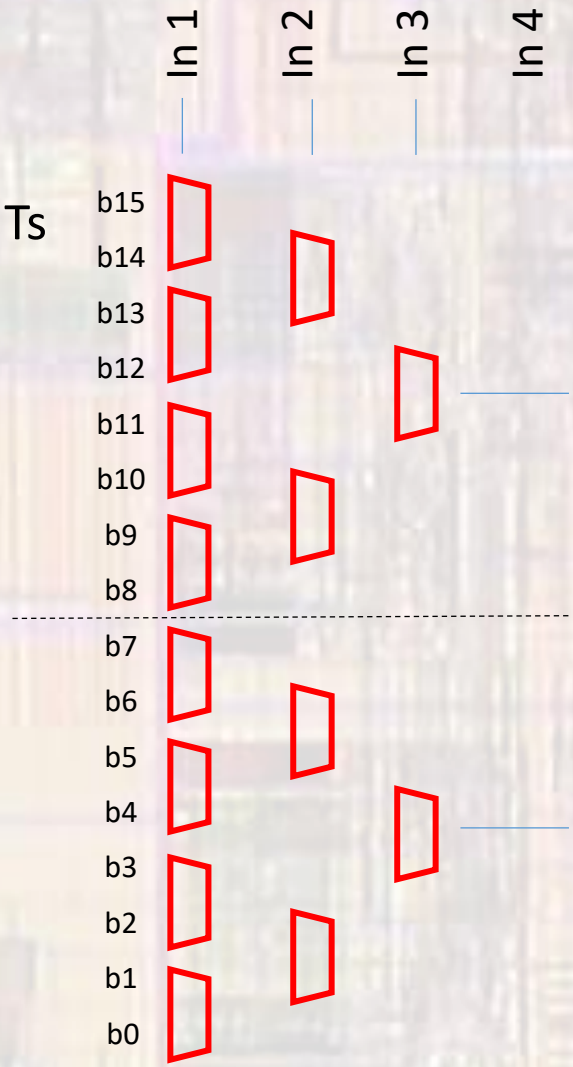
- Logic Element
  - Arithmetic Mode
    - 1 LUT can implement an adder



Src: MAX 10 Device Handbook

FPGA MAX10

- Logic Element
  - Partial LUT Mode
    - 1 LUT → 2, 3 input LUTs

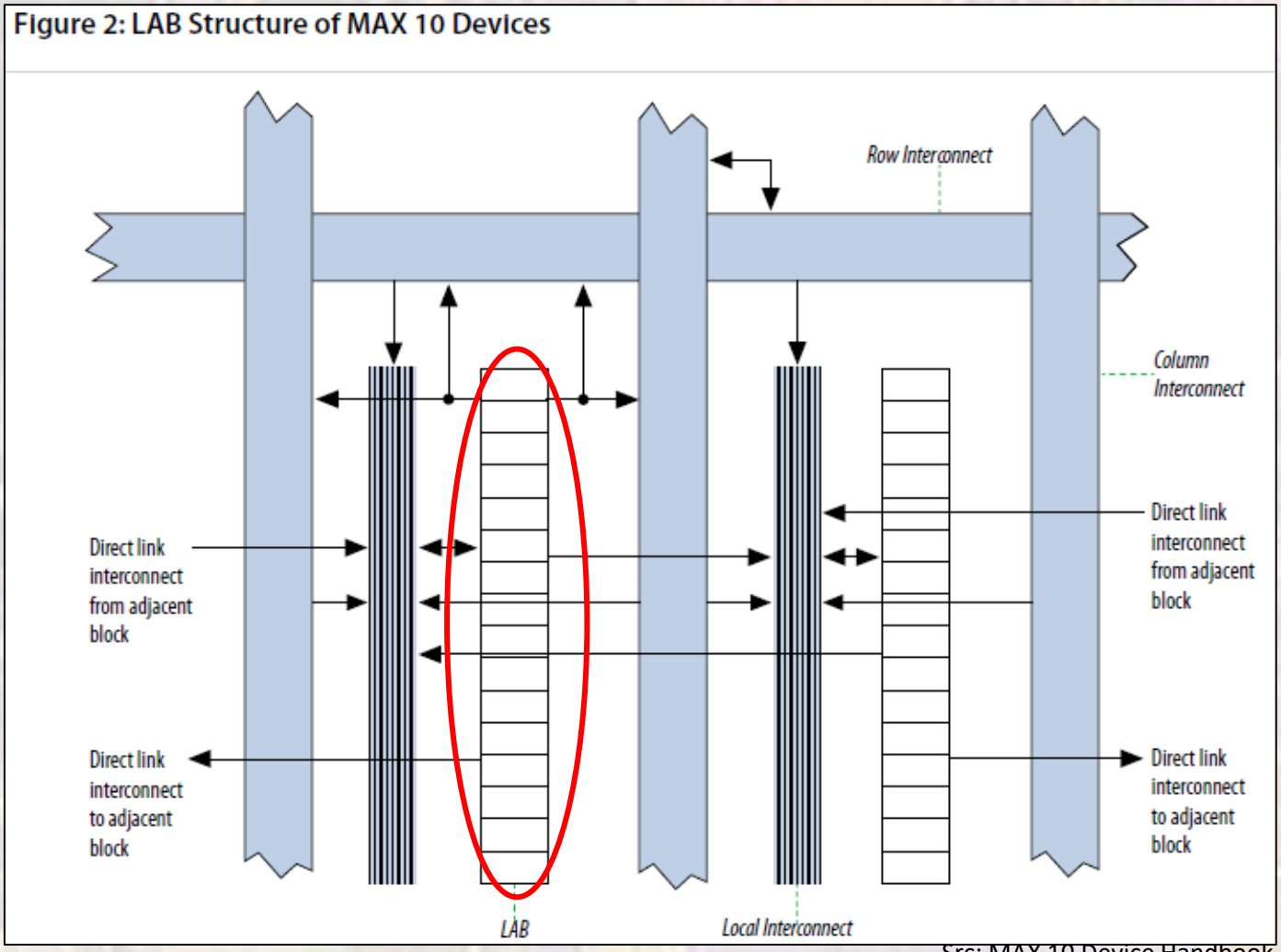


FPGA MAX10

- Logic Array Block (LAB)
  - 16 LEs
  - LAB control signals
  - LE carry chains
  - Register chains
  - Local interconnect

FPGA MAX10

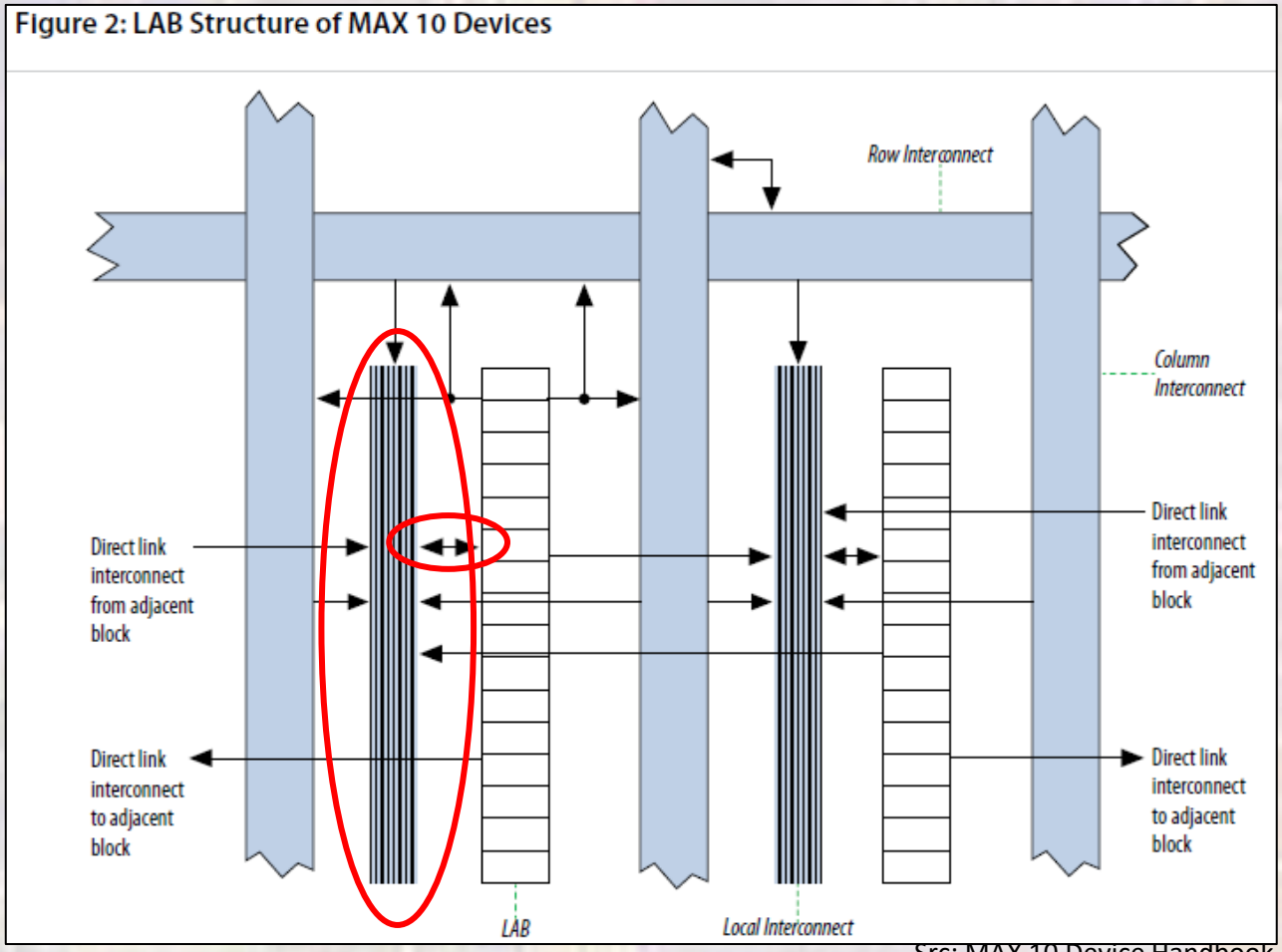
- LAB



Src: MAX 10 Device Handbook

FPGA MAX10

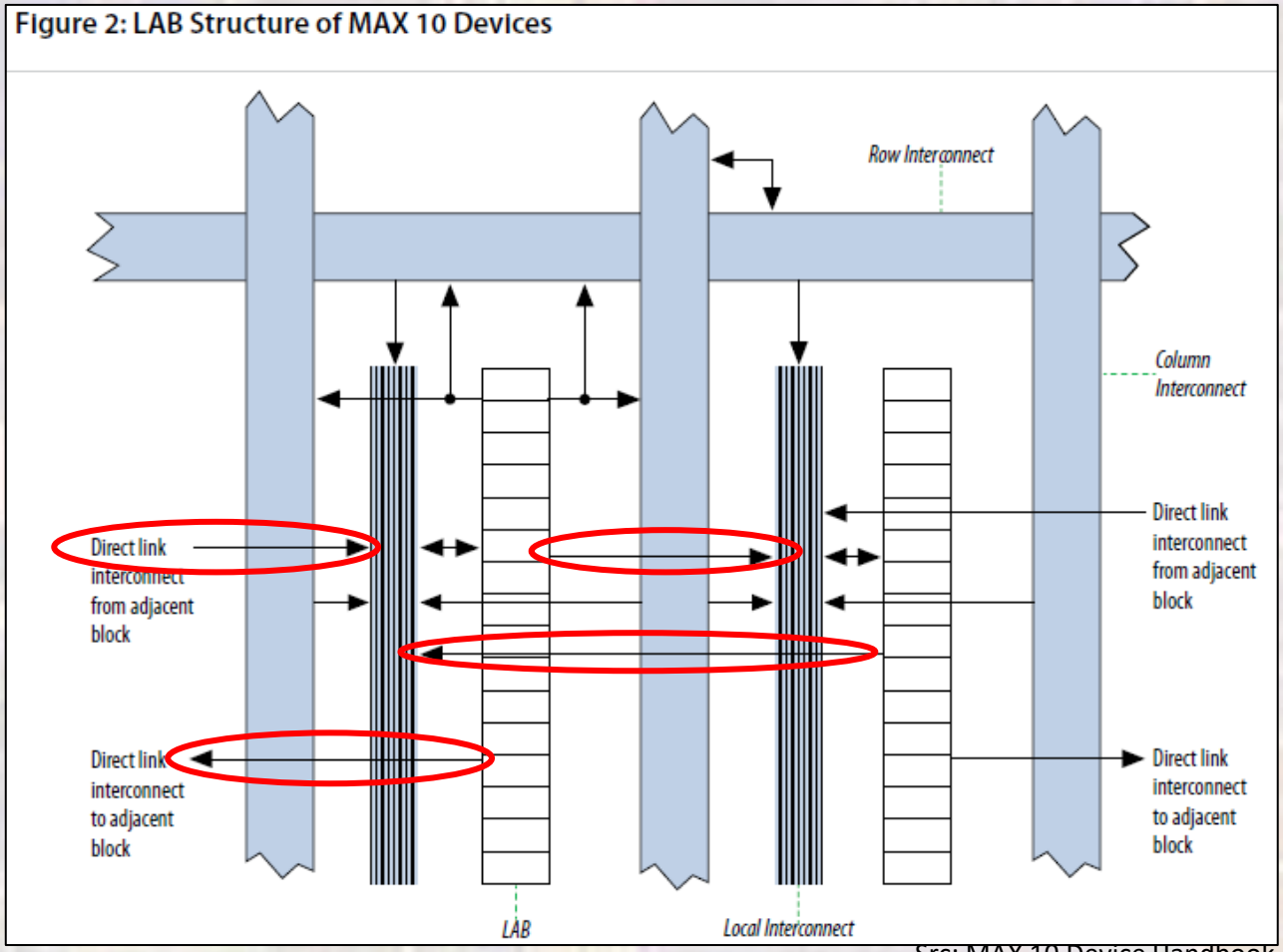
- Multiple Levels of Interconnect
  - Local Interconnect



Src: MAX 10 Device Handbook

FPGA MAX10

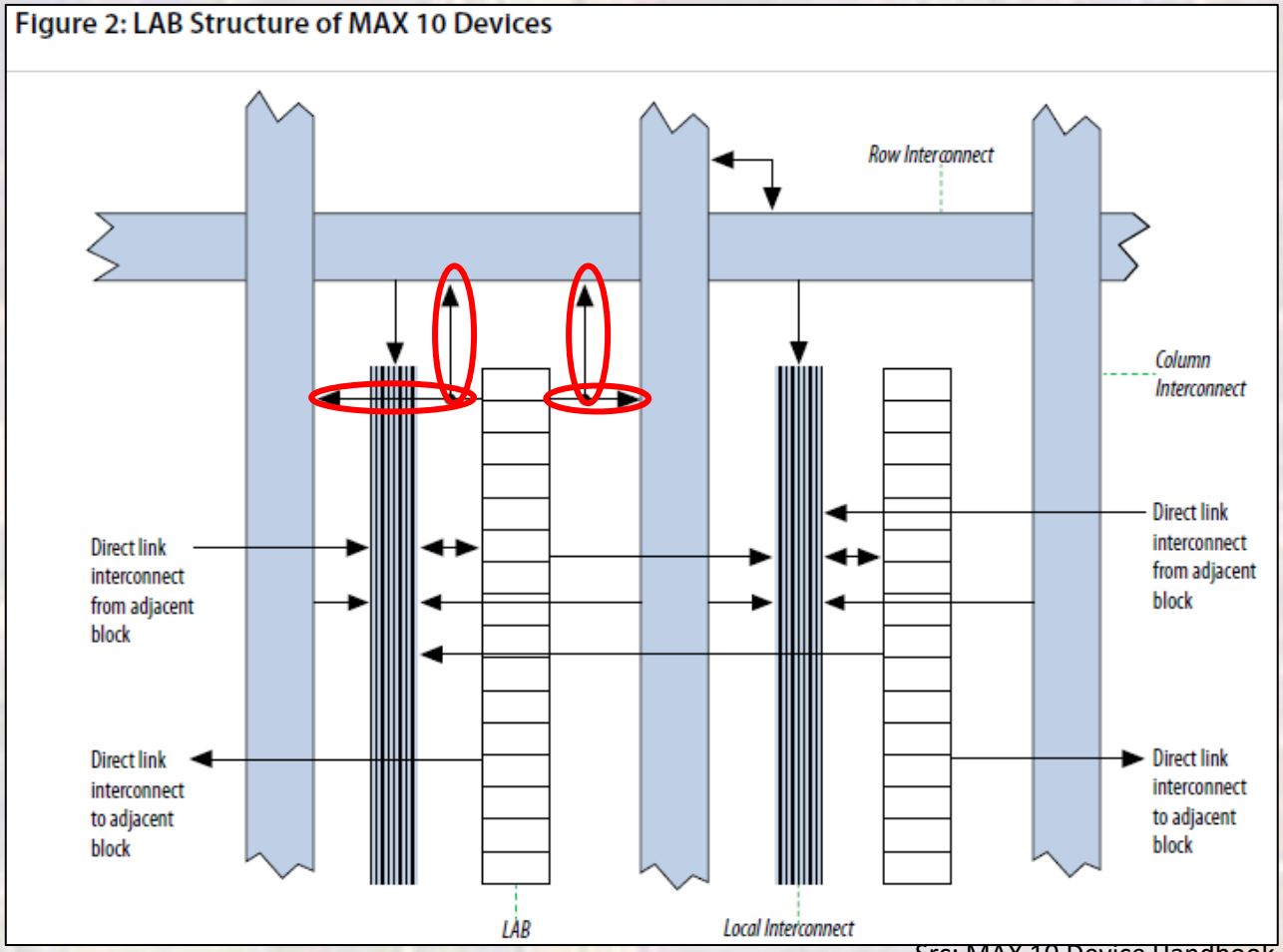
- Multiple Levels of Interconnect
  - Direct Link Interconnect



Src: MAX 10 Device Handbook

FPGA MAX10

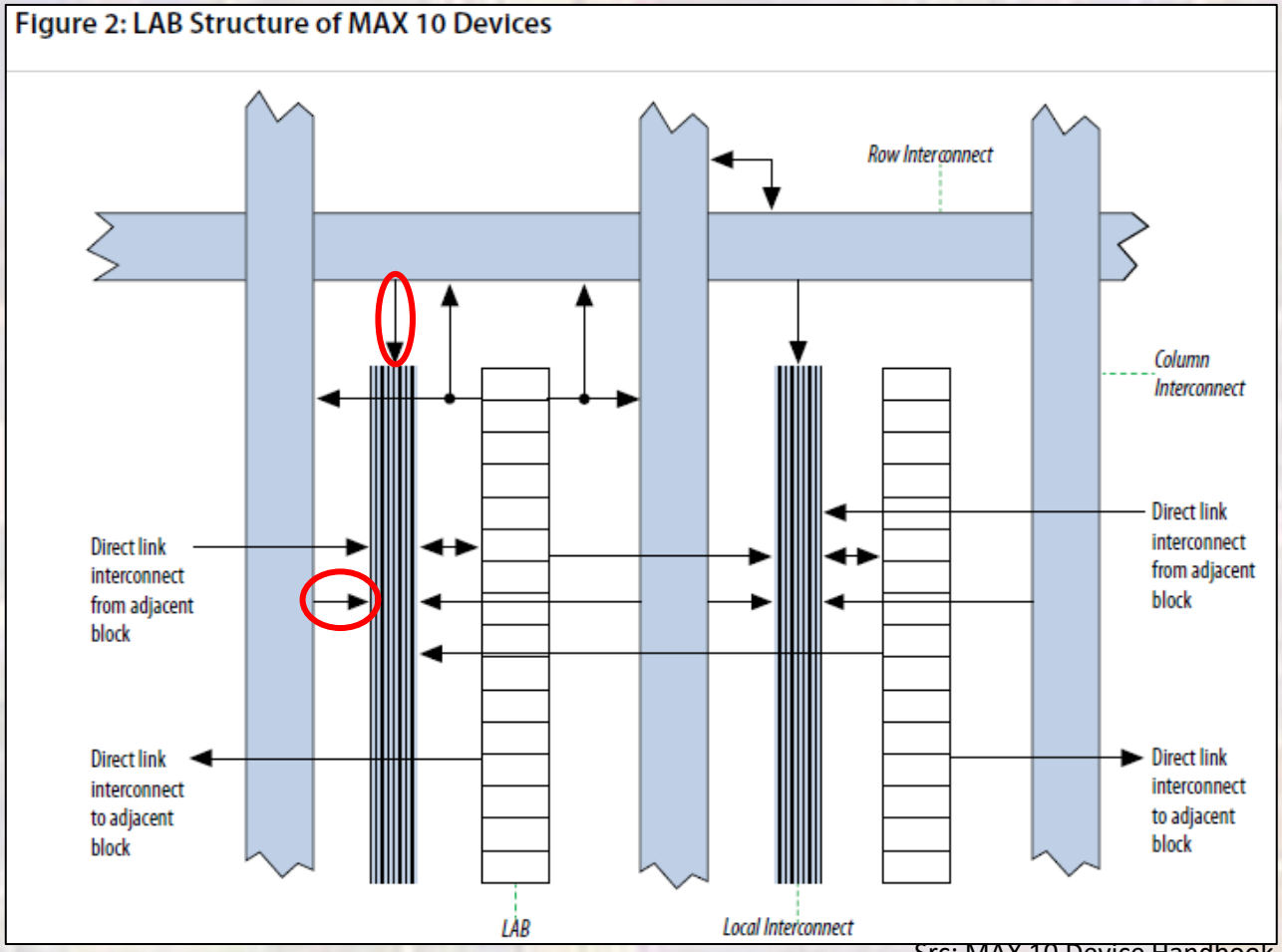
- Multiple Levels of Interconnect
  - Global Interconnect - direct



Src: MAX 10 Device Handbook

FPGA MAX10

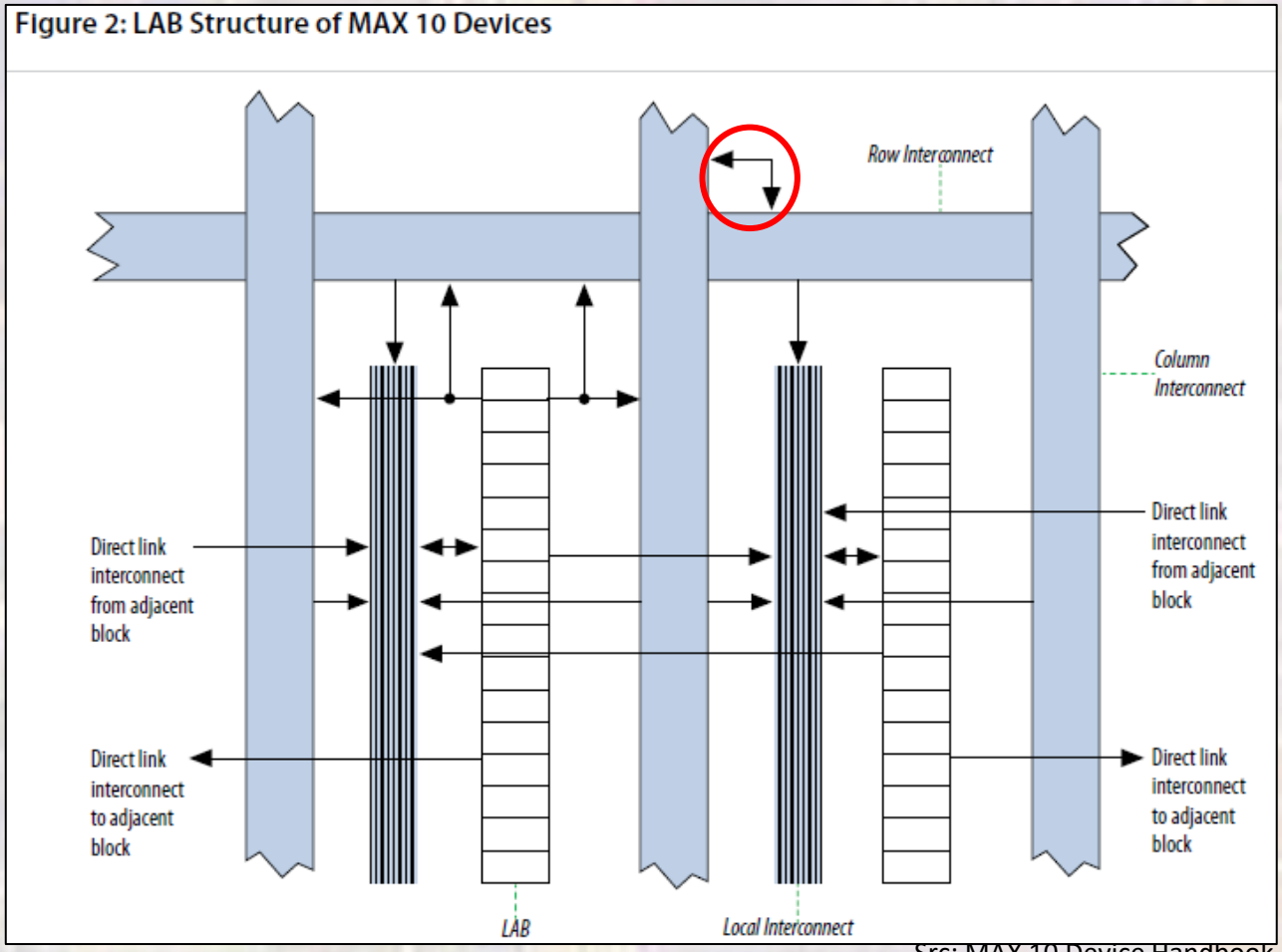
- Multiple Levels of Interconnect
  - Global Interconnect - indirect



Src: MAX 10 Device Handbook

FPGA MAX10

- Multiple Levels of Interconnect
  - Row/Column Interconnect

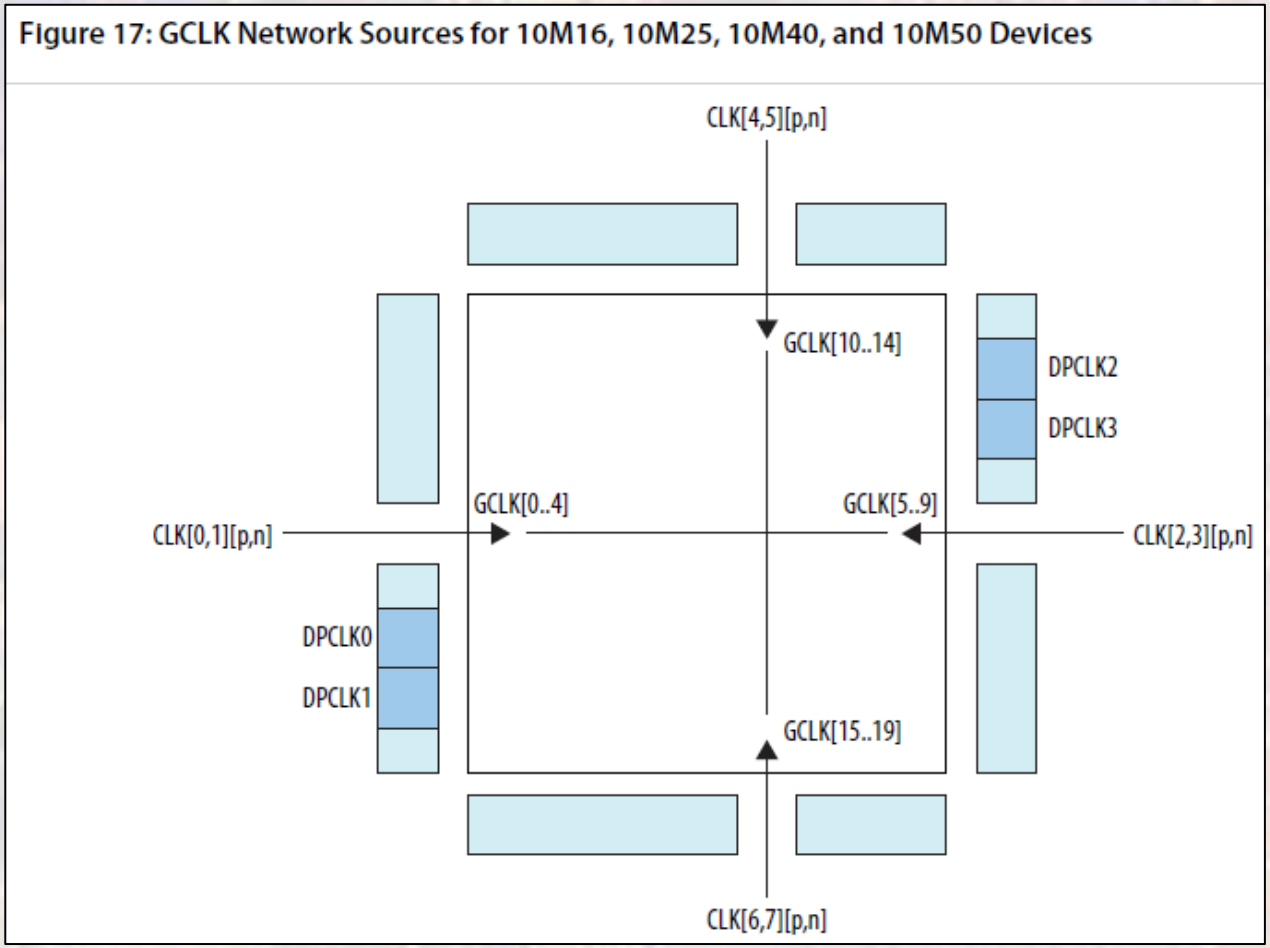


Src: MAX 10 Device Handbook

FPGA MAX10

- Additional Fixed Blocks - Clocks

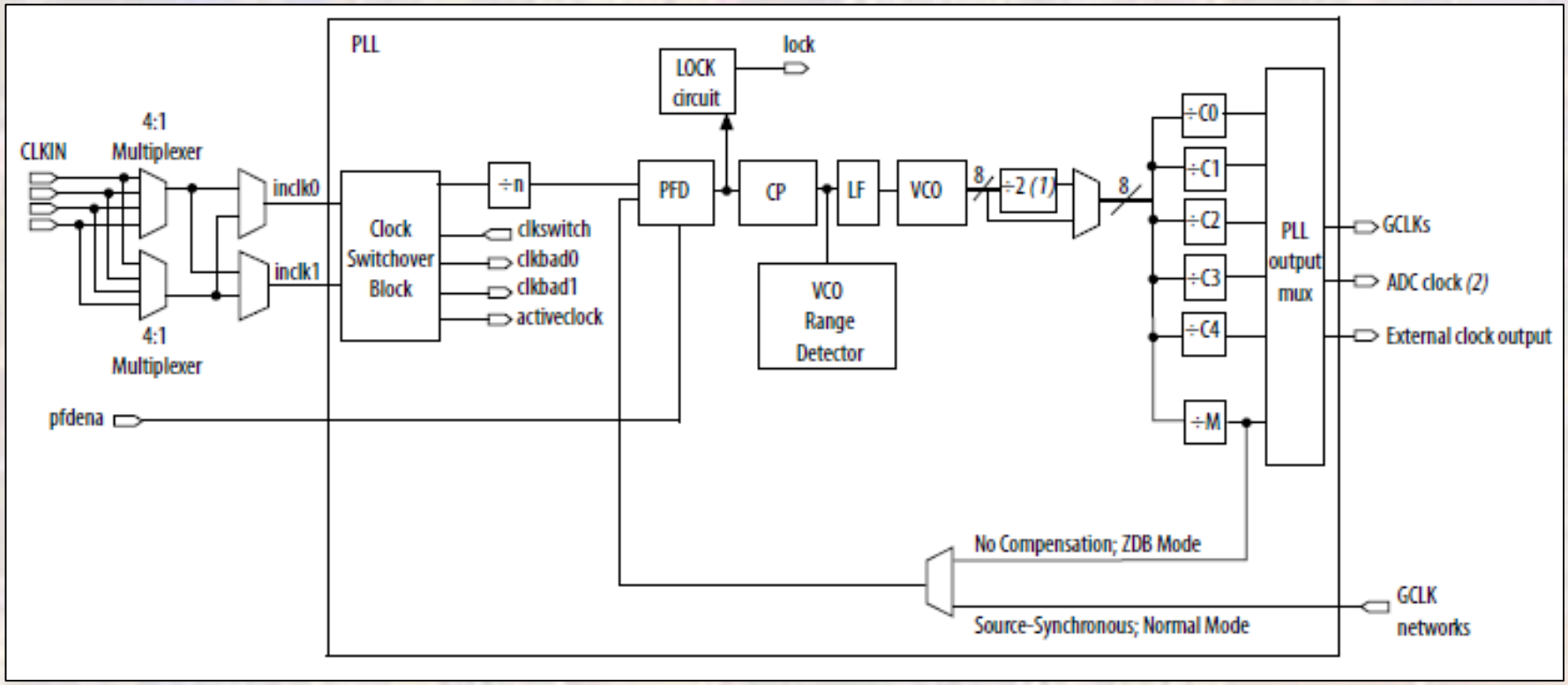
Figure 17: GCLK Network Sources for 10M16, 10M25, 10M40, and 10M50 Devices



Src: MAX 10 Device Handbook

FPGA MAX10

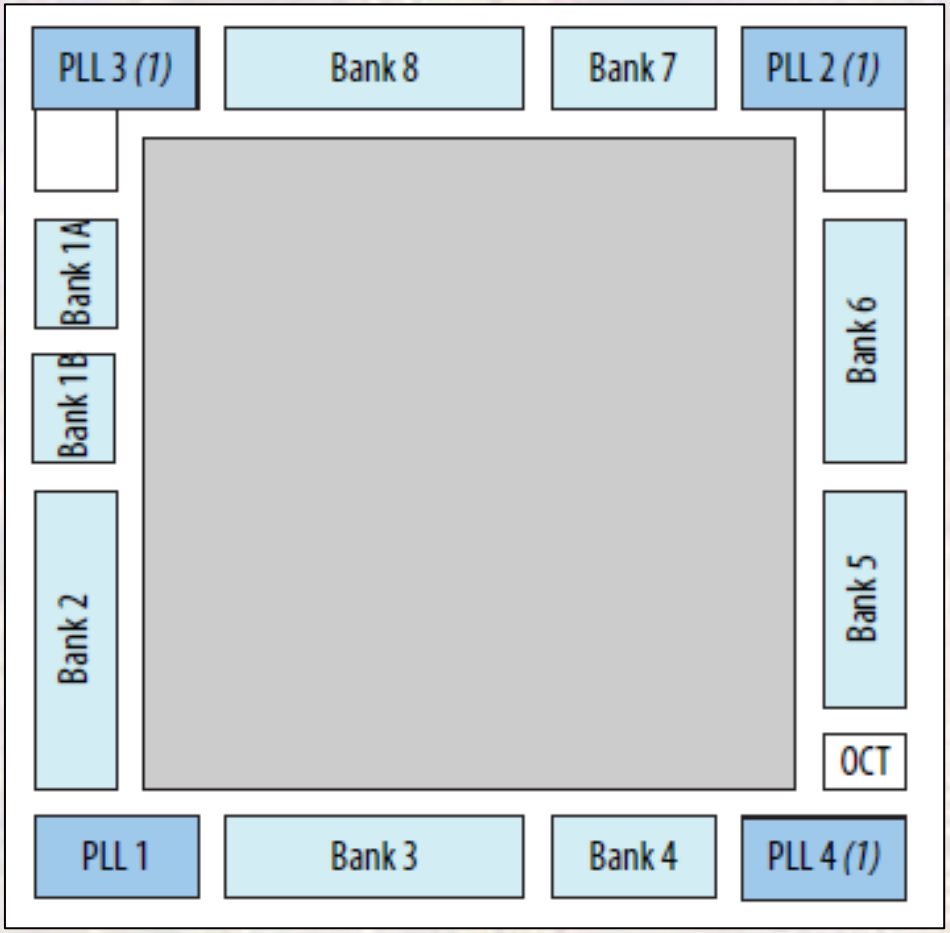
- Additional Fixed Blocks – Clocks
  - PLL



Src: MAX 10 Device Handbook

FPGA MAX10

- Additional Fixed Blocks - Clocks
  - PLL locations



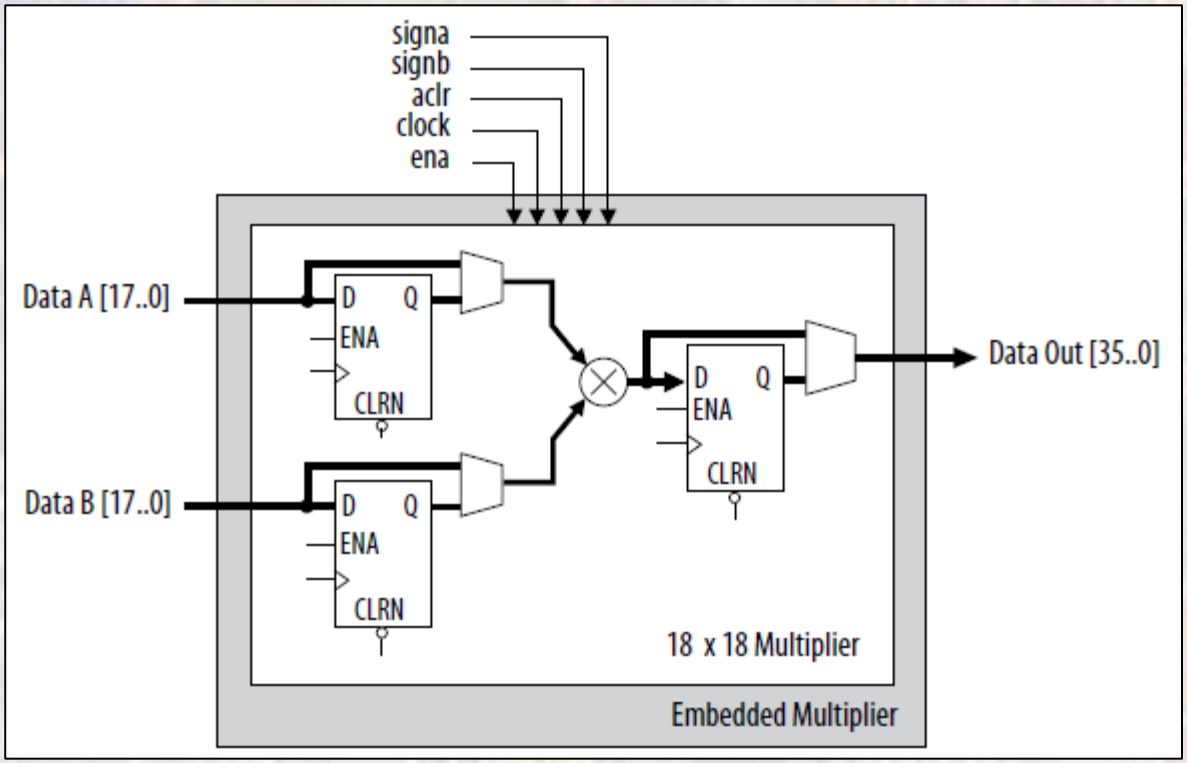
Src: MAX 10 Device Handbook

FPGA MAX10

- Additional Fixed Blocks - Memory
  - M9K Block
    - 8192 RAM bits (9216 including parity)
    - 284-MHz performance
    - True dual-port memory
    - Simple dual-port memory
    - Single-port memory
    - Byte enable
    - Parity bits
    - Shift register
    - FIFO buffer
    - ROM
    - Various clock modes
    - Address clock enable

FPGA MAX10

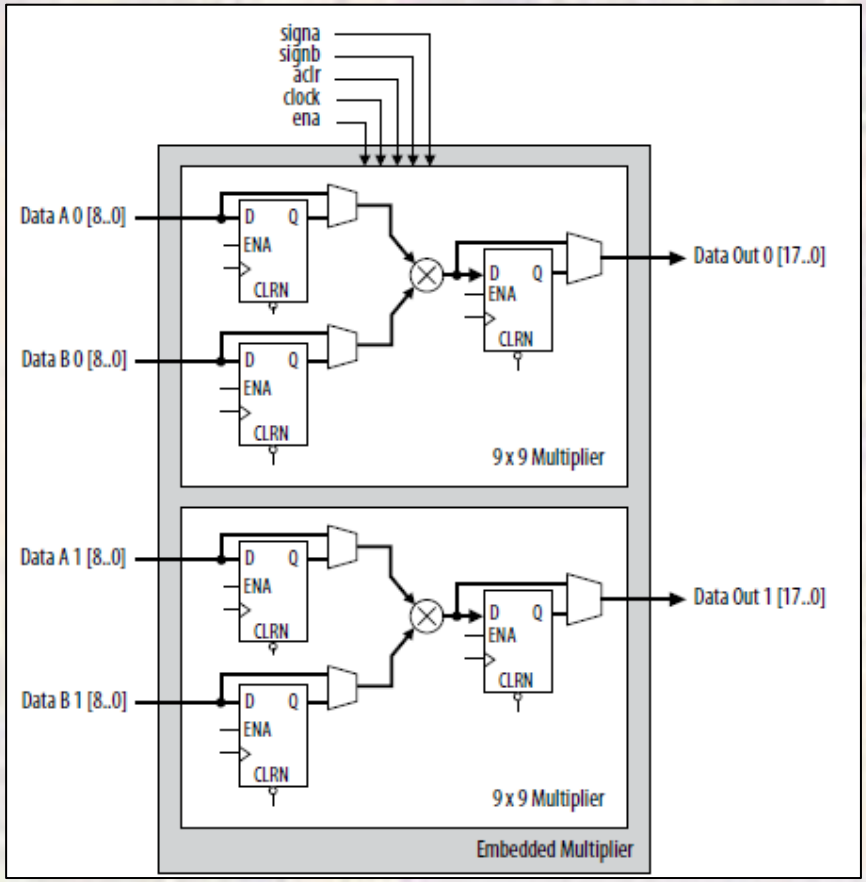
- Additional Fixed Blocks - Multiplier
  - 144 - 18 x 18 multipliers
  - Can be configured as 2 – 9 x 9 multipliers



Src: MAX 10 Device Handbook

FPGA MAX10

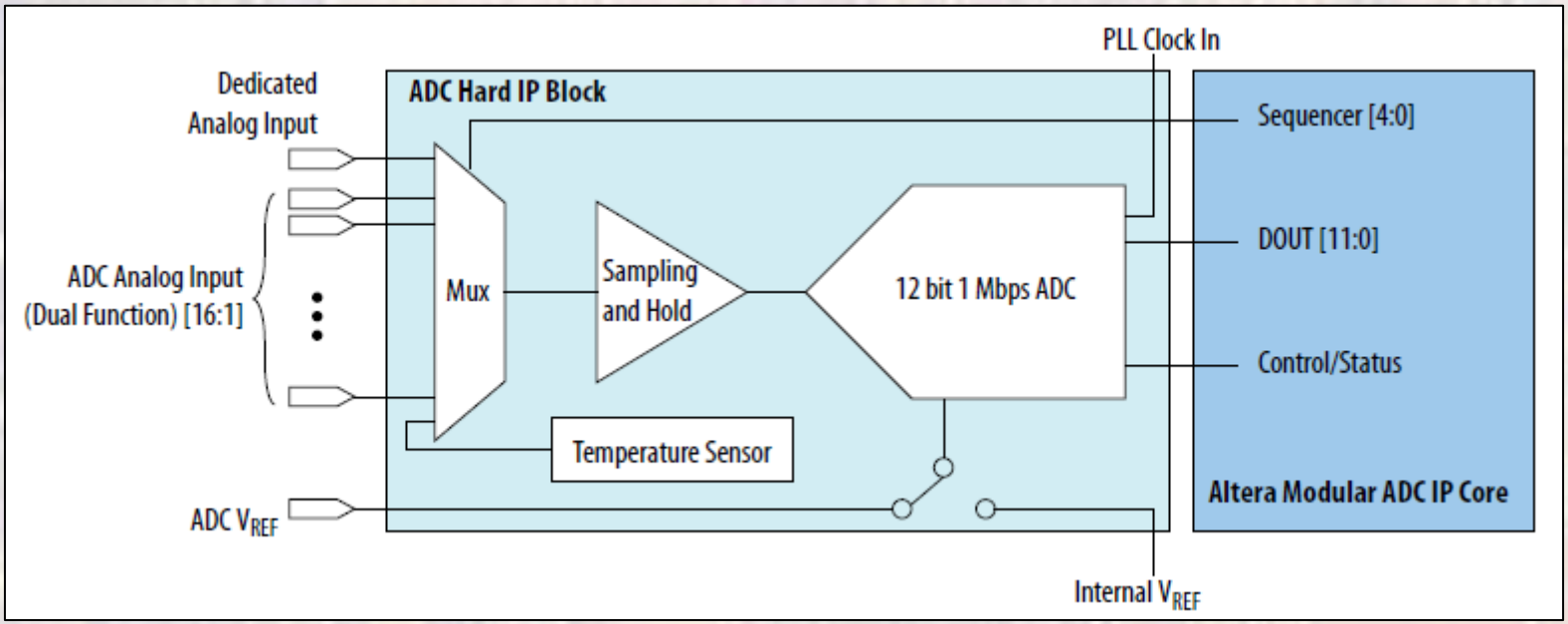
- Additional Fixed Blocks - Multiplier
  - Configured as 2 – 9 x 9 multipliers



Src: MAX 10 Device Handbook

FPGA MAX10

- Additional Fixed Blocks - ADC
  - 12 bit
  - 1Mbps



Src: MAX 10 Device Handbook

FPGA MAX10

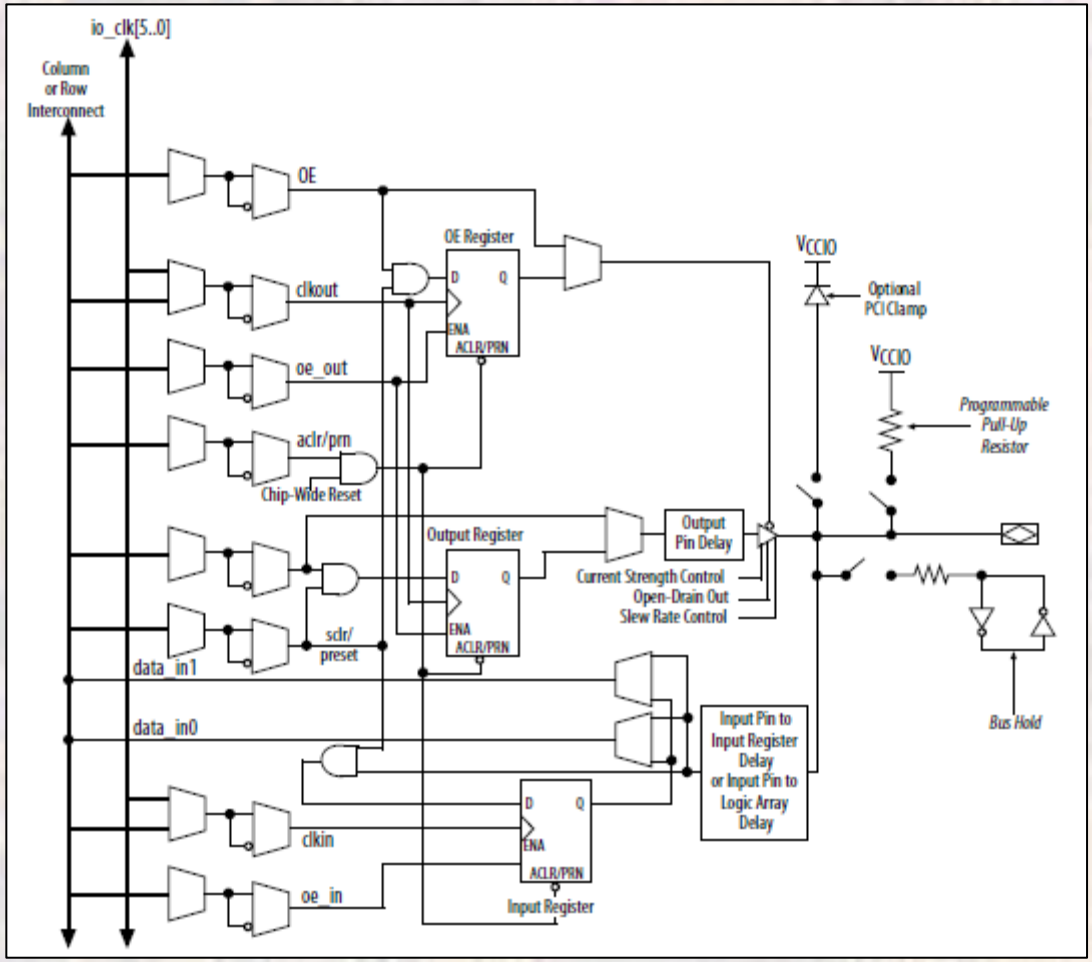
- Additional Fixed Blocks - User Flash
  - 2 user partitions
  - 5888Kb total memory

Device	Pages per Sector					Page Size (Kb)	Total User Flash Memory Size (Kb)	Total Configuration Memory Size (Kb)
	UFM1	UFM0	CFM2	CFM1	CFM0			
10M02	3	3	0	0	34	16	96	544
10M04	0	8	41	29	70	16	1248	2240
10M08	8	8	41	29	70	16	1376	2240
10M16	4	4	38	28	66	32	2368	4224
10M25	4	4	52	40	92	32	3200	5888
10M40	4	4	48	36	84	64	5888	10752
10M50	4	4	48	36	84	64	5888	10752

Src: MAX 10 Device Handbook

FPGA MAX10

- Additional Fixed Blocks - IO



Src: MAX 10 Device Handbook

FPGA MAX10

- A IO

I/O Standard	Type	Direction		Application	Standard Support
		Input	Output		
3.3 V LVTTL/3.3 V LVCMOS	Single-ended	Yes	Yes	General purpose	JESD8-B
3.0 V LVTTL/3.0 V LVCMOS	Single-ended	Yes	Yes	General purpose	JESD8-B
2.5 V LVCMOS	Single-ended	Yes	Yes	General purpose	JESD8-5
1.8 V LVCMOS	Single-ended	Yes	Yes	General purpose	JESD8-7
1.5 V LVCMOS	Single-ended	Yes	Yes	General purpose	JESD8-11
1.2 V LVCMOS	Single-ended	Yes	Yes	General purpose	JESD8-12
3.0 V PCI	Single-ended	Yes	Yes	General purpose	PCI Rev. 2.2
3.3 V Schmitt Trigger	Single-ended	Yes	—	General purpose	—
2.5 V Schmitt Trigger	Single-ended	Yes	—	General purpose	—
1.8 V Schmitt Trigger	Single-ended	Yes	—	General purpose	—
1.5 V Schmitt Trigger	Single-ended	Yes	—	General purpose	—
SSTL-2 Class I	Voltage-referenced	Yes	Yes	DDR1	JESD8-9B
SSTL-2 Class II	Voltage-referenced	Yes	Yes	DDR1	JESD8-9B
SSTL-18 Class I	Voltage-referenced	Yes	Yes	DDR2	JESD8-15
SSTL-18 Class II	Voltage-referenced	Yes	Yes	DDR2	JESD8-15
SSTL-15 Class I	Voltage-referenced	Yes	Yes	DDR3	—
SSTL-15 Class II	Voltage-referenced	Yes	Yes	DDR3	—
SSTL-15[1]	Voltage-referenced	Yes	Yes	DDR3	JESD79-3D
SSTL-135[1]	Voltage-referenced	Yes	Yes	DDR3L	—
1.8 V HSTL Class I	Voltage-referenced	Yes	Yes	DDR II+, QDR II+, and RLDRAM 2	JESD8-6
1.8 V HSTL Class II	Voltage-referenced	Yes	Yes	DDR II+, QDR II+, and RLDRAM 2	JESD8-6
1.5 V HSTL Class I	Voltage-referenced	Yes	Yes	DDR II+, QDR II+, QDR II, and RLDRAM 2	JESD8-6
1.5 V HSTL Class II	Voltage-referenced	Yes	Yes	DDR II+, QDR II+, QDR II, and RLDRAM 2	JESD8-6
1.2 V HSTL Class I	Voltage-referenced	Yes	Yes	General purpose	JESD8-16A
1.2 V HSTL Class II	Voltage-referenced	Yes	Yes	General purpose	JESD8-16A
HSUL-12[1]	Voltage-referenced	Yes	Yes	LPDDR2	—
Differential SSTL-2 Class I and II	Differential	Yes[2]	Yes[3]	DDR1	JESD8-9B
Differential SSTL-18 Class I and Class II	Differential	Yes[2]	Yes[3]	DDR2	JESD8-15
Differential SSTL-15 Class I and Class II	Differential	Yes[2]	Yes[3]	DDR3	—
Differential SSTL-15	Differential	Yes[2]	Yes[3]	DDR3	JESD79-3D
Differential SSTL-135	Differential	Yes[2]	Yes[3]	DDR3L	—
Differential 1.8 V HSTL Class I and Class II	Differential	Yes[2]	Yes[3]	DDR II+, QDR II+, and RLDRAM 2	JESD8-6
Differential 1.5 V HSTL Class I and Class II	Differential	Yes[2]	Yes[3]	DDR II+, QDR II+, QDR II, and RLDRAM 2	JESD8-6
Differential 1.2 V HSTL Class I and Class II	Differential	Yes[2]	Yes[3]	General purpose	JESD8-16A
Differential HSUL-12	Differential	Yes[2]	Yes[3]	LPDDR2	—
LVDS (dedicated)[4]	Differential	Yes	Yes[5]	—	ANSI/TIA/EIA-644
LVDS (external resistor)	Differential	—	Yes	—	ANSI/TIA/EIA-644
Mini-LVDS (dedicated)[4]	Differential	—	Yes[5]	—	—
Mini-LVDS (external resistor)	Differential	—	Yes	—	—
RSDS (dedicated)[4]	Differential	—	Yes[5]	—	—
RSDS (external resistor, 1R)	Differential	—	Yes	—	—
RSDS (external resistor, 3R)	Differential	—	Yes	—	—
PPDS (dedicated)[4]	Differential	—	Yes[5]	—	—
PPDS (external resistor)	Differential	—	Yes	—	—
LVPECL	Differential	Yes	—	—	—
Bus LVDS	Differential	Yes	Yes[6]	—	—
TMDS	Differential	Yes	—	—	—
Sub-LVDS	Differential	Yes	Yes[7]	—	—
SLVS	Differential	Yes	Yes[8]	—	—
HiSpi	Differential	Yes	—	—	—

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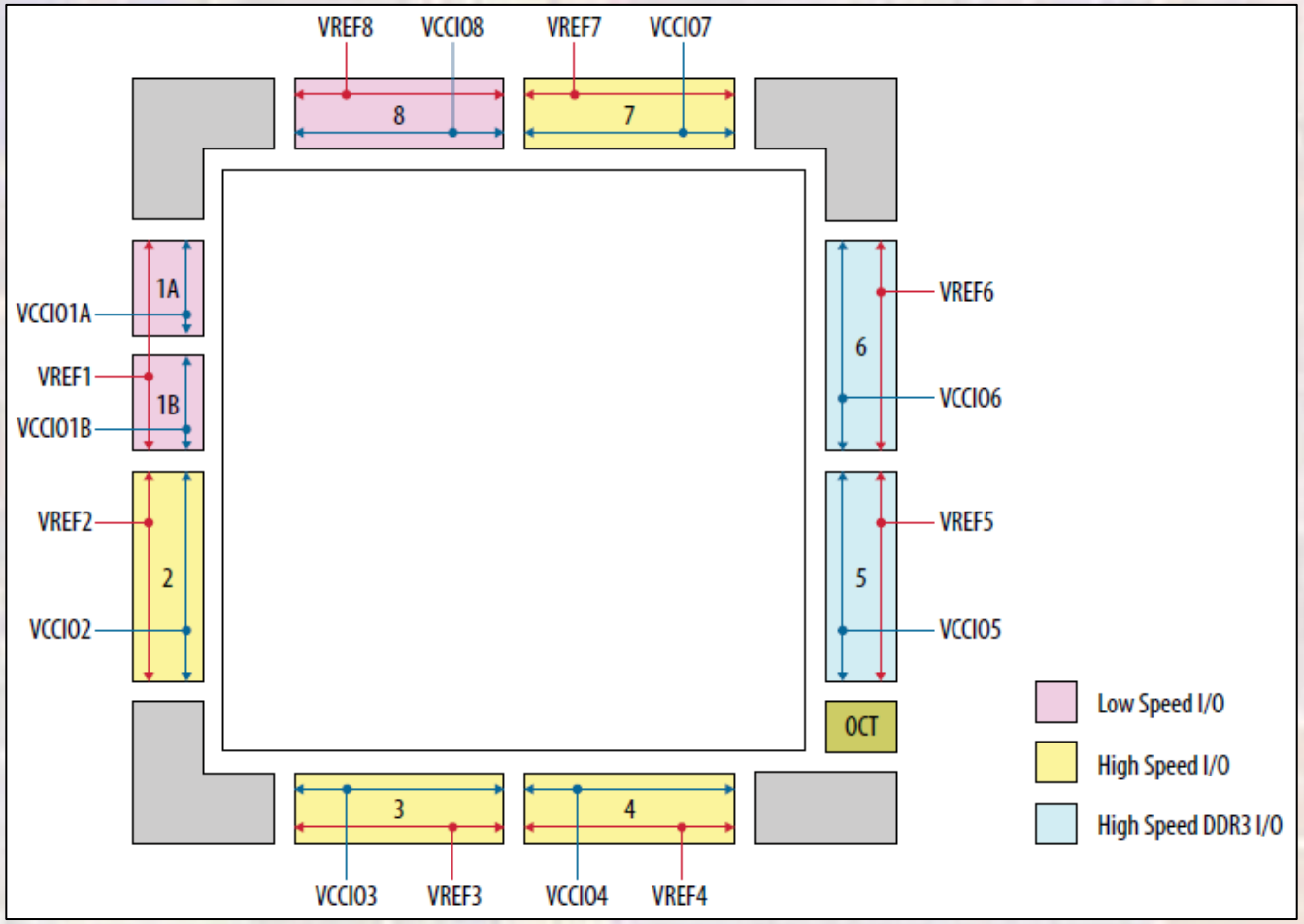
FPGA MAX10

- Additional Fixed Blocks - IO



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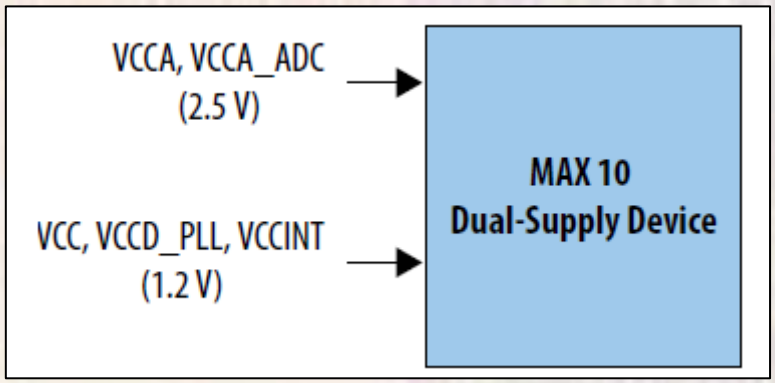
FPGA MAX10

- Dual Power Supply

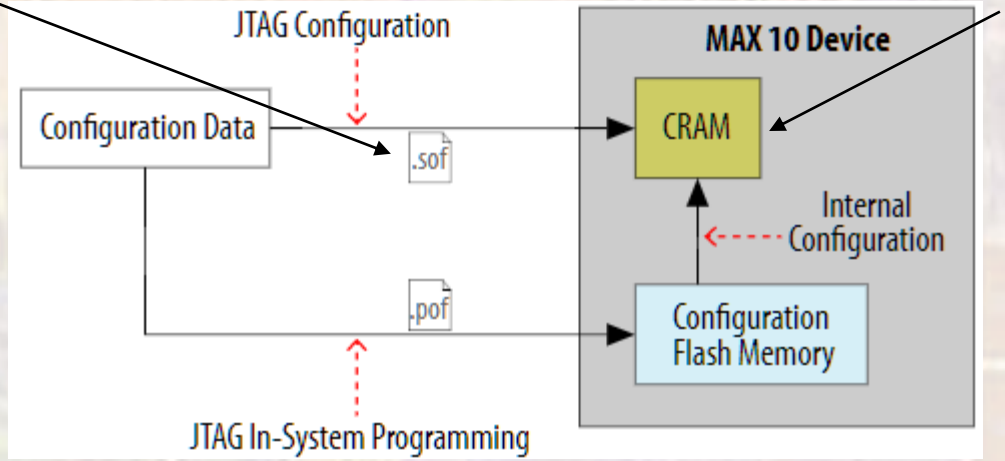


Src: MAX 10 Device Handbook

FPGA Basics

- FPGA – programmable
  - JTAG Programming Configurations
    - On power-up, the contents of the Configuration Flash Memory (default program) are loaded into the Configuration RAM
      - Flashing lights and numbers we see on power up
    - Load programming information (xx.sof file) directly into the Configuration RAM via the JTAG interface (Programmer)
      - Our configuration is loaded

xx.sof file
SRAM Object File



Configuration RAM