

MAX 10 Memory Configurations

Last updated 7/19/23

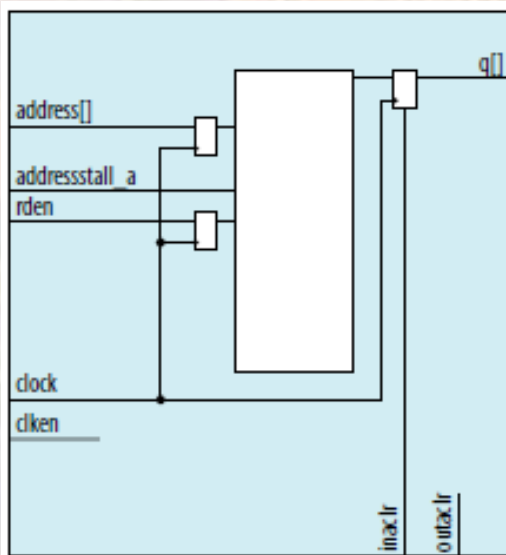
MAX10 Memory - Configurations

- Functional configurations
 - Single-port
 - Simple dual-port
 - True dual-port (bidirectional dual-port)
 - Shift register
 - ROM
 - FIFO buffers
 - Memory Based Multiplier
- Available via the Mega-Wizard tool

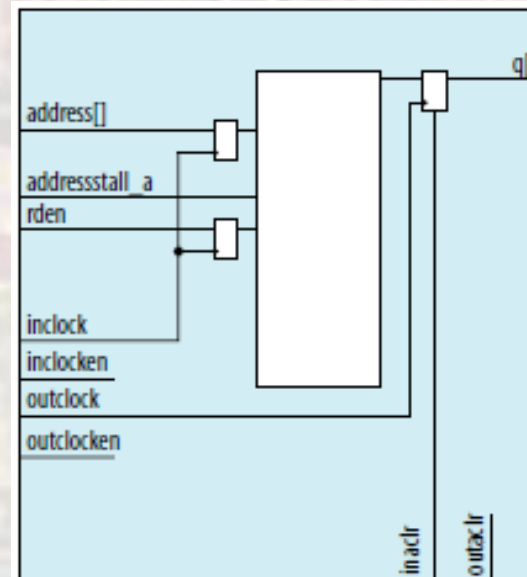
MAX10 Memory - Configurations

- M9K Fixed Memory Blocks
 - ROM – Single Port
 - SRAM with memory pre-loaded from a MIF file
 - Single Port
 - Read only

Single Clock



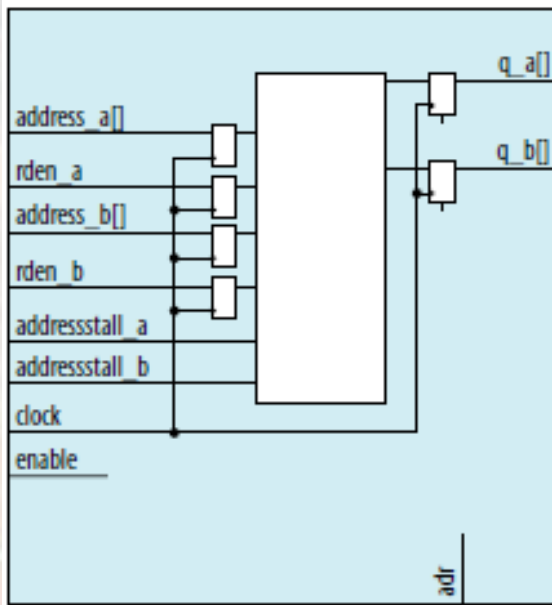
In/Out Clock



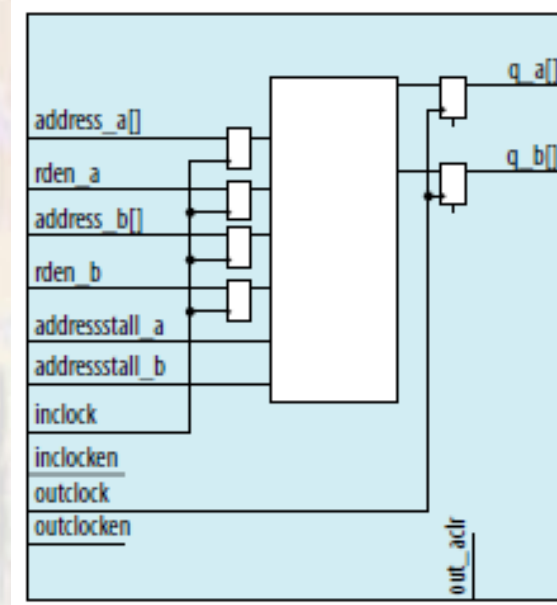
MAX10 Memory - Configurations

- M9K Fixed Memory Blocks
 - ROM – Dual Port
 - SRAM with memory pre-loaded from a MIF file
 - Dual Port
 - Read only

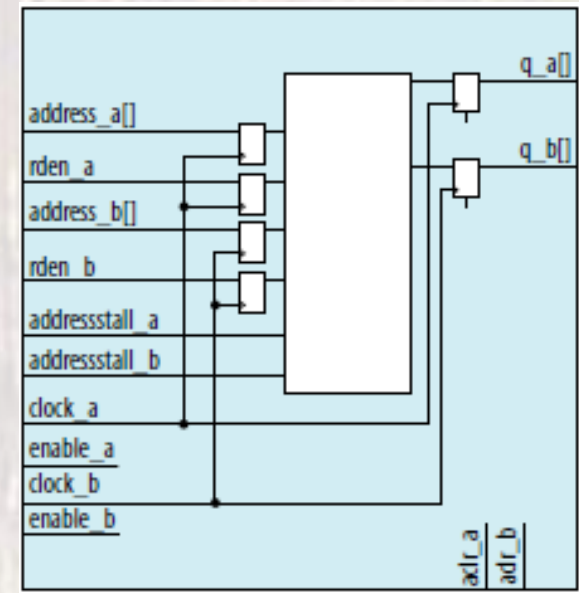
Single Clock



In/Out Clock



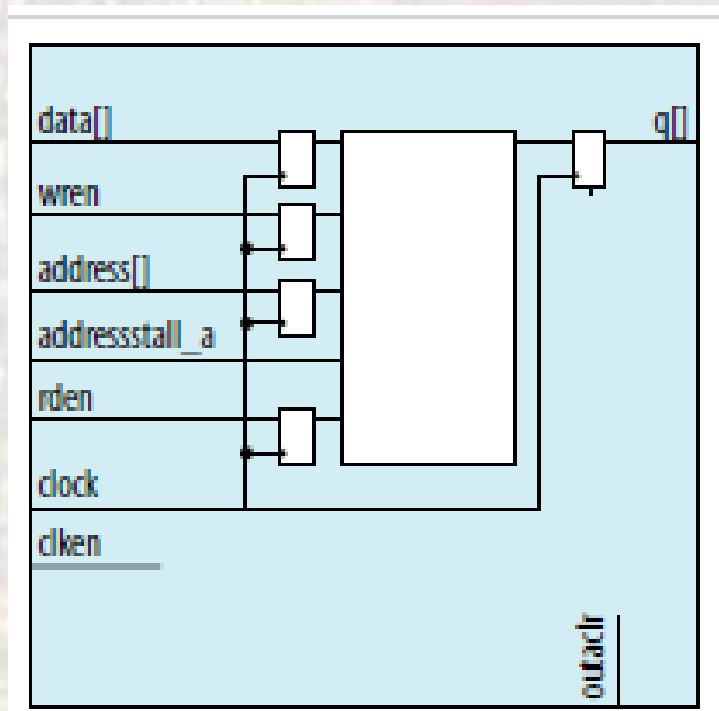
A/B Clock



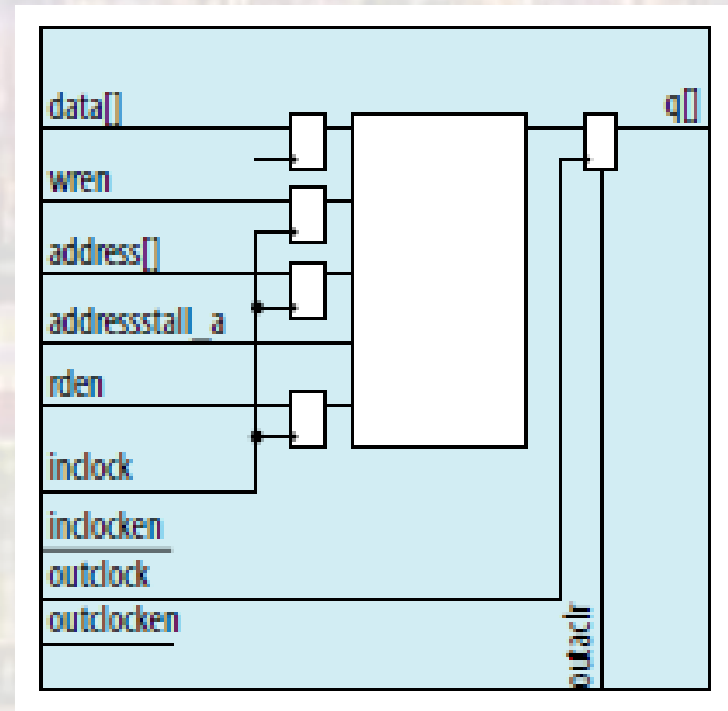
MAX10 Memory - Configurations

- M9K Fixed Memory Blocks
 - Single Port RAM

Single Clock



Dual Clock

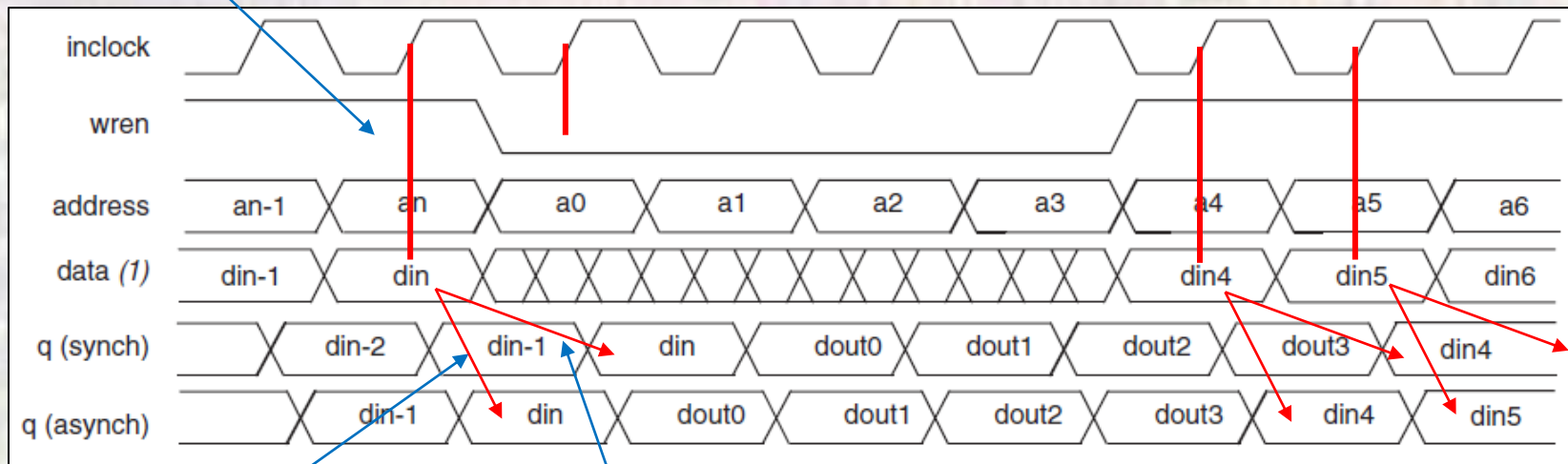


Src: MAX 10 Device Handbook

MAX10 Memory - Configurations

- M9K Fixed Memory Blocks
 - Single Port RAM - write

Write addr captured



Src: Cyclone II Device Handbook

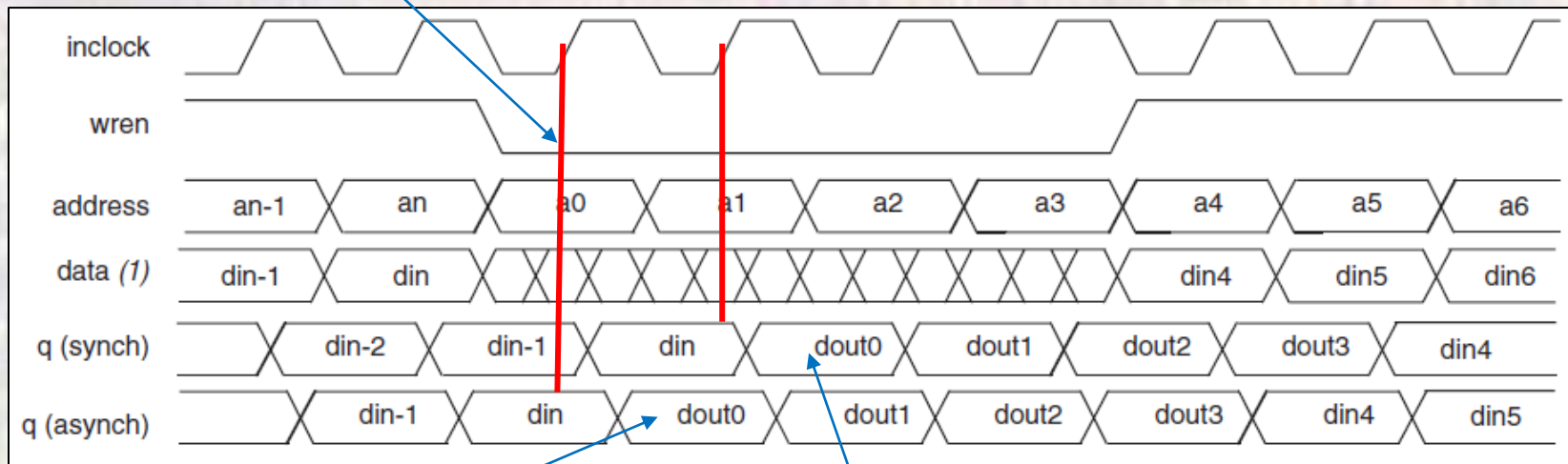
Async data flow through with delay

Sync data flow through with 1 clk + td delay

MAX10 Memory - Configurations

- M9K Fixed Memory Blocks
 - Single Port RAM - read

Read addr captured



Src: Cyclone II Device Handbook

Async read
with delay

Sync data read
with 1 clk + td delay

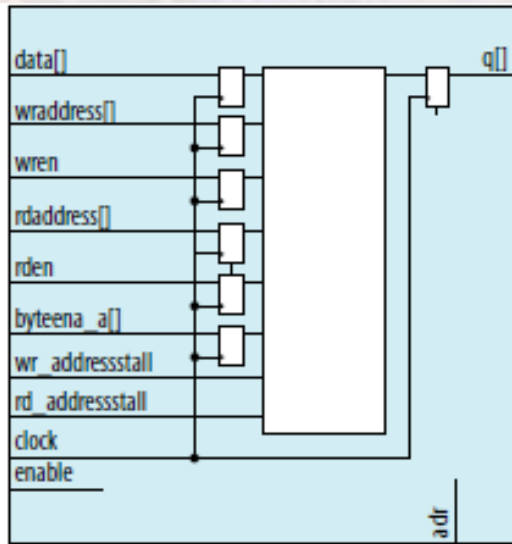
MAX10 Memory - Configurations

- M9K Fixed Memory Blocks
 - Simple Dual Port RAM
 - Separate read and write addresses
 - Simultaneous read and write
 - Data in and out ports do not have to have matching widths

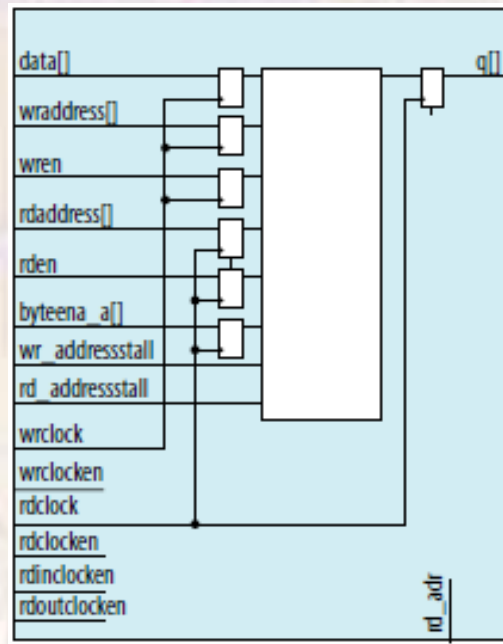
MAX10 Memory - Configurations

- M9K Fixed Memory Blocks
 - Simple Dual Port RAM

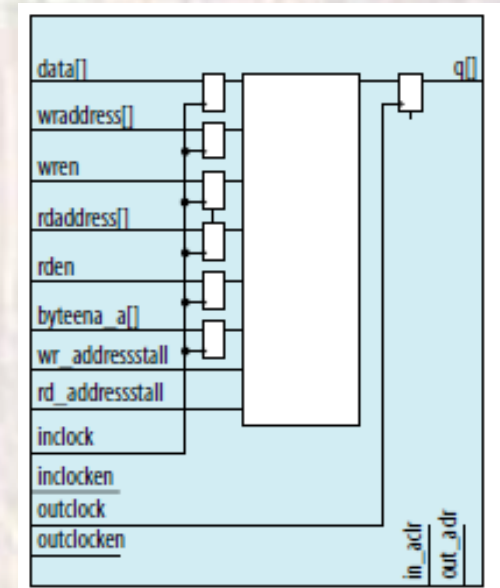
Single Clock



R/W Clock

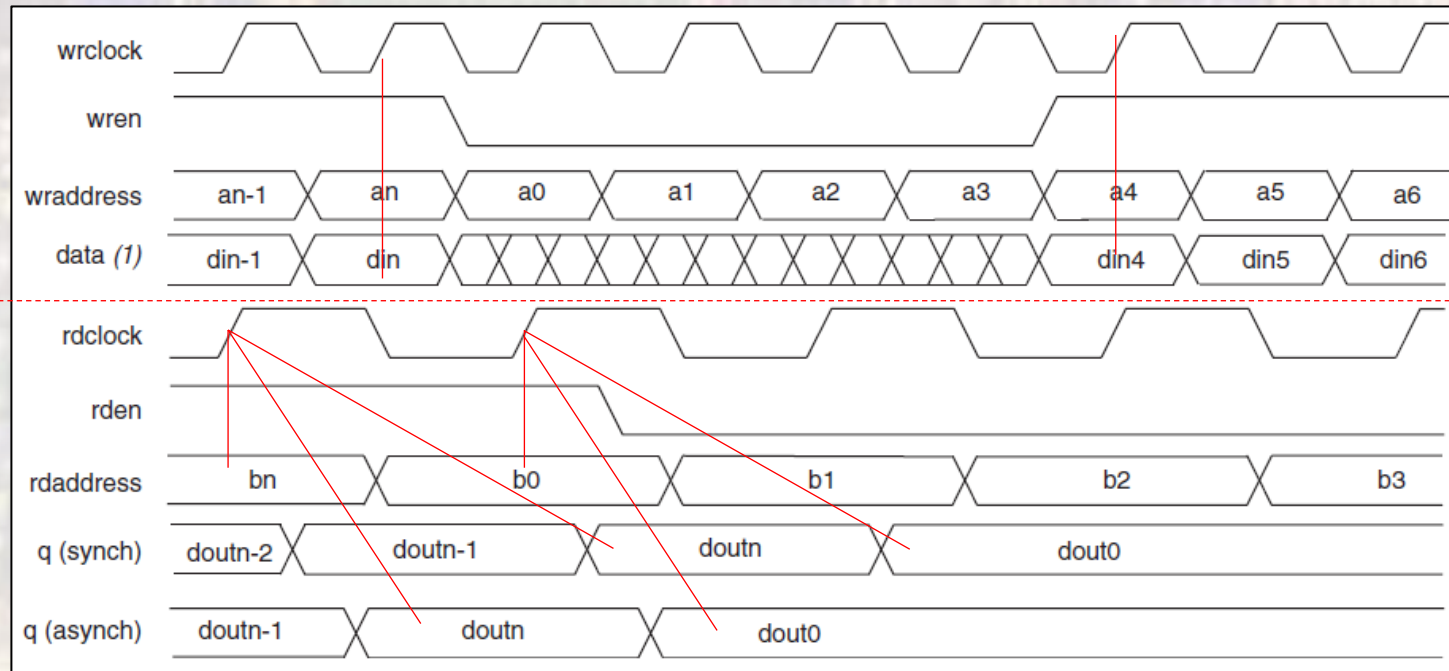


In/Out Clock



MAX10 Memory - Configurations

- M9K Fixed Memory Blocks
 - Simple Dual Port RAM



Src: Cyclone II Device Handbook

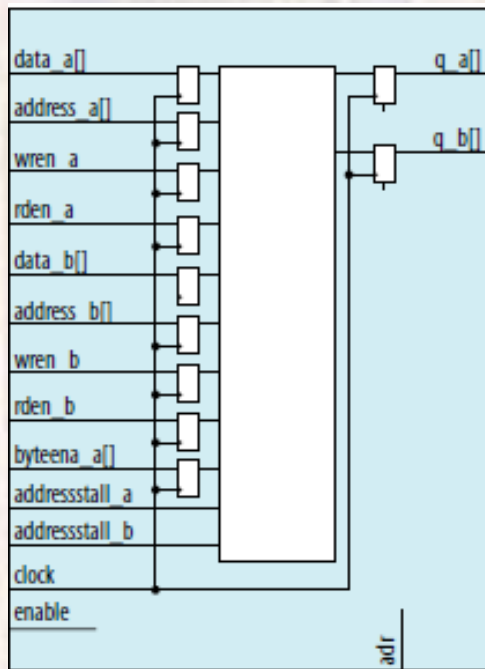
MAX10 Memory - Configurations

- M9K Fixed Memory Blocks
 - True Dual Port RAM
 - Supports 2 reads, 2 writes, Read/Write
 - Multiple clock options
 - Data in and out ports do not have to have matching widths

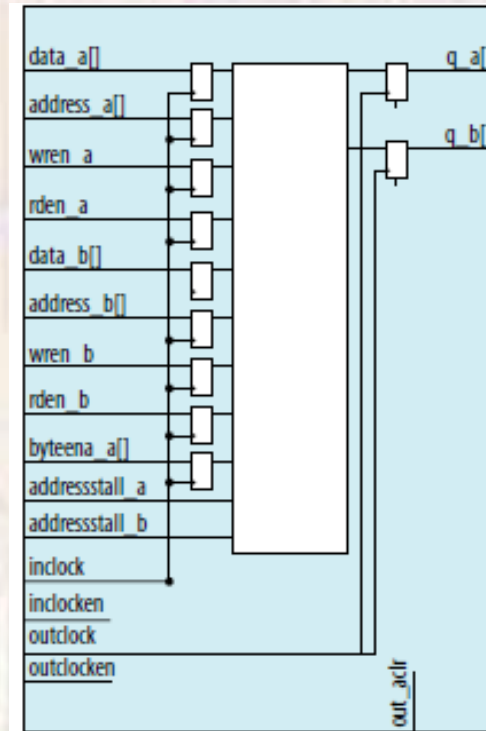
MAX10 Memory - Configurations

- M9K Fixed Memory Blocks
 - True Dual Port RAM
 - Multiple R/W Ports

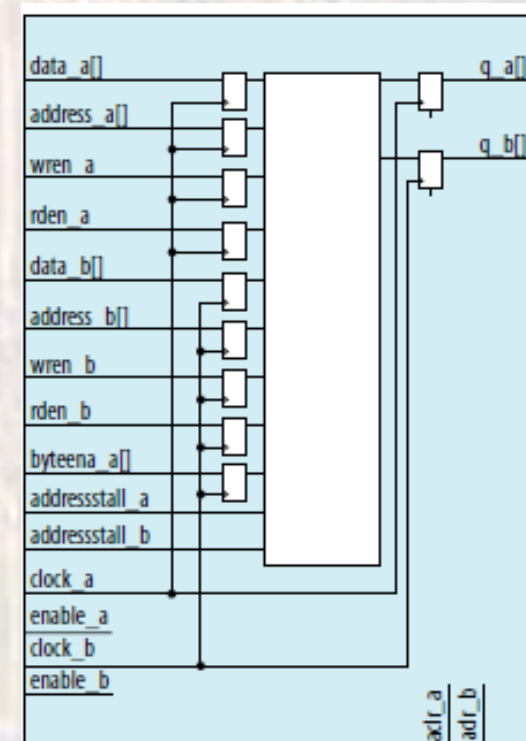
Single Clock



R/W Clock

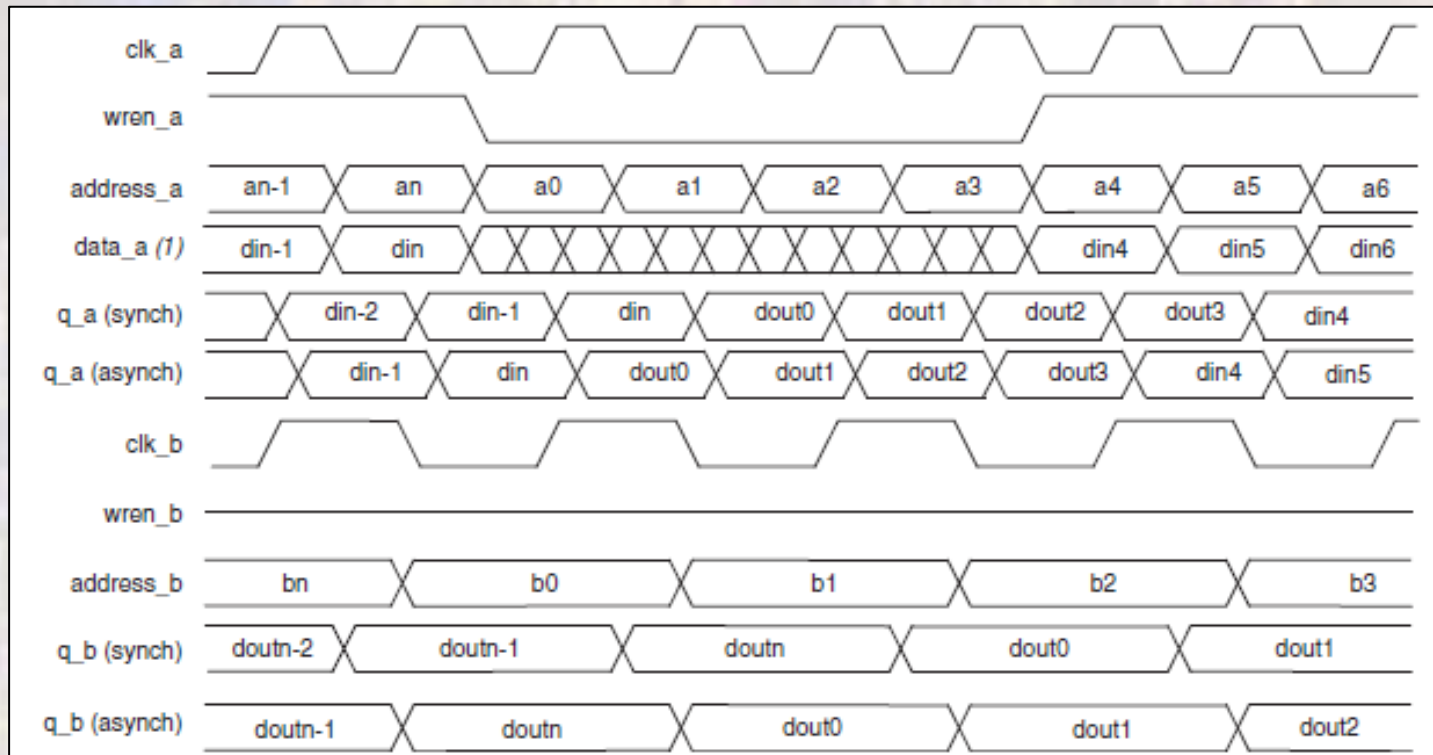


A/B Clock



MAX10 Memory - Configurations

- M9K Fixed Memory Blocks
 - True Dual Port RAM



Src: Cyclone II Device Handbook

MAX10 Memory - Configurations

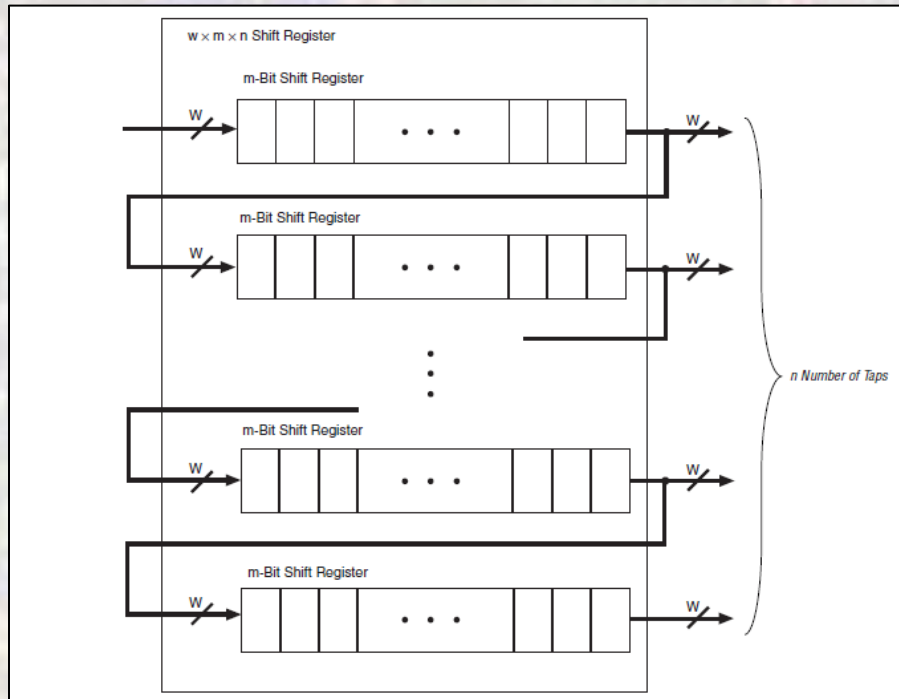
- M9K Fixed Memory Blocks
- Mixed Port Configurations

M9K Block Mixed-Width Configurations (Simple Dual-Port RAM)									
Read Port	Write Port								
	8192 × 1	4096 × 2	2048 × 4	1024 × 8	512 × 16	256 × 32	1024 × 9	512 × 18	256 × 36
8192 × 1	Yes	Yes	Yes	Yes	Yes	Yes	—	—	—
4096 × 2	Yes	Yes	Yes	Yes	Yes	Yes	—	—	—
2048 × 4	Yes	Yes	Yes	Yes	Yes	Yes	—	—	—
1024 × 8	Yes	Yes	Yes	Yes	Yes	Yes	—	—	—
512 × 16	Yes	Yes	Yes	Yes	Yes	Yes	—	—	—
256 × 32	Yes	Yes	Yes	Yes	Yes	Yes	—	—	—
1024 × 9	—	—	—	—	—	—	Yes	Yes	Yes
512 × 18	—	—	—	—	—	—	Yes	Yes	Yes
256 × 36	—	—	—	—	—	—	Yes	Yes	Yes

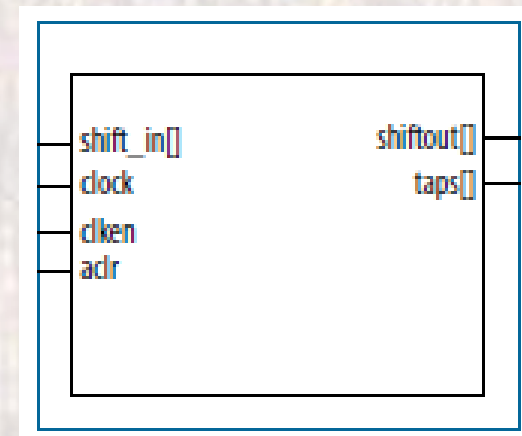
M9K Block Mixed-Width Configurations (True Dual-Port RAM Mode)							
Read Port	Write Port						
	8192 × 1	4096 × 2	2048 × 4	1024 × 8	512 × 16	1024 × 9	512 × 18
8192 × 1	Yes	Yes	Yes	Yes	Yes	—	—
4096 × 2	Yes	Yes	Yes	Yes	Yes	—	—
2048 × 4	Yes	Yes	Yes	Yes	Yes	—	—
1024 × 8	Yes	Yes	Yes	Yes	Yes	—	—
512 × 16	Yes	Yes	Yes	Yes	Yes	—	—
1024 × 9	—	—	—	—	—	Yes	Yes
512 × 18	—	—	—	—	—	Yes	Yes

MAX10 Memory - Configurations

- M9K Fixed Memory Blocks
 - Multi-tap Shift RAM
 - Multiple M9K blocks can be cascaded

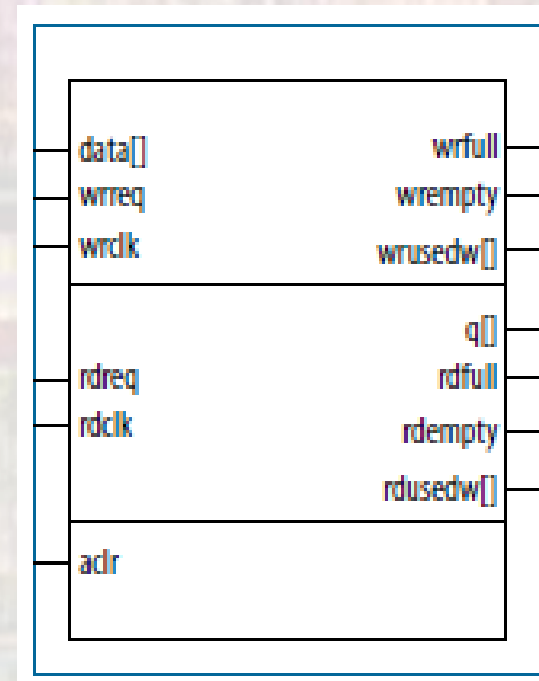
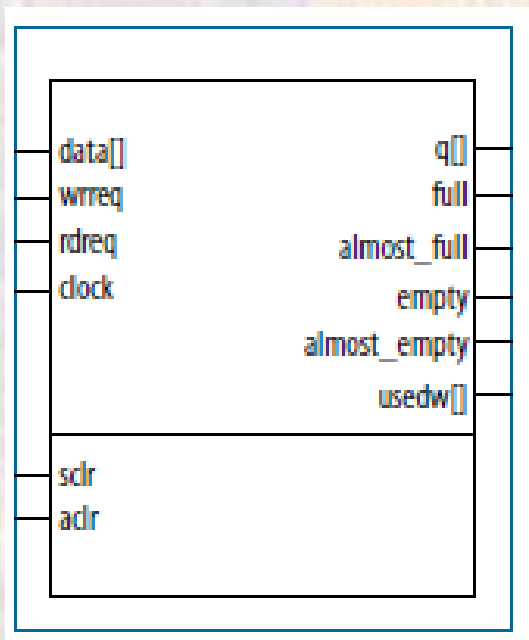


Src: Cyclone II Device Handbook



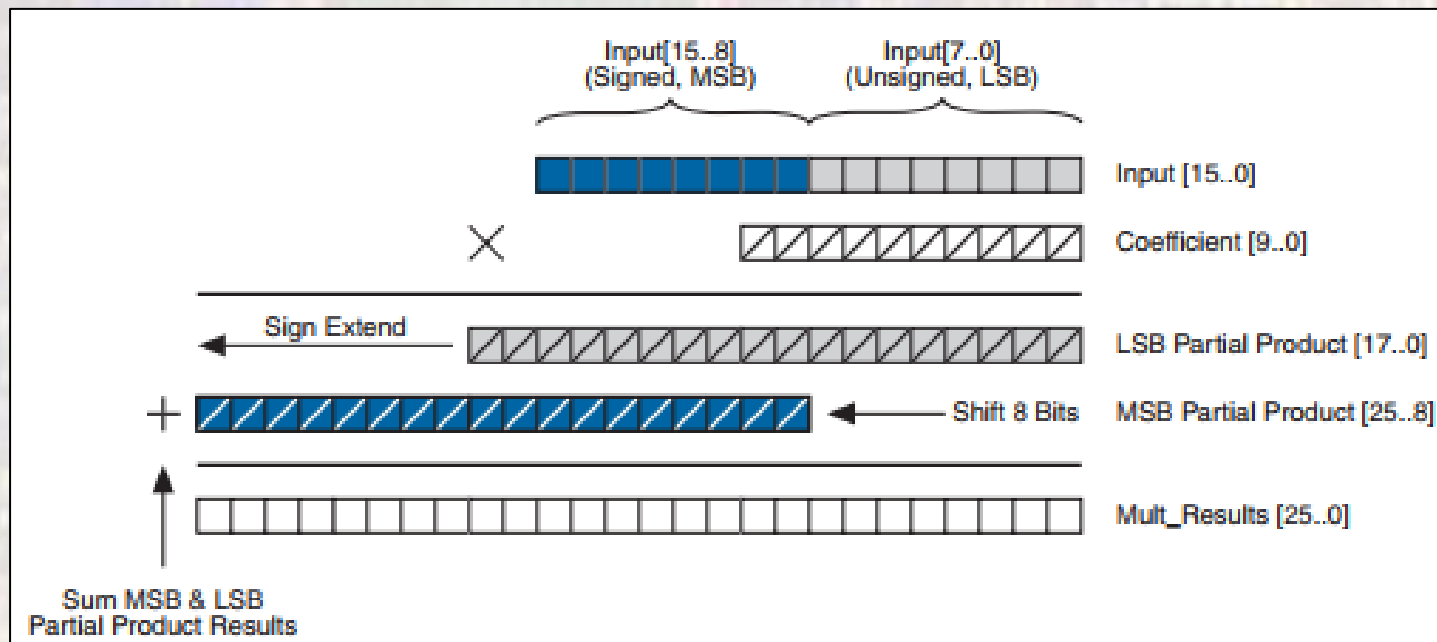
MAX10 Memory - Configurations

- M9K Fixed Memory Blocks
 - FIFO
 - Separate read and write clocks available
 - Separate read and write data widths available
 - Empty and Full signals



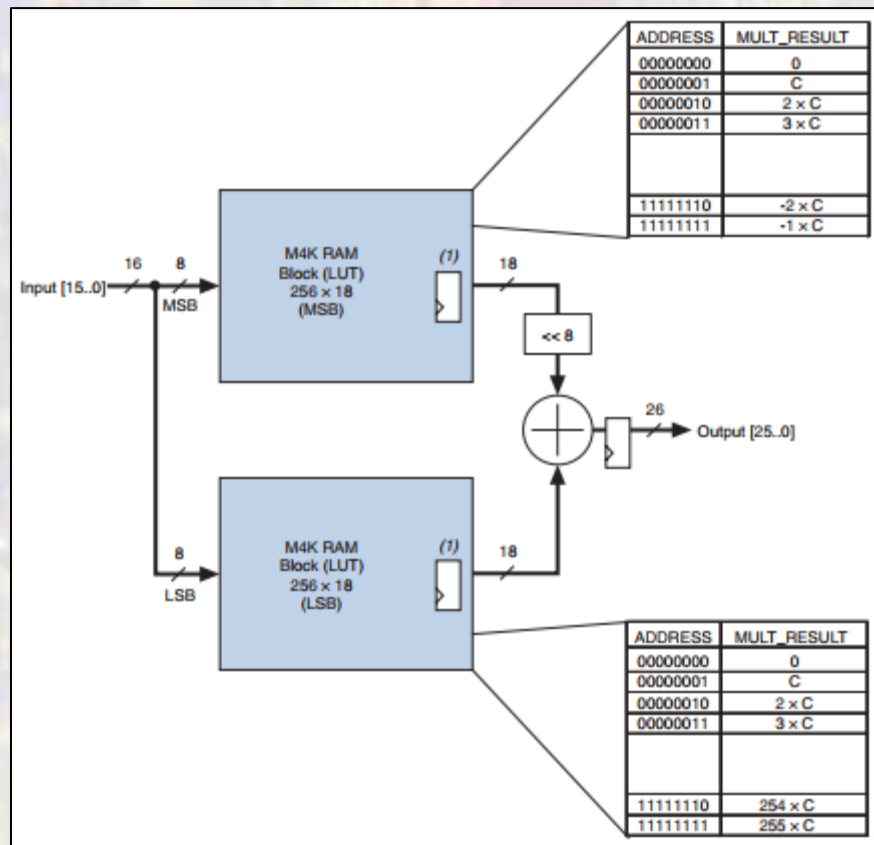
MAX10 Memory - Configurations

- M9K Fixed Memory Blocks
 - Memory Based Multiplier



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