MAX 10 Memory Operation

Last updated 7/19/23

MAX10 Memory - Operation

- M9K Fixed Memory Blocks
  - Functional configurations
    - Single-port
    - Simple dual-port
    - True dual-port (bidirectional dual-port)
    - Shift register
    - ROM
    - FIFO buffers
    - Memory Based Multiplier

MAX10 Memory - Operation

- M9K Fixed Memory Blocks
  - Data width (word) configurations

Feature	M9K Block
Configurations (depth × width)	8192 × 1
	4096 × 2
	2048 × 4
	1024 × 8
	1024 × 9
	512 × 16
	512 × 18
	256 × 32
	256 × 36

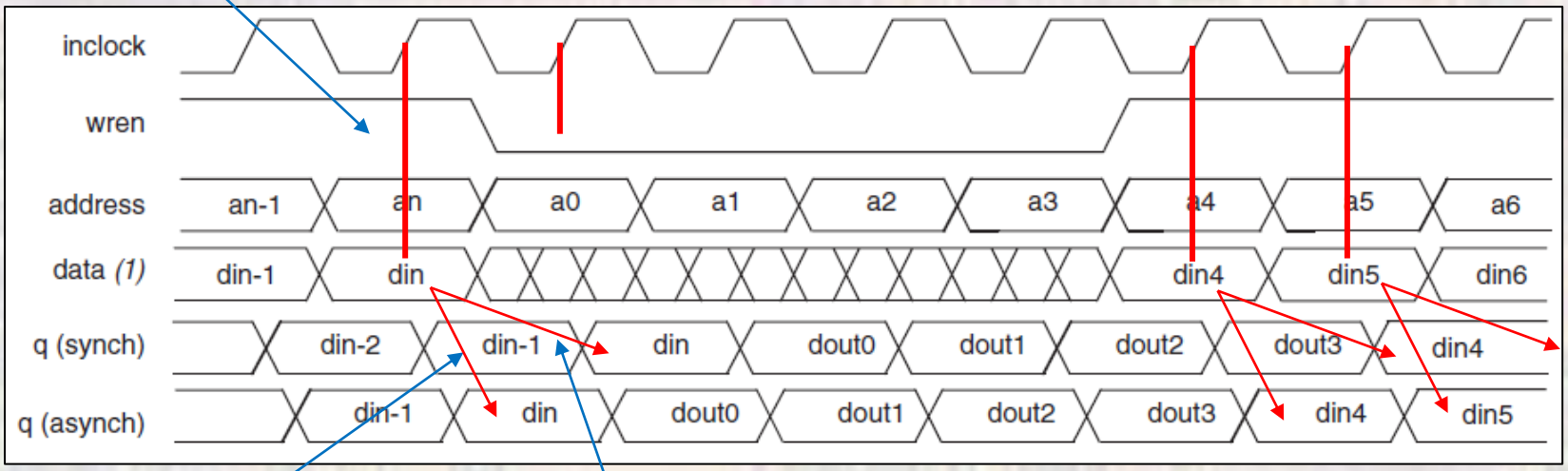
Parity used as memory

  - Packed Mode
    - Single Port configuration
    - Each M9K block can be broken into 2 independent memories
    - Each memory must be less than ½ the full block size
    - 18 bit word size maximum ??
    - Each memory has only single clock support

MAX10 Memory - Operation

- M9K Fixed Memory Blocks
  - Single Port RAM - write

Write addr captured



Src: Cyclone II Device Handbook

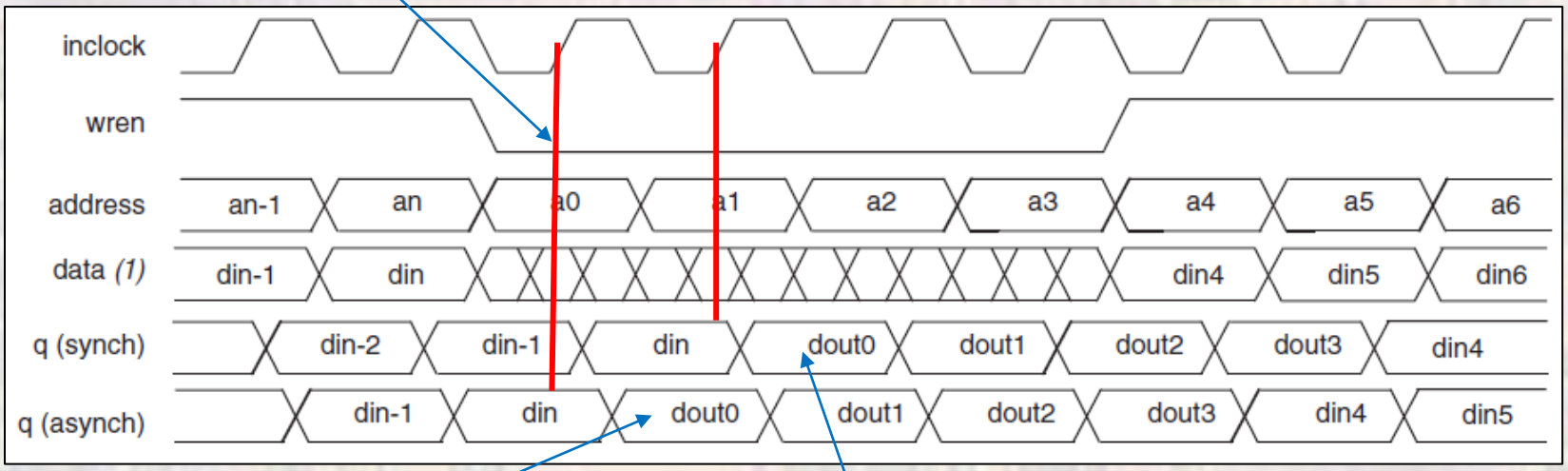
Async data flow through with delay

Sync data flow through with 1 clk + td delay

MAX10 Memory - Operation

- M9K Fixed Memory Blocks
  - Single Port RAM - read

Read addr captured



Src: Cyclone II Device Handbook

Async read with delay

Sync data read with 1 clk + td delay

MAX10 Memory - Operation

- M9K Fixed Memory Blocks
  - Byte Enable
    - SRAM only
    - Multi-byte words can be masked

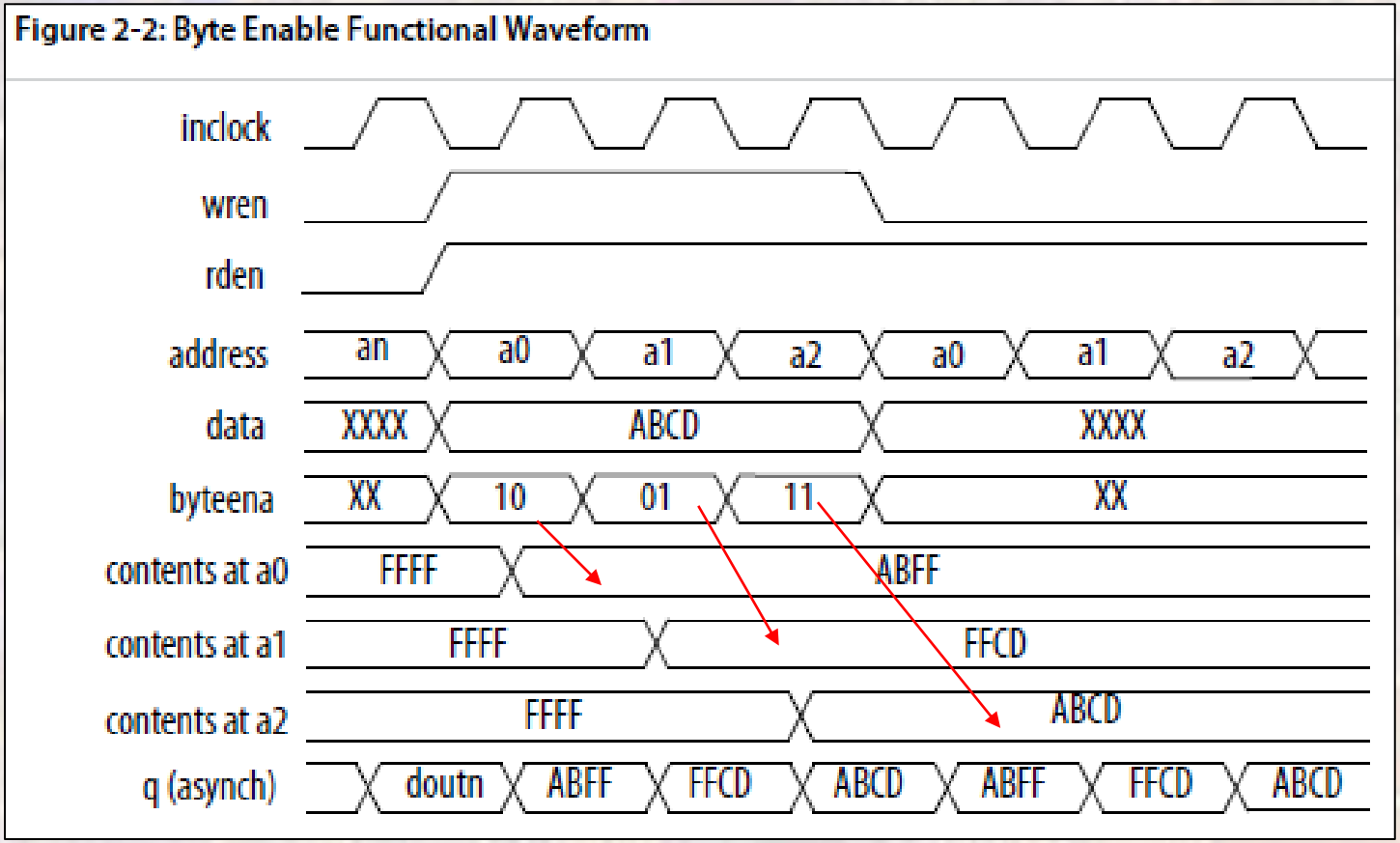
Table 2-1: M9K Blocks Byte Enable Selections

byteena[3:0]	Affected Bytes. Any Combination of Byte Enables is Possible.			
	datain x 16	datain x 18	datain x 32	datain x 36
[0] = 1	[7:0]	[8:0]	[7:0]	[8:0]
[1] = 1	[15:8]	[17:9]	[15:8]	[17:9]
[2] = 1	—	—	[23:16]	[26:18]
[3] = 1	—	—	[31:24]	[35:27]

Src: MAX 10 Device Handbook

MAX10 Memory - Operation

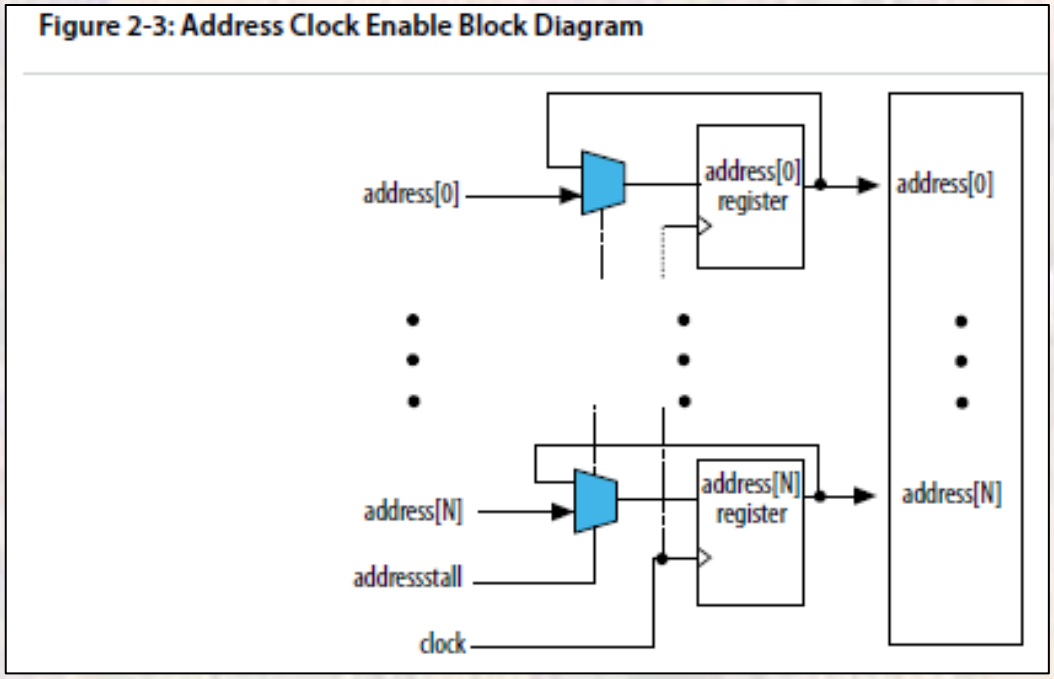
- M9K Fixed Memory Blocks
  - Byte Enable – 16b example



Src: MAX 10 Device Handbook

MAX10 Memory - Operation

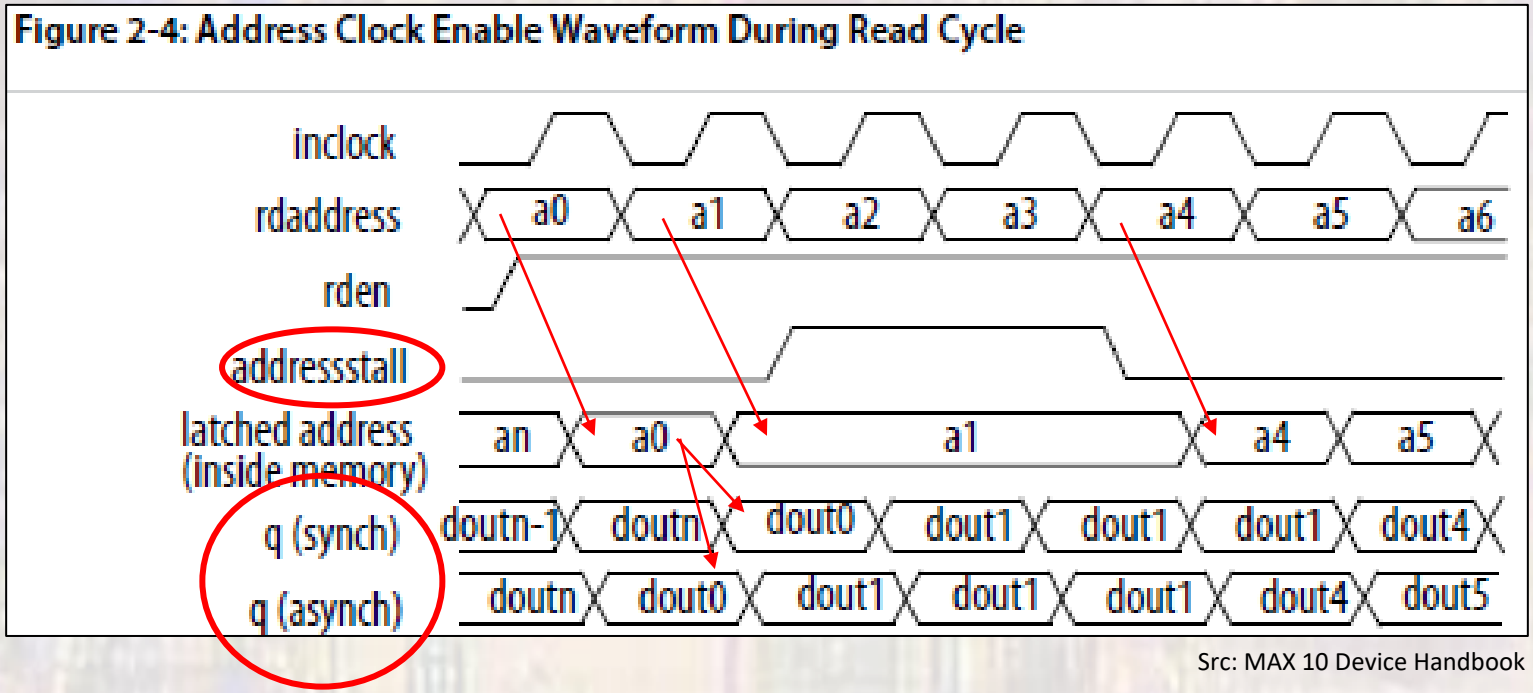
- M9K Fixed Memory Blocks
  - Address Clock Enable
    - Holds the previous address input until enabled
    - Clock gate
    - Implemented as a Stall



Src: MAX 10 Device Handbook

MAX10 Memory - Operation

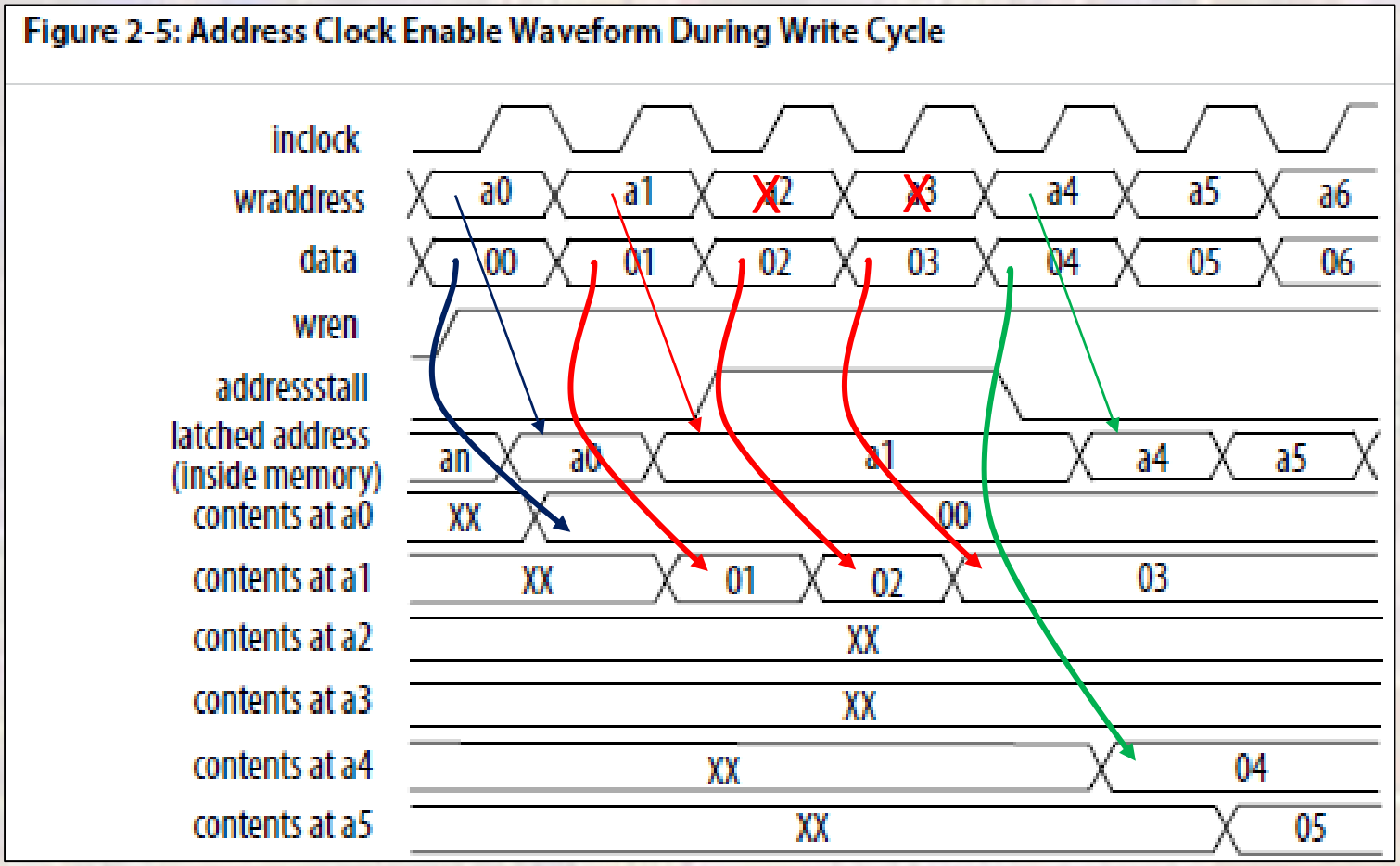
- M9K Fixed Memory Blocks
  - Address Clock Enable - read



Src: MAX 10 Device Handbook

MAX10 Memory - Operation

- M9K Fixed Memory Blocks
  - Address Clock Enable - write



Src: MAX 10 Device Handbook

MAX10 Memory - Operation

- M9K Fixed Memory Blocks
  - Clock Modes

Clock Mode	Description	Modes				
		True Dual-Port	Simple Dual-Port	Single-Port	ROM	FIFO
Independent Clock Mode	A separate clock is available for the following ports: • Port A—Clock A controls all registers on the port A side. • Port B—Clock B controls all registers on the port B side.	Yes	—	—	Yes	—
Input/Output Clock Mode	• M9K memory blocks can implement input or output clock mode for single-port, true dual-port, and simple dual-port memory modes. • An input clock controls all input registers to the memory block, including `data`, `address`, `byteena`, `wren`, and `rden` registers. • An output clock controls the data-output registers.	Yes	Yes	Yes	Yes	—
Read or Write Clock Mode	• M9K memory blocks support independent clock enables for both the read and write clocks. • A read clock controls the data outputs, read address, and read enable registers. • A write clock controls the data inputs, write address, and write enable registers.	—	Yes	—	—	Yes
Single-Clock Mode	A single clock, together with a clock enable, controls all registers of the memory block.	Yes	Yes	Yes	Yes	Yes

Src: MAX 10 Device Handbook

MAX10 Memory - Operation

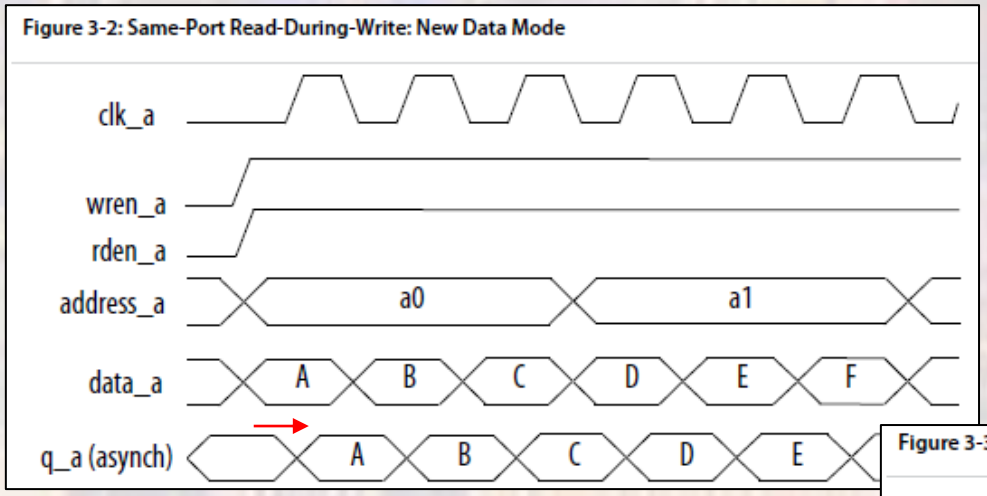
- M9K Fixed Memory Blocks
  - Additional Control Signals
    - Clock Enable
      - Enables the clock
      - If no clock is enabled – no memory activity
    - Asynchronous Clear
      - Clears the output data register if present
      - No clear for the input data register
    - Read/Write
      - Several variations depending on mode

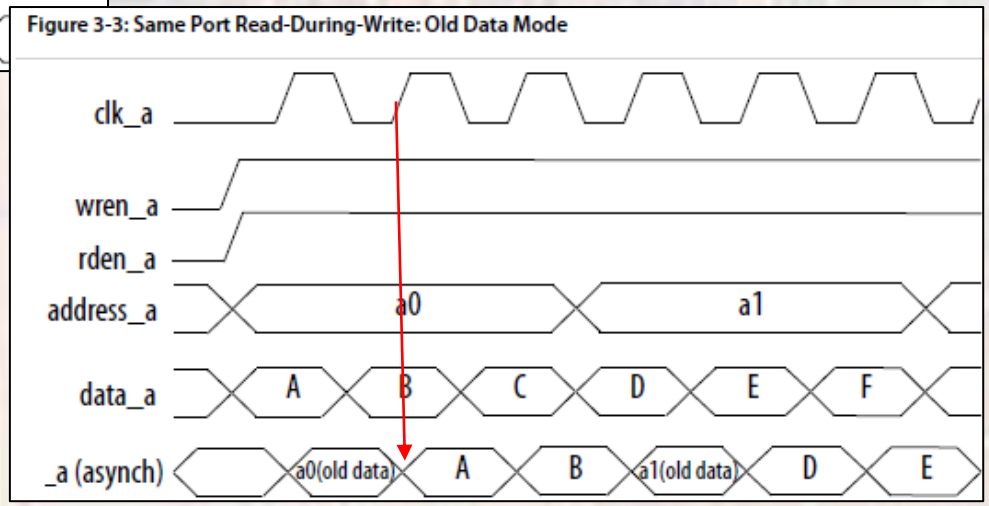
MAX10 Memory - Operation

- M9K Fixed Memory Blocks
  - Data flow-through model
    - All inputs are registered
    - Outputs can be synchronous or asynchronous
    - 2 flow through options
  - Read-during-write – new data
    - Single port, true Dual Port
    - Write data flows through to the output
  - Read-during-write – old data
    - Single port, true Dual Port
    - Old data is provided to the output

MAX10 Memory - Operation

- M9K Fixed Memory Blocks
  - Read during Write





Write complete