

MAX 10 PLL

Last updated 7/20/23

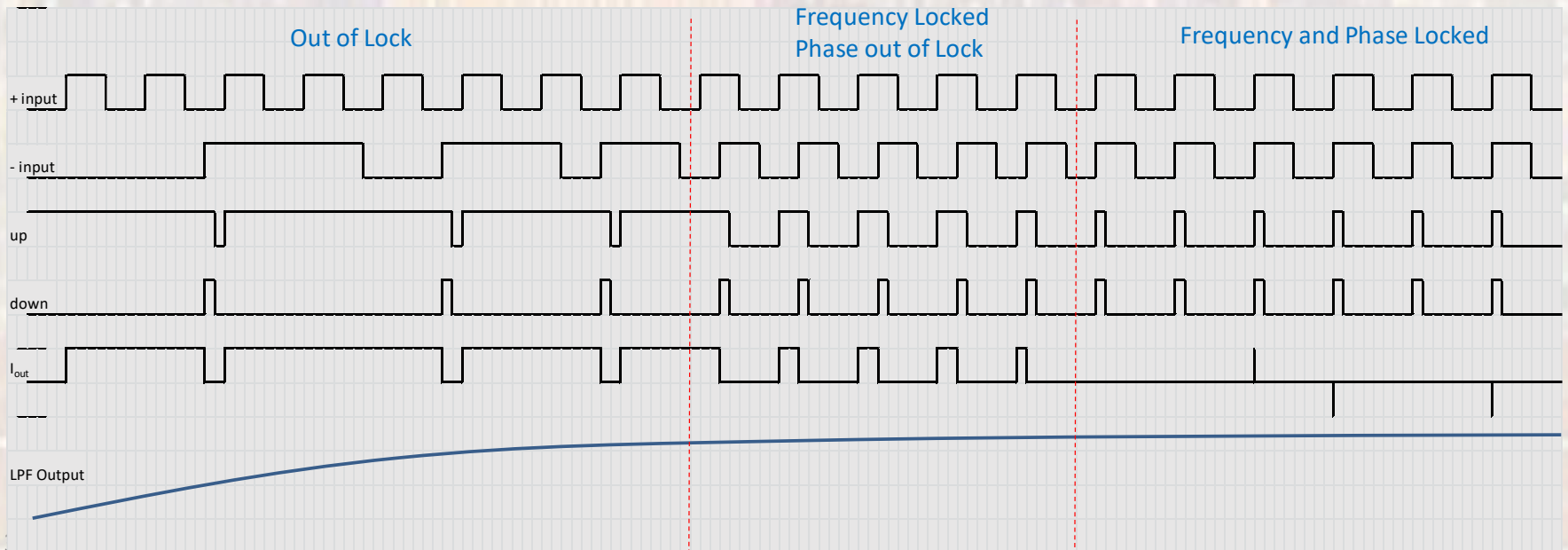
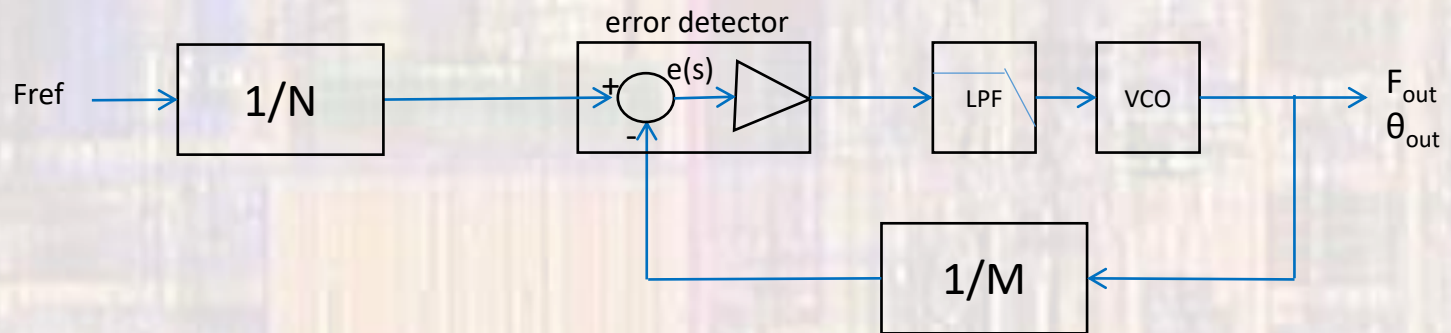
MAX10 PLL

- Phase Locked Loop
 - Designed to match an output signal to the frequency and phase of an input signal
 - Signals must be periodic (clocks)
 - By using input and feedback dividers the PLL can create an output that is a fractional frequency of the input

$$F_{out} = F_{in} \left(\frac{m}{n} \right)$$

MAX10 PLL

- Phase Locked Loop
 - Simplified block diagram



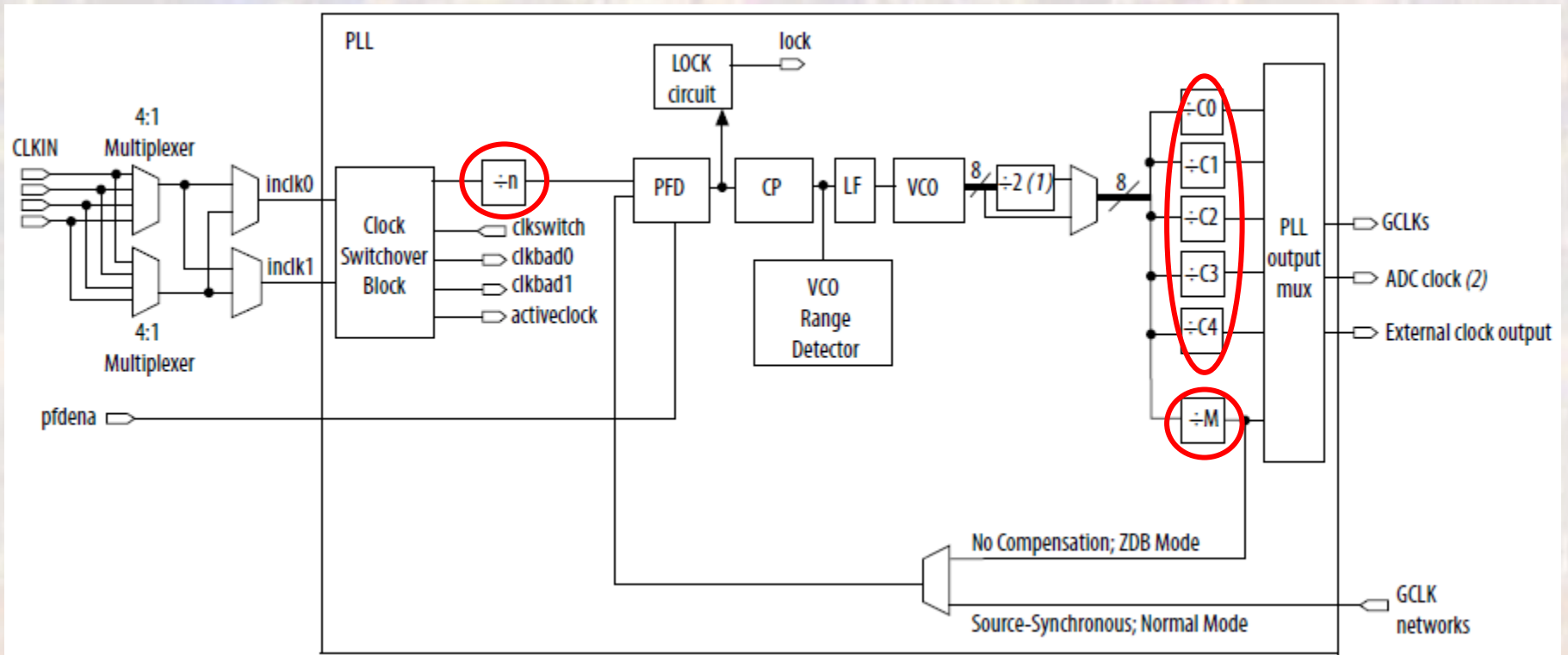
MAX10 PLL

- Phase Locked Loop
 - MAX10 Features
 - M/N divider
 - M: 1 – 512
 - N: 1 – 512
 - Post-scale counters (c0 – c4)
 - 1 to 512
 - Single or differential input
 - 5 internal logic outputs/PLL
 - 1 external (pin) output/PLL
 - Lock signal
 - Extensive multiplexing
 - Phase shift capability
 - Programmable output duty cycle

MAX10 PLL

- Phase Locked Loop

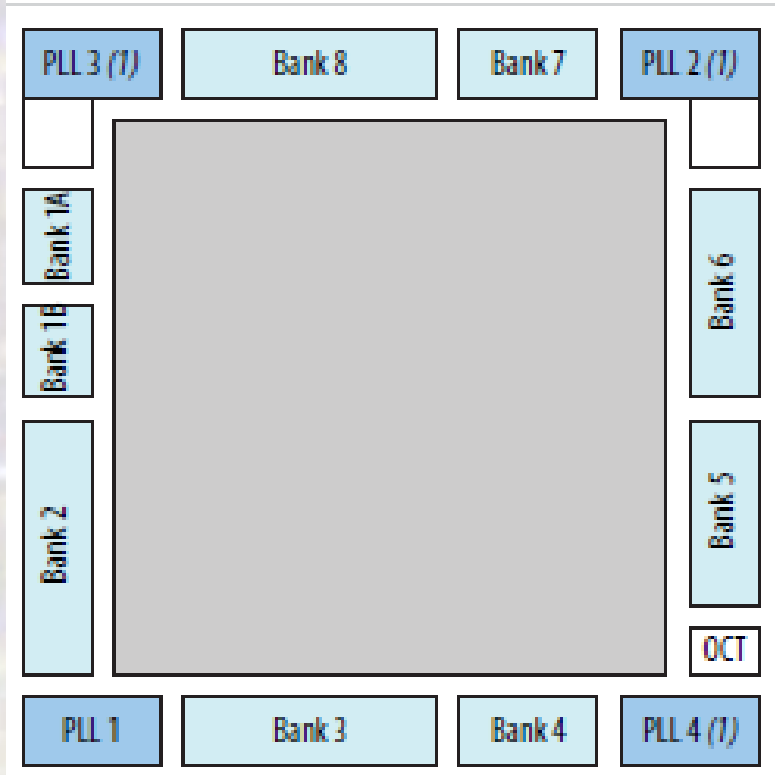
$$F_{out} = F_{in} \left(\frac{M}{n} \right) \left(\frac{1}{C} \right)$$



Src: MAX 10 Device Handbook

MAX10 PLL

- Phase Locked Loop
 - MAX 10M50
 - 4 PLLs



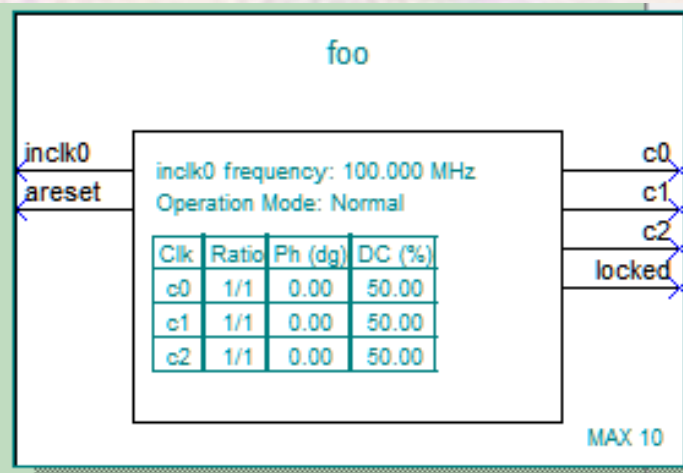
Src: MAX 10 Device Handbook

MAX10 PLL

- Phase Locked Loop

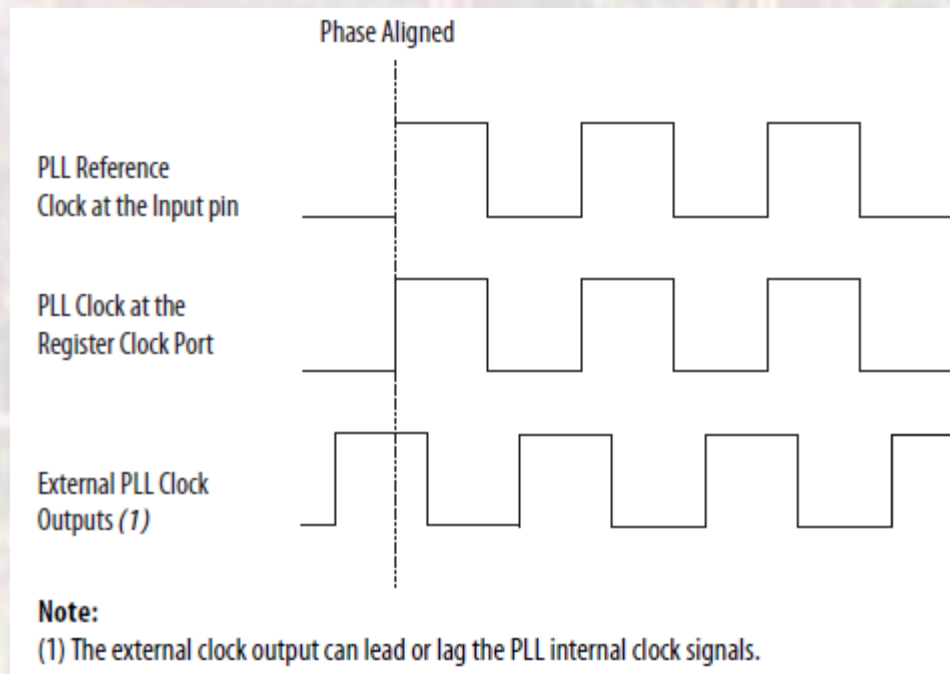
- Signals

- Clock Input(s)
- Clock Outputs
- Lock Output
- pllenna
 - PLL enable
- areset
 - PLL reset
 - Clears counters
- pfdena
 - Turns off the charge pumps
 - VCO continues to operate but no longer updates



MAX10 PLL

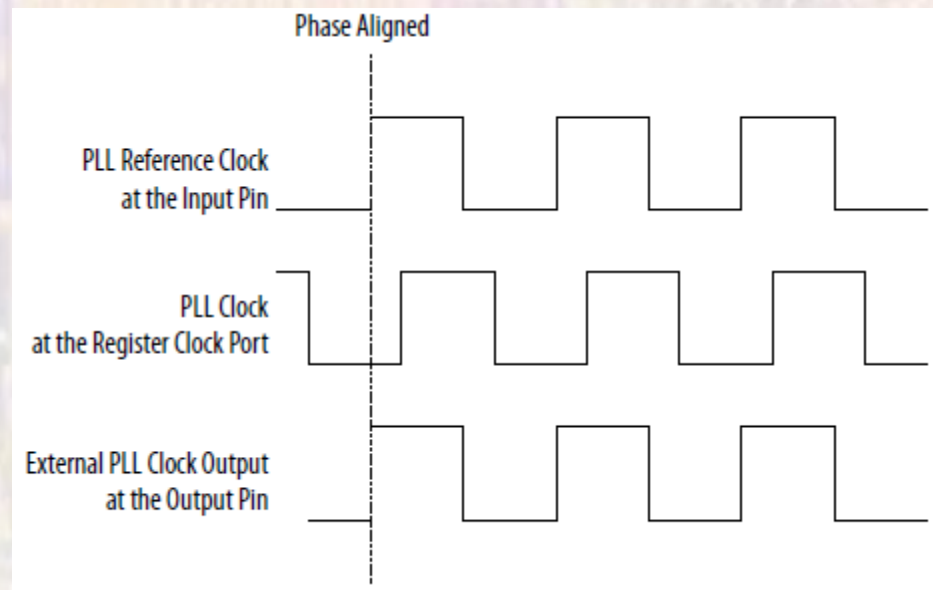
- Phase Locked Loop
 - Normal Mode Operation
 - Clock signal at register inputs is phase locked
 - External clock signal may lead or lag the internal signals



Src: MAX 10 Device Handbook

MAX10 PLL

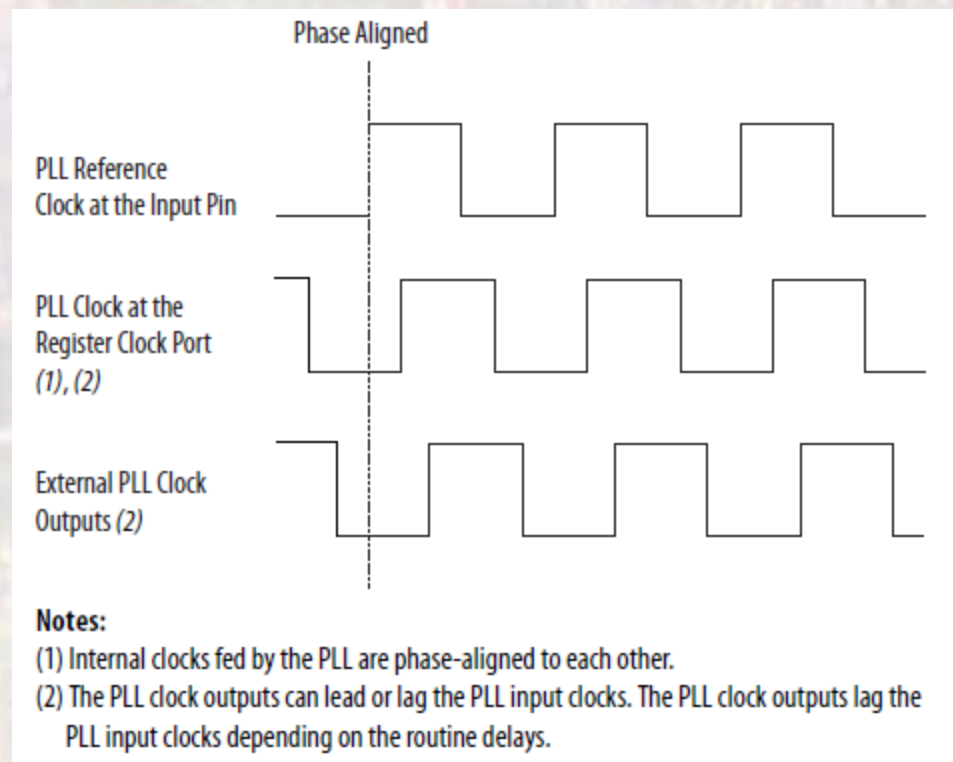
- Phase Locked Loop
 - Zero Delay Buffer Mode Operation
 - Clock signal at output pin is phase locked
 - Internal clock signal at the register inputs may lead or lag the input signal



Src: MAX 10 Device Handbook

MAX10 PLL

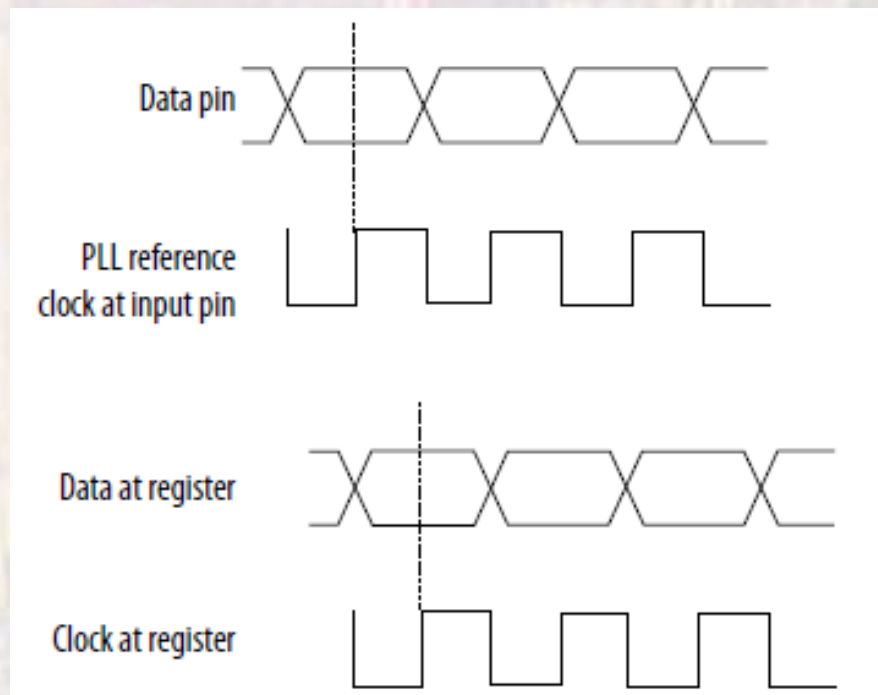
- Phase Locked Loop
 - No Compensation Mode Operation
 - PLL is locked but no compensation made for clock loads/paths
 - Lowest jitter configuration



Src: MAX 10 Device Handbook

MAX10 PLL

- Phase Locked Loop
 - Source Synchronous Mode Operation
 - Data/Clk phase relationship maintained
 - Input/Output phase relationship is lost



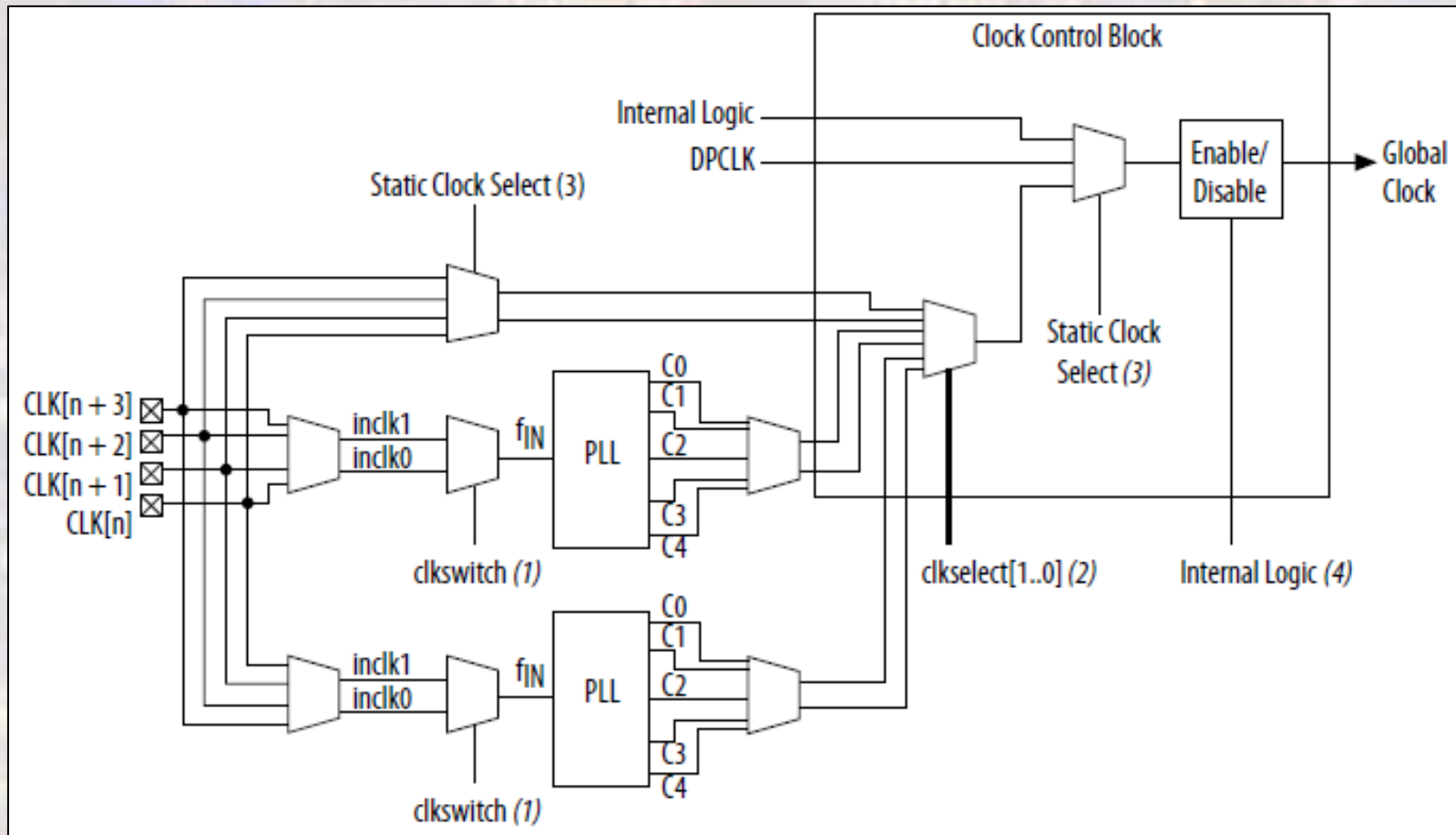
Src: MAX 10 Device Handbook

MAX10 PLL

- Phase Locked Loop
 - Programmable Duty Cycle
 - Output duty cycle can be programmed
 - Granularity = 50% / Count
 - Count is a setting on the post scale counter
 - High, low count value
 - Programmable Phase Shift
 - Coarse and Fine shifting

MAX10 PLL

- Phase Locked Loop
 - Multiplexing



Src: MAX 10 Device Handbook

MAX10 PLL

- Phase Locked Loop
- Multiplexing

