Measuring Gate Delays

Last modified 1/8/24

Measuring Gate Delays

- Source Effects
  - Need to guard against source effects in both simulation and lab testing
  - Ideal sources do not exist in real designs
    - Unlimited current
    - No over/under shoot
    - No limits on slew rate
- Load Effects
  - The standard for measuring gate delays differs for:
    - Designs using discrete parts on a PCB
      - Use a fixed load capacitance (10pF, 25pF, 50pf)
    - Integrated circuit designs
      - Use one input from a minimum 2 input NAND gate

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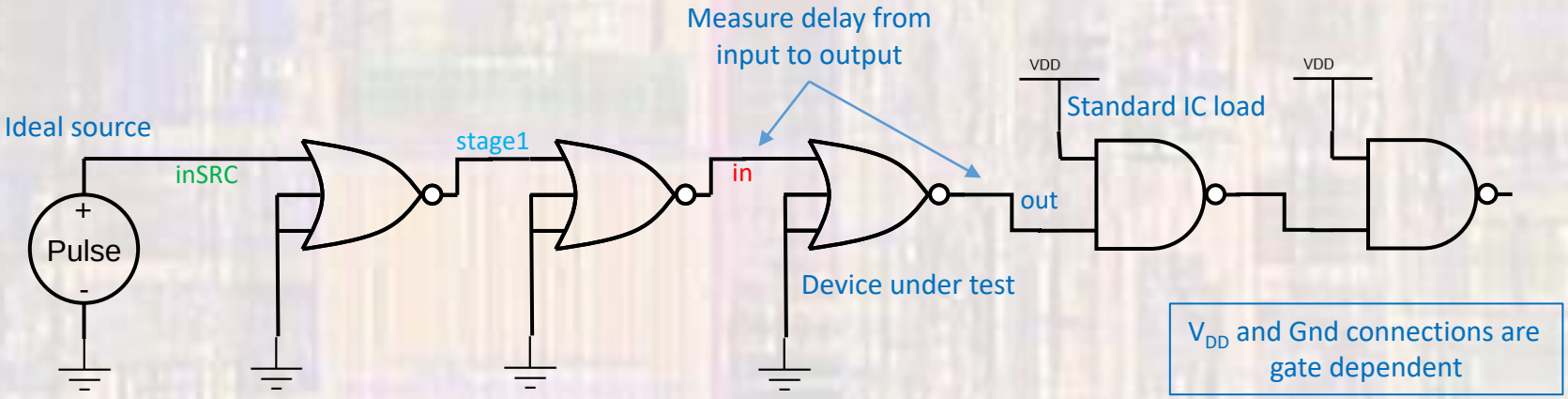
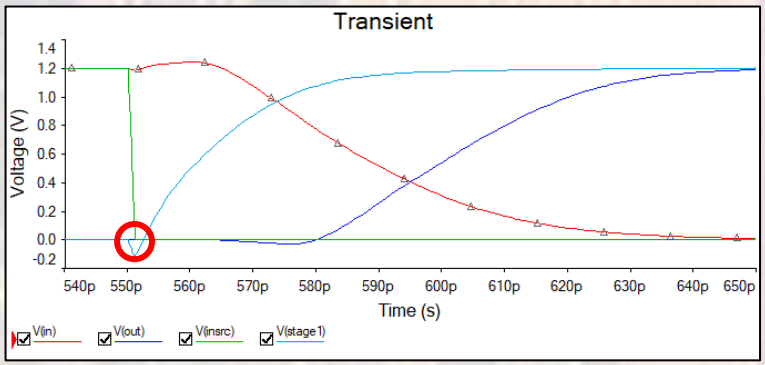
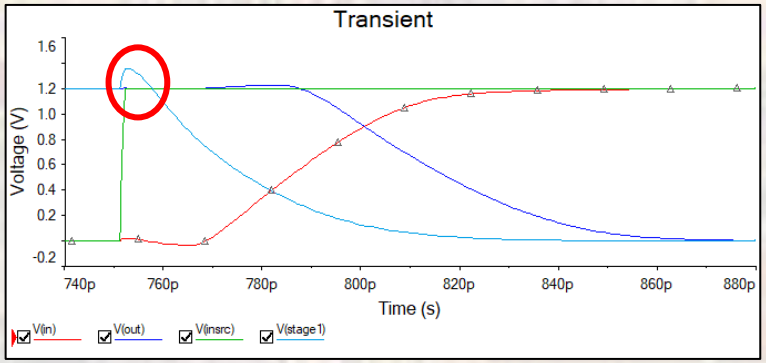
- Isolate the source
  - Chain gates of the same type to isolate the source







Example test for 3 input NOR (IC method)