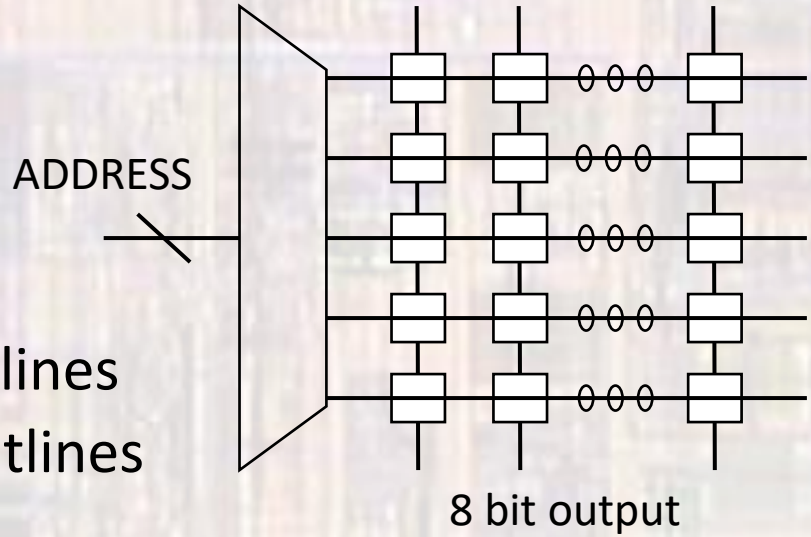
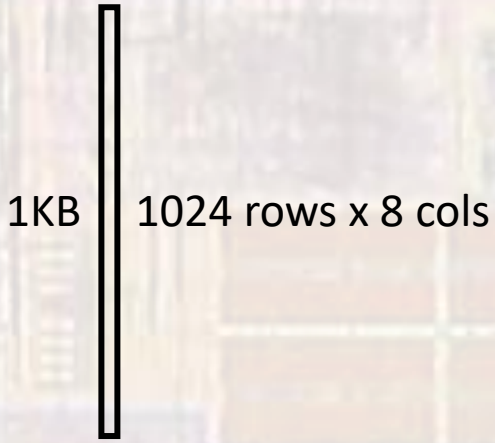
Memory Architecture

Last updated 9/19/23

Memory Architecture

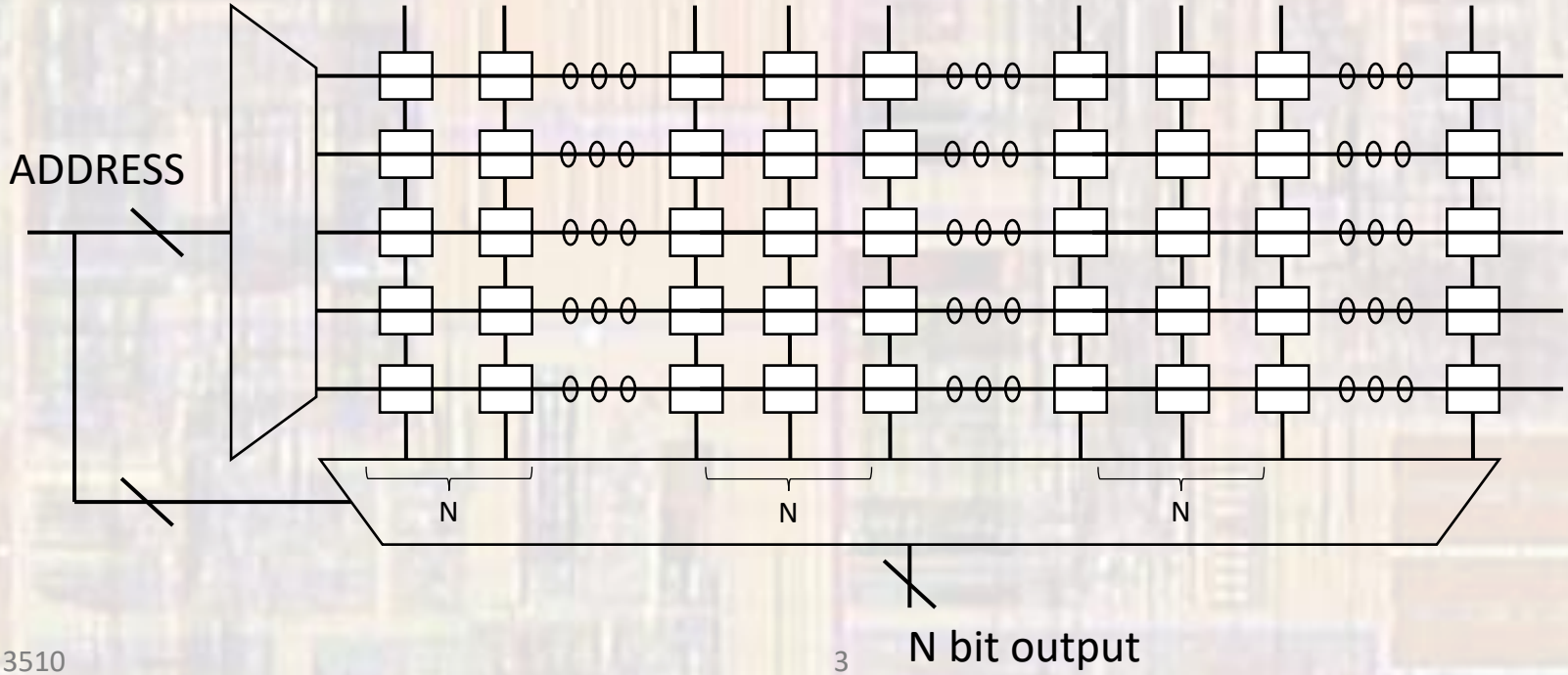
- Basic Memory Topology
  - Array of single bit cells
  - Row decoder chooses 1 row
  - Rows are typically called wordlines
  - Columns are typically called bitlines
  - Non optimal
    - Physical implementation
      - Array
      - Decoder
    - Speed
      - Column capacitance very large





Memory Architecture

- General Memory Topology
  - Array of n bit cells
  - Row decoder chooses 1 row
  - Column decoder chooses one N bit ‘column’
    - 1,4,8,16,32,64,128,… bits/column



Memory Architecture

- Memory Descriptive Terminology
  - 16Mb in a x4
    - 16Mb total memory, each memory address provides 4 bits
  - 16Mb x 4
    - 64Mb total memory, each memory address provides 4 bits
    - Could be configured as 4 16MB memories, each providing 1b to the output

Memory Architecture

- Example – 16Mb in a x4 configuration

x4 means each column is 4 bits

or each address points to 4 bits

16Mb → 16,777,216 bits

16Mb in a x4 configuration → 4 bits / address → 4,194,304 - individual addresses

4,194,304 addresses → 22 address bits

x4 means 4 bit cells for every column

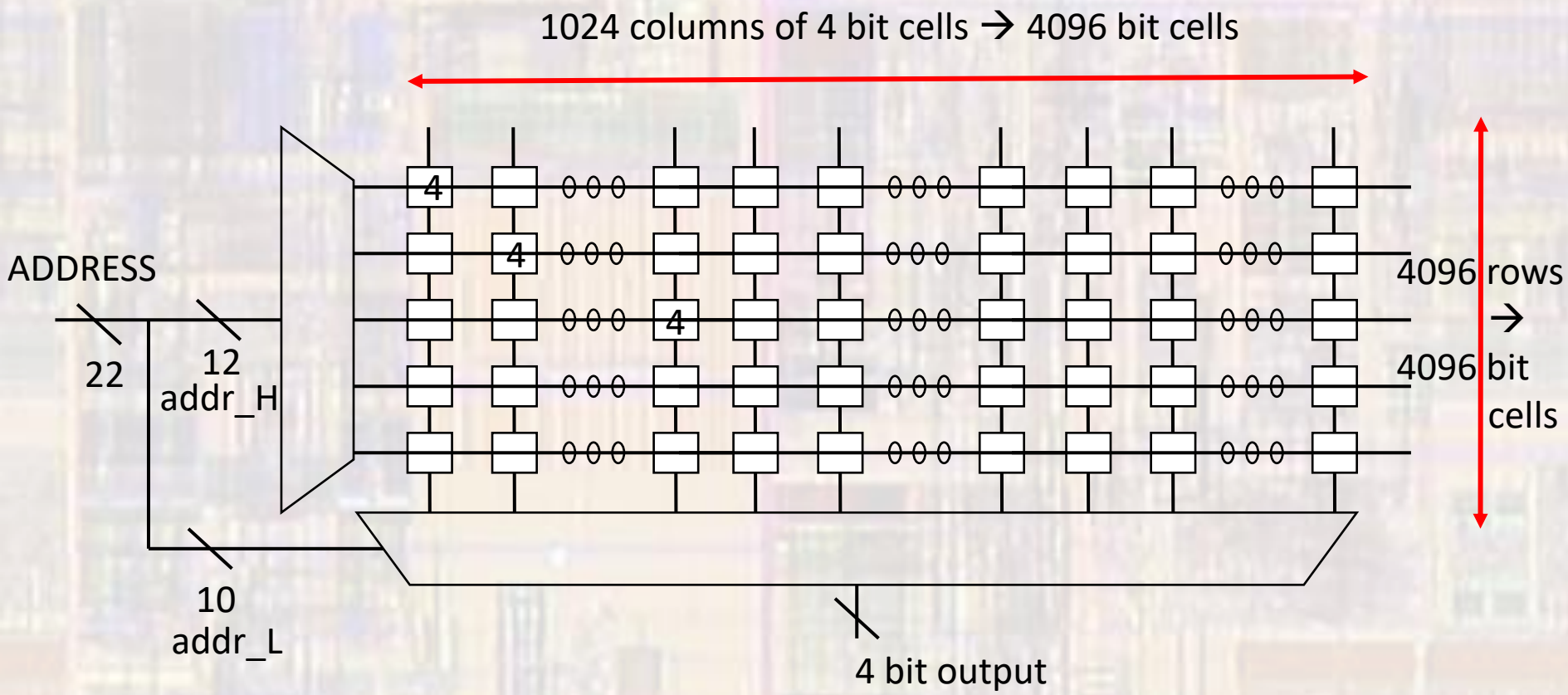
Assuming a square memory array and a square bit cell → 4 times as many rows as columns

4 times as many rows as columns → 2 more row address bits than column address bits

22 address bits → 12 bits for row addresses and 10 bits for column addresses

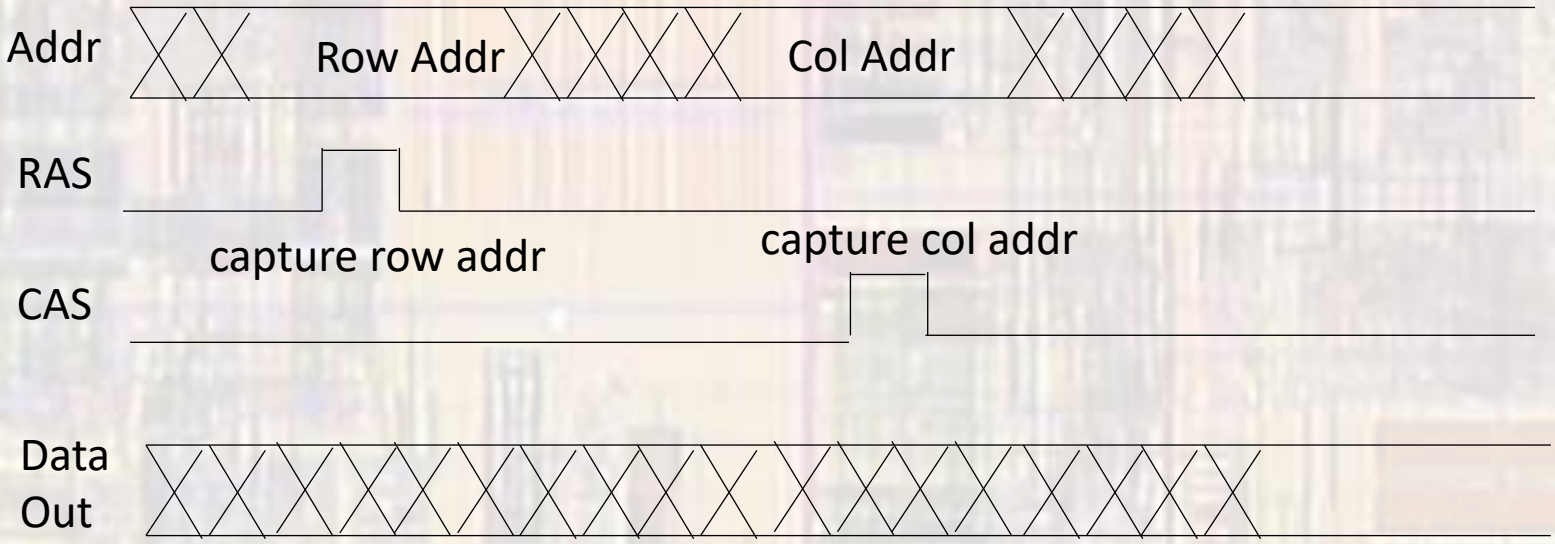
Memory Architecture

- Example – 16Mb in a x4 configuration



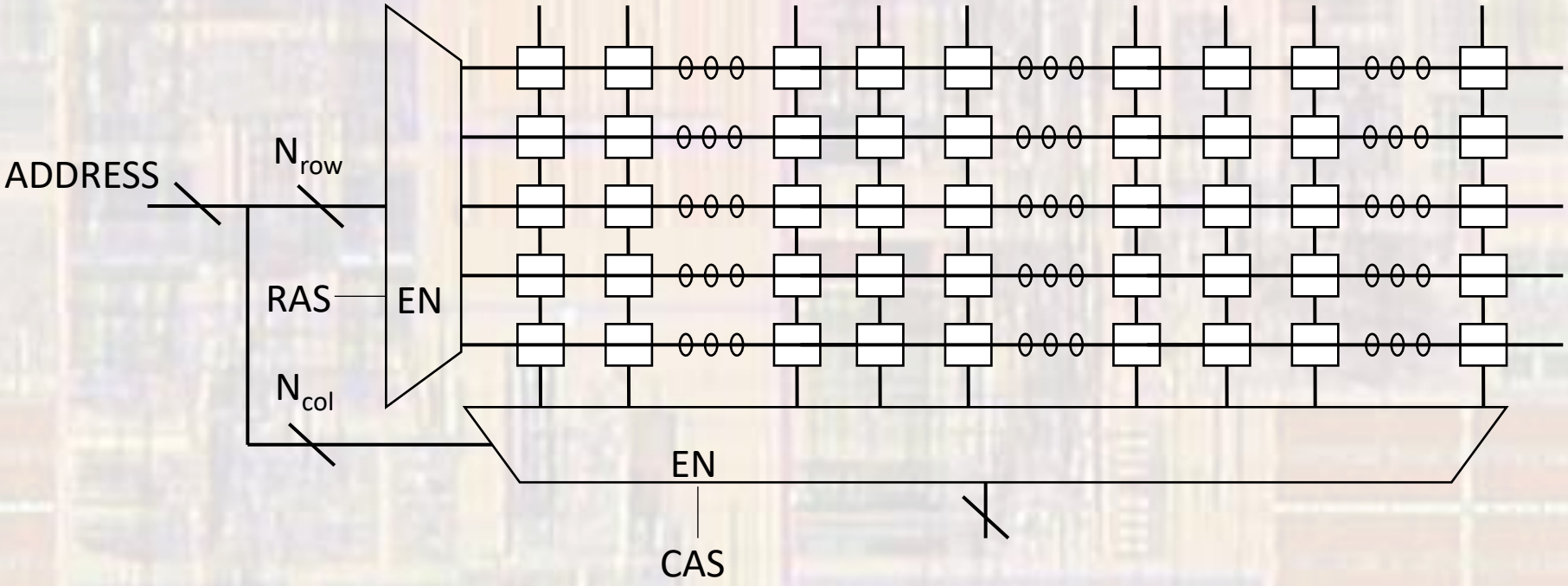
Memory Architecture

- Address Line Sharing
  - Reduce I/O by sharing the address inputs between Row addresses and Column addresses in time
  - RAS – Row Address Strobe (current address is for row decode)
  - CAS – Column Address Strobe (current address is for column decode)



Memory Architecture

- Address Line Sharing
  - Reduce I/O by sharing the address inputs between Row addresses and Column addresses – in time
  - Number of address bits is the greater of the number of row address bits and column address bits



Memory Architecture

- Address Line Sharing
  - Reduce I/O by sharing the address inputs between Row addresses and Column addresses
  - 22 bit addr → 12 bit addr + RAS and CAS → 14 wires
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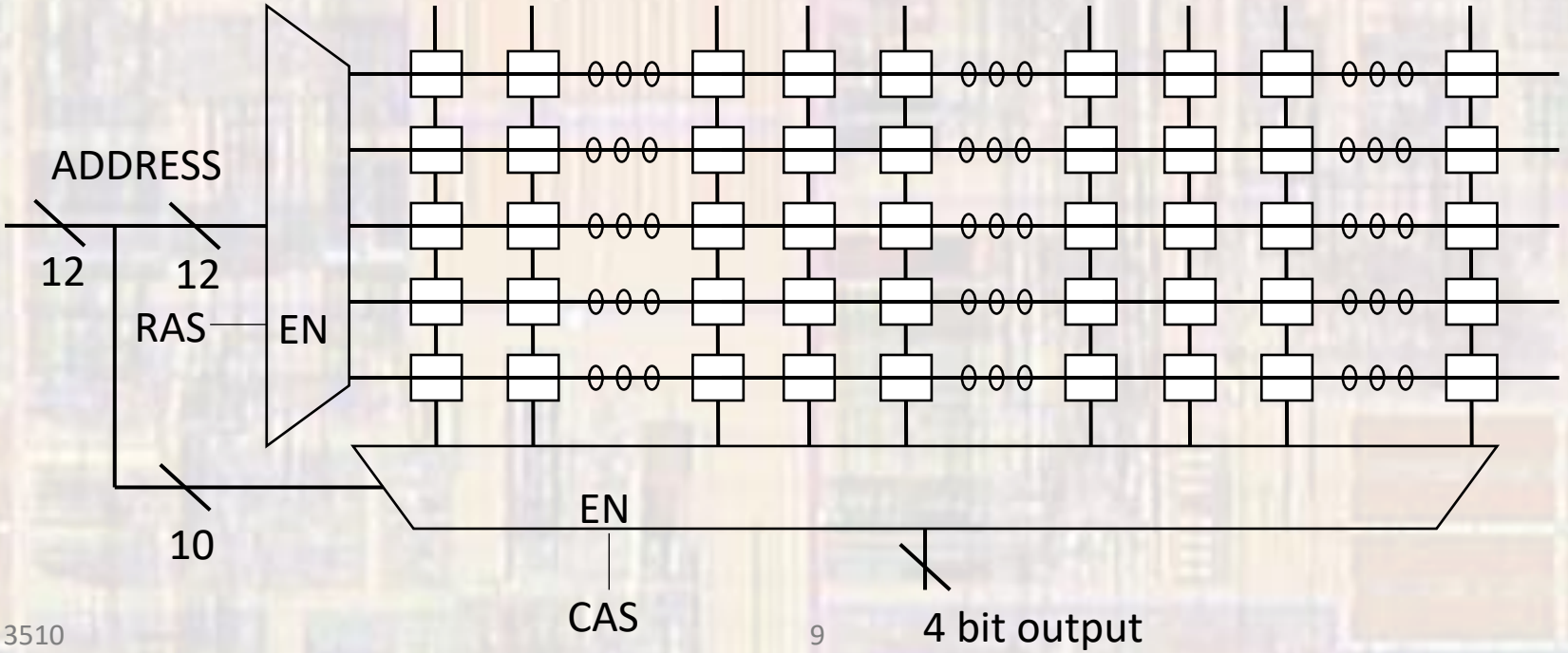

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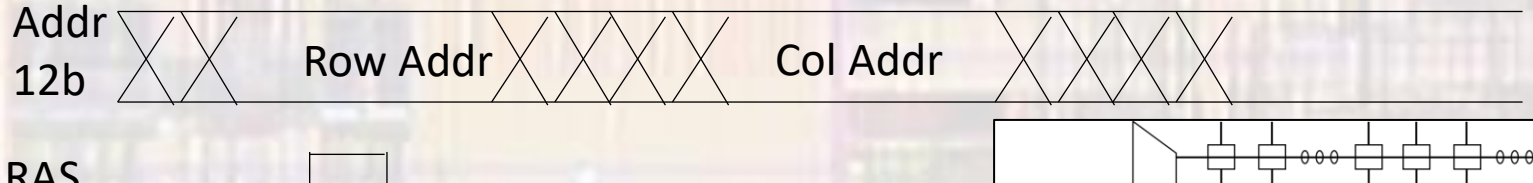

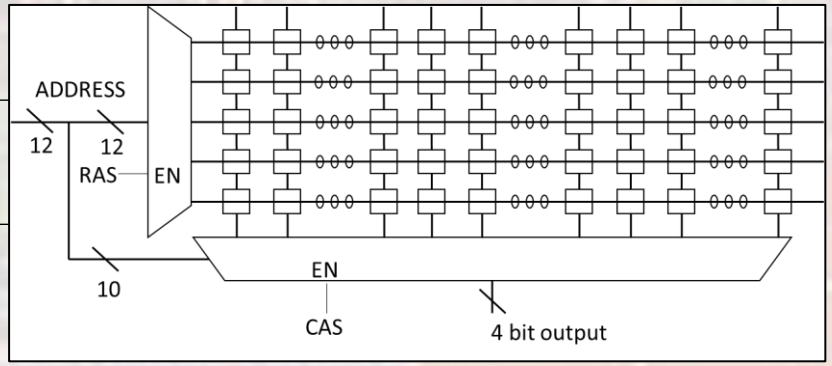

Memory Architecture

- Performance Issues
  - Can 1 bad array element ruin an entire part?
  - Use redundant rows and columns in the array
    - Any bad cells are programmed out at final test
  - Some Memory Management Units (MMUs) can detect poorly performing calls and modify the virtual to physical address translation to remove them from the memory map