Memory Logical View

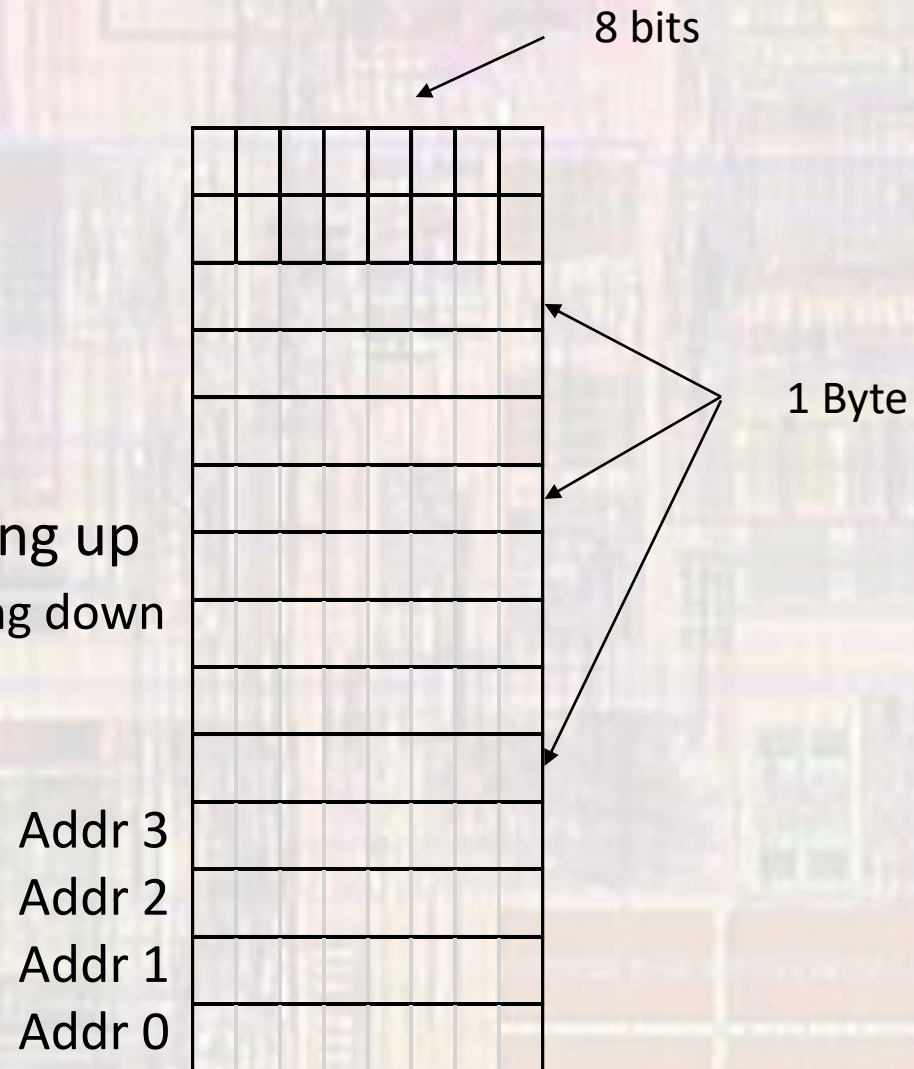## Last updated 9/19/23

These slides introduce semiconductor memories

Memory – Logical View

- Elements

  - Minimum logical element
    - 1 – bit (b)
    - Has a logical value of '0' or '1'
    - Has a physical value of "vdd" or "gnd"
      - 5v, 3.3v, 2.4v, 1.8v, 1.2v

  - Minimum accessible storage element
    - 1- Byte (B)
    - 8 bits

  - Minimum Addressable element
    - 1 – Word
    - Situational dependent length
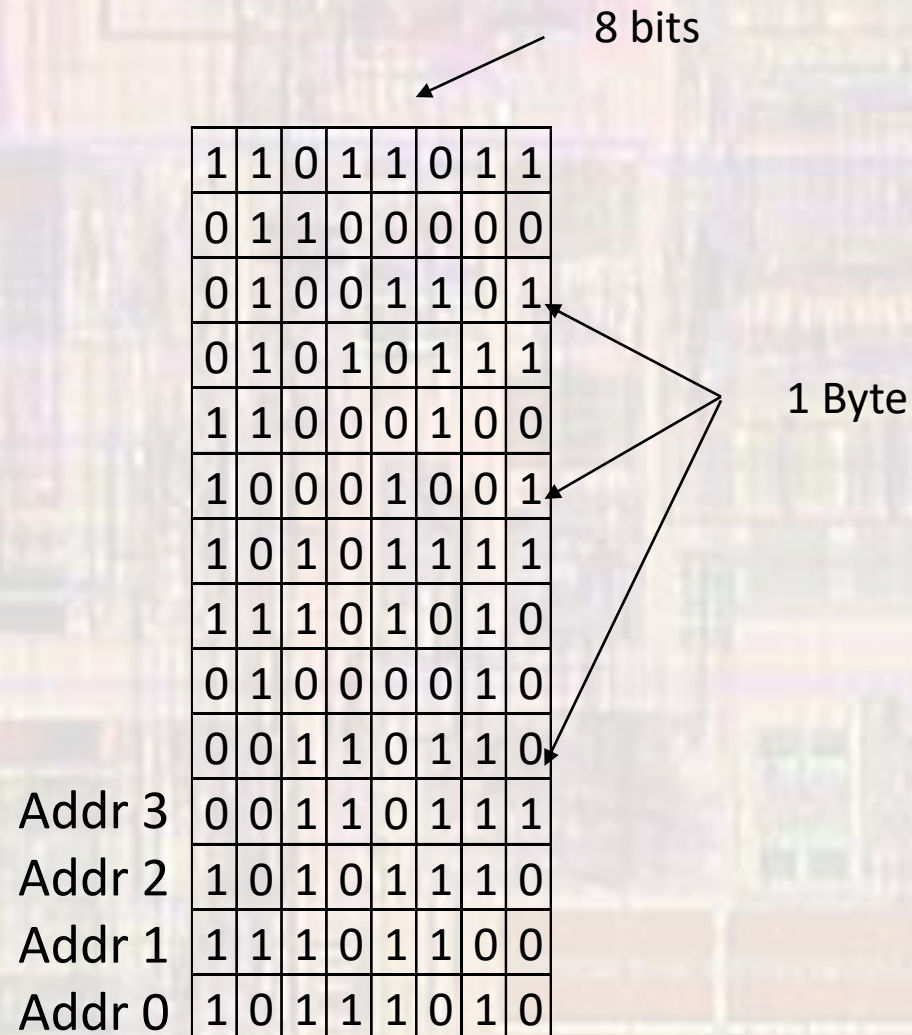   - 1B, 2B, 4B, 8B, 16B, …

Memory – Logical View

- Logical configuration

  - Long column of bytes

  - 1st address is "0"

  - Typically thought of as growing up
    - Sometimes thought of as growing down

8 bits

1 Byte

Addr 3
Addr 2
Addr 1
Addr 0

Memory – Logical View

- Initialization

  - Even though we may not have stored anything in a specific memory location
    - It has a value
    - The value is likely random

8 bits

1 Byte

1	1	0	1	1	0	1	1
0	1	1	0	0	0	0	0
0	1	0	0	1	1	0	1
0	1	0	1	0	1	1	1
1	1	0	0	0	1	0	0
1	0	0	0	1	0	0	1
1	0	1	0	1	1	1	1
1	1	1	0	1	0	1	0
0	1	0	0	0	0	1	0
0	0	1	1	0	1	1	0

Addr 3	0	0	1	1	0	1	1	1
Addr 2	1	0	1	0	1	1	1	0
Addr 1	1	1	1	0	1	1	0	0
Addr 0	1	0	1	1	1	0	1	0

Memory – Logical View

- Write

  - Provide Address and Data

  - Write (addr 4, 11101000)
  - Write (addr 6, 00000101)
  - Write (addr 10, 11001010)

  - Note: Writing overwrites existing data

0	0	1	0	0	1	1	1
1	1	1	0	1	0	0	0
0	0	0	1	1	1	0	1
1	1	0	0	1	0	1	0
0	1	1	1	1	0	1	1
0	0	0	1	0	0	0	1
0	0	0	1	1	1	0	1
0	0	0	0	0	1	0	1
1	0	1	1	0	1	0	0
1	1	1	0	1	0	0	0
1	0	0	1	0	1	1	1
1	1	0	1	1	1	0	1
1	1	0	1	0	1	0	0
1	0	1	0	1	0	0	1

Addr 3
Addr 2
Addr 1
Addr 0

Memory – Logical View

- Read

  - Provide Address

  - Read (addr 4) → 11101000
  - Read (addr 6) → 00000101
  - Read (addr 8) → ????????

  - NOTE: Reading does not destroy the data

0	0	1	0	0	1	1	1
1	1	1	0	1	0	0	0
0	0	0	1	1	1	0	1
1	1	0	0	1	0	1	0
0	1	1	1	1	0	1	1
0	0	0	1	0	0	0	1
0	0	0	1	1	1	0	1
0	0	0	0	0	1	0	1
1	0	1	1	0	1	0	0
1	1	1	0	1	0	0	0
1	0	0	1	0	1	1	1
1	1	0	1	1	1	0	1
1	1	0	1	0	1	0	0
1	0	1	0	1	0	0	1

Addr 3
Addr 2
Addr 1
Addr 0

Memory – Logical View

- Addresses

  - Addresses are NOT part of the memory array

  - Addresses are logic circuits to choose which part of the array to read from or write to – decoders determine the location

0	0	1	0	0	1	1	1
1	1	1	0	1	0	0	0
0	0	0	1	1	1	0	1
1	1	0	0	1	0	1	0
0	1	1	1	1	0	1	1
0	0	0	1	0	0	0	1
0	0	0	1	1	1	0	1
0	0	0	0	0	1	0	1
1	0	1	1	0	1	0	0
1	1	1	0	1	0	0	0
1	0	0	1	0	1	1	1
1	1	0	1	1	1	0	1
1	1	0	1	0	1	0	0
1	0	1	0	1	0	0	1

Addr 3
Addr 2
Addr 1
Addr 0

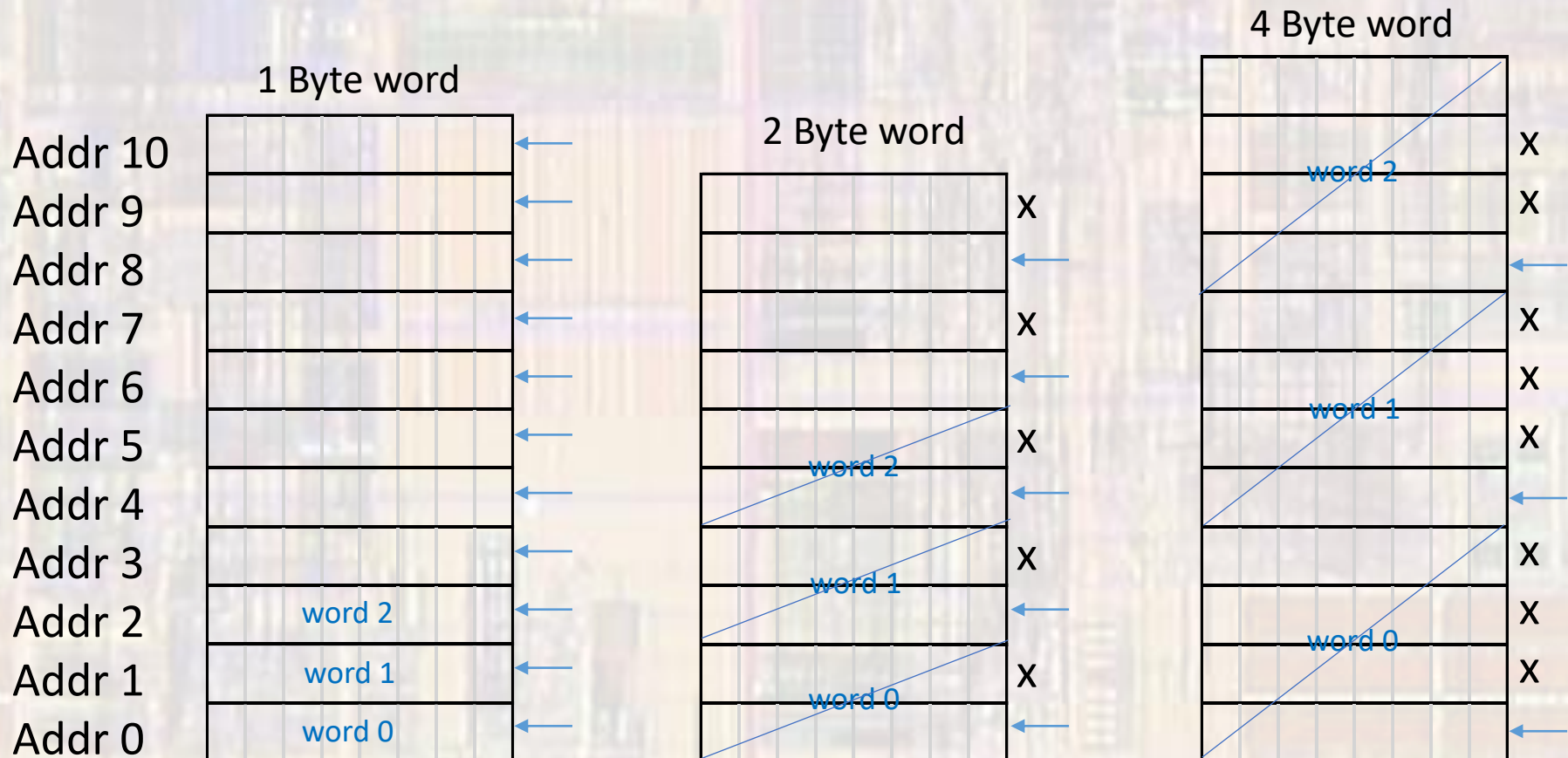# Memory – Logical View

- ## Word Alignment

  - ### Processors work with data WORDS

  - ### Size of the internal registers
    - 1 Byte – 8 bit processor
    - 2 Bytes – 16 bit processor
    - 4 Bytes – 32 bit processor
    - 8 Bytes – 64 bit processor

  - ### Memory is word aligned
    - Must access the entire word
    - Not allowed/possible to access inside a word*

    * exceptions exist

Memory – Logical View

- Word Alignment
  - Allowed addresses indicated by ←

1 Byte word

Addr 10		←
Addr 9		←
Addr 8		←
Addr 7		←
Addr 6		←
Addr 5		←
Addr 4		←
Addr 3		←
Addr 2	word 2	←
Addr 1	word 1	←
Addr 0	word 0	←

2 Byte word

X
← (Addr 8)
X
← (Addr 6)
X word 2
← (Addr 4)
X word 1
← (Addr 2)
X word 0
← (Addr 0)

4 Byte word

word 2   X
          X
← (Addr 8)
word 1   X
          X
← (Addr 4)
word 0   X
          X
← (Addr 0)

Memory – Logical View

- Endianness
  - The order words > 1B are stored in memory
  - data value 01110111 10111011 11011101 01110111 in a 4 byte word

Big Endian

Addr 10									X
Addr 9									X
Addr 8									←
Addr 7									X
Addr 6									X
Addr 5									X
Addr 4									←
Addr 3	1	1	1	0	1	1	1	0	X
Addr 2	1	1	0	1	1	1	0	1	X
Addr 1	1	0	1	1	1	0	1	1	X
Addr 0	0	1	1	1	0	1	1	1	←

Most significant byte Stored in lowest memory

Little Endian

									X
									X
									←
									X
									X
									X
									←
	0	1	1	1	0	1	1	1	X
	1	0	1	1	1	0	1	1	X
	1	1	0	1	1	1	0	1	X
	1	1	1	0	1	1	1	0	←

Least significant byte Stored in lowest memory