MidTerm Project Notes

- Implementation Notes
  - Normally the Register file would only have Read_Data_1 and Read_Data_2 outputs – but – because we want to see the internal register values you need to also have outputs for RegA, RegB, RegC, and RegD

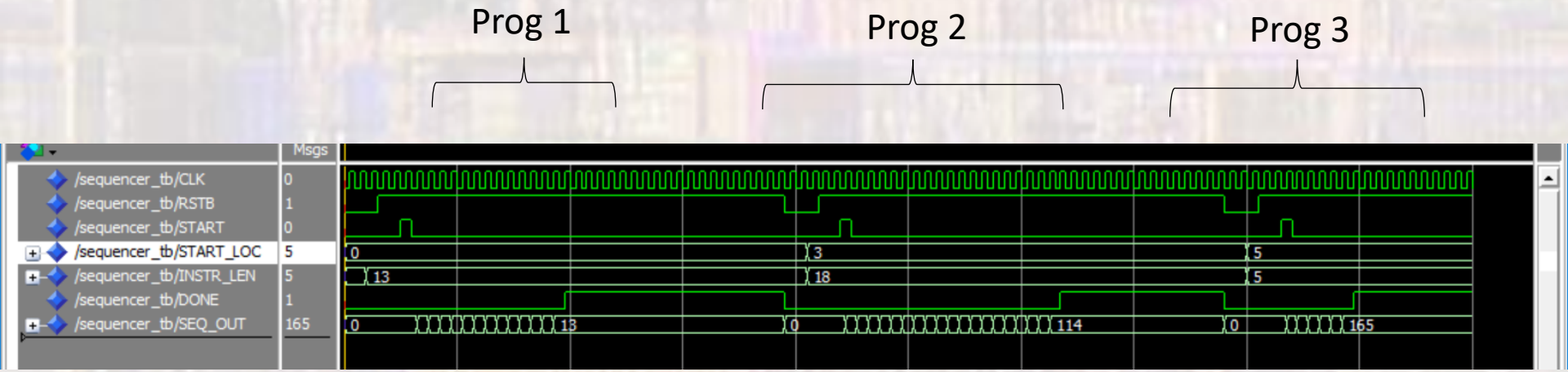
```
entity reg_file is
   port (
      i_clk :           in std_logic;
      i_reg1_addr :     in std_logic_vector(1 downto 0);
      i_reg2_addr :     in std_logic_vector(1 downto 0);
      i_wreg_addr :     in std_logic_vector(1 downto 0);
      i_wreg_data :     in std_logic_vector(7 downto 0);
      i_we_b:           in std_logic;

      o_reg1_data:      out std_logic_vector(7 downto 0);
      o_reg2_data:      out std_logic_vector(7 downto 0);

      o_regA_data:      out std_logic_vector(7 downto 0);
      o_regB_data:      out std_logic_vector(7 downto 0);
      o_regC_data:      out std_logic_vector(7 downto 0);
      o_regD_data:      out std_logic_vector(7 downto 0)
    );
end entity;
```

MidTerm Project Notes

- Implementation Notes
  - Create a sseg output block to do the conversion from binary to sseg display and place 6 of them in the DE10 top level design
    - Takes the nibble from the register and converts it to a sseg display value
    - 2 for each register value
    - See the DE10 RTL view later in the notes

MidTerm Project Notes

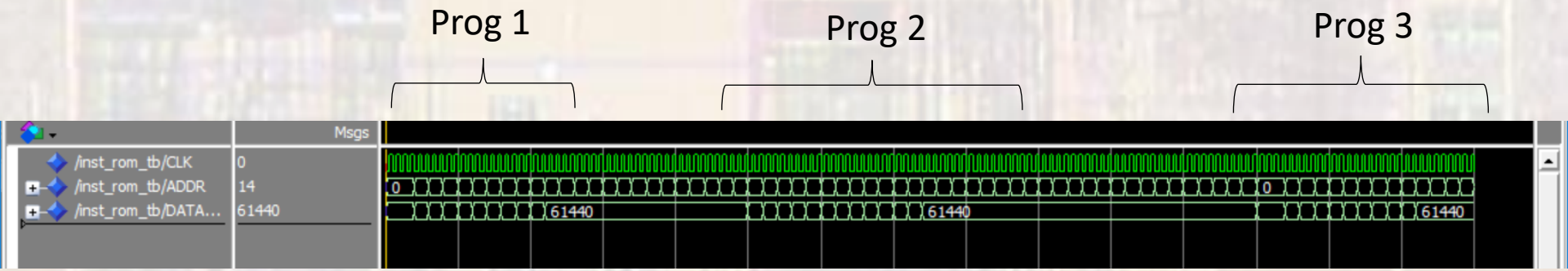
- Sequencer Simulation



MidTerm Project Notes

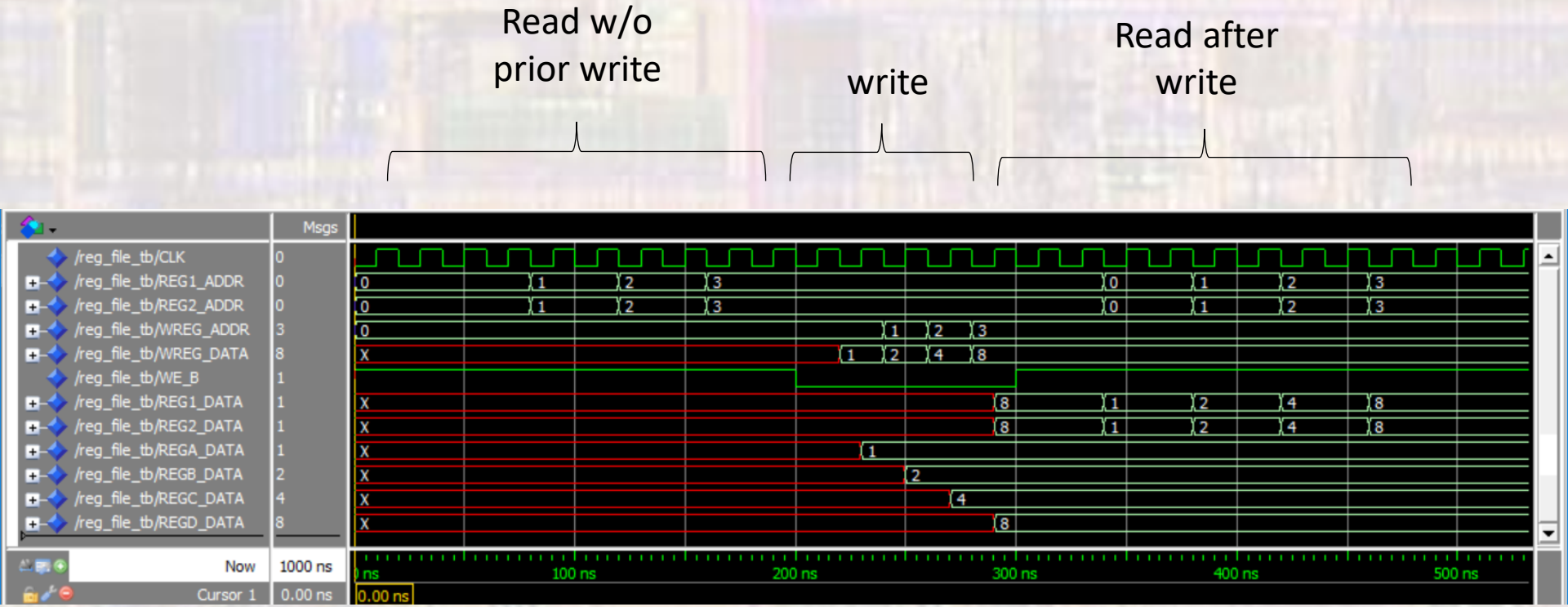
- Instruction ROM
  - Mux based using VHDL Memories, slide 4
  - Add addresses to the constant section
    - Only the addresses you are using
    - Others go to NOP: x”F000”

```
-- ROM contents
constant instr_ROM: rom_type:=(
        0 =>        X"C010",
        1 =>        X"C04A",
        2 =>        X"5180",
            • • •

        64 =>       x"C002",
        65 =>       x"C044",
        66 =>       x"C088",
            • • •
        others =>   x”F000”
);
```



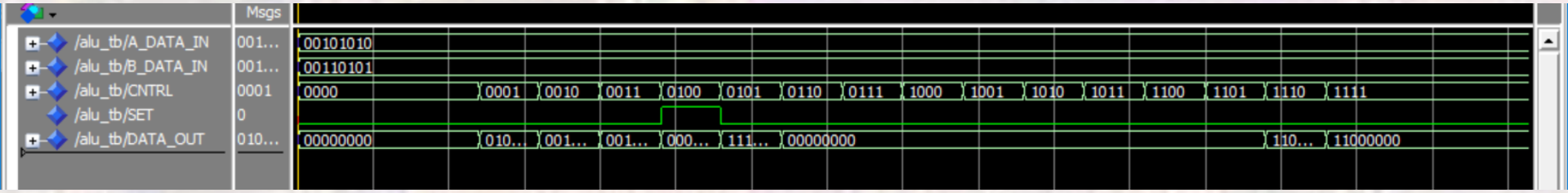
MidTerm Project Notes

- Register File Simulation



MidTerm Project Notes

- ALU Simulation

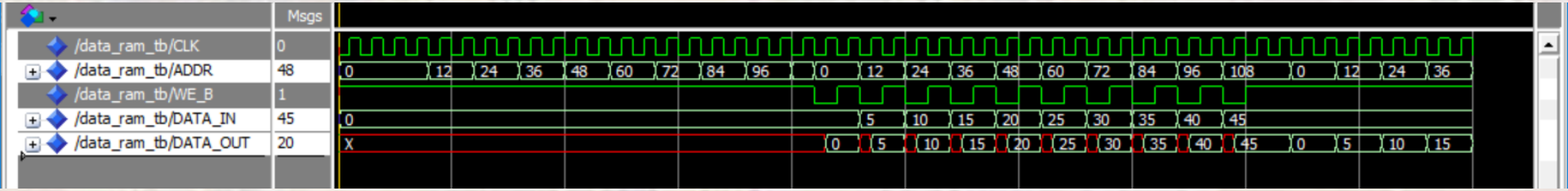


- Data RAM Simulation

Read w/o prior write

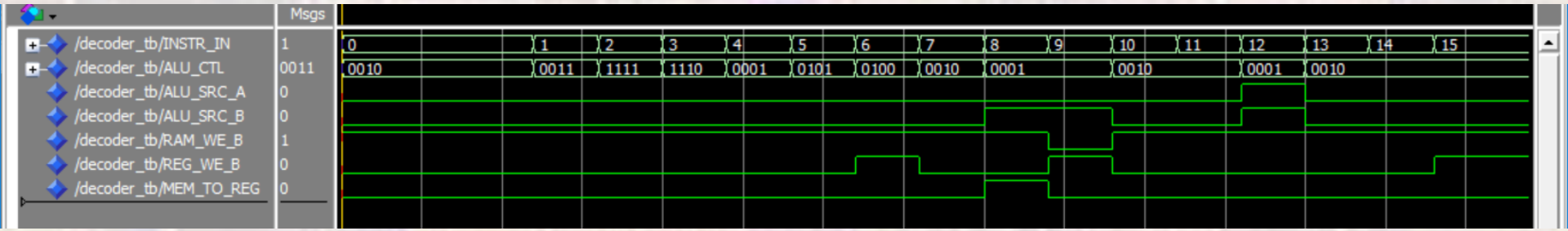
write

Read after write



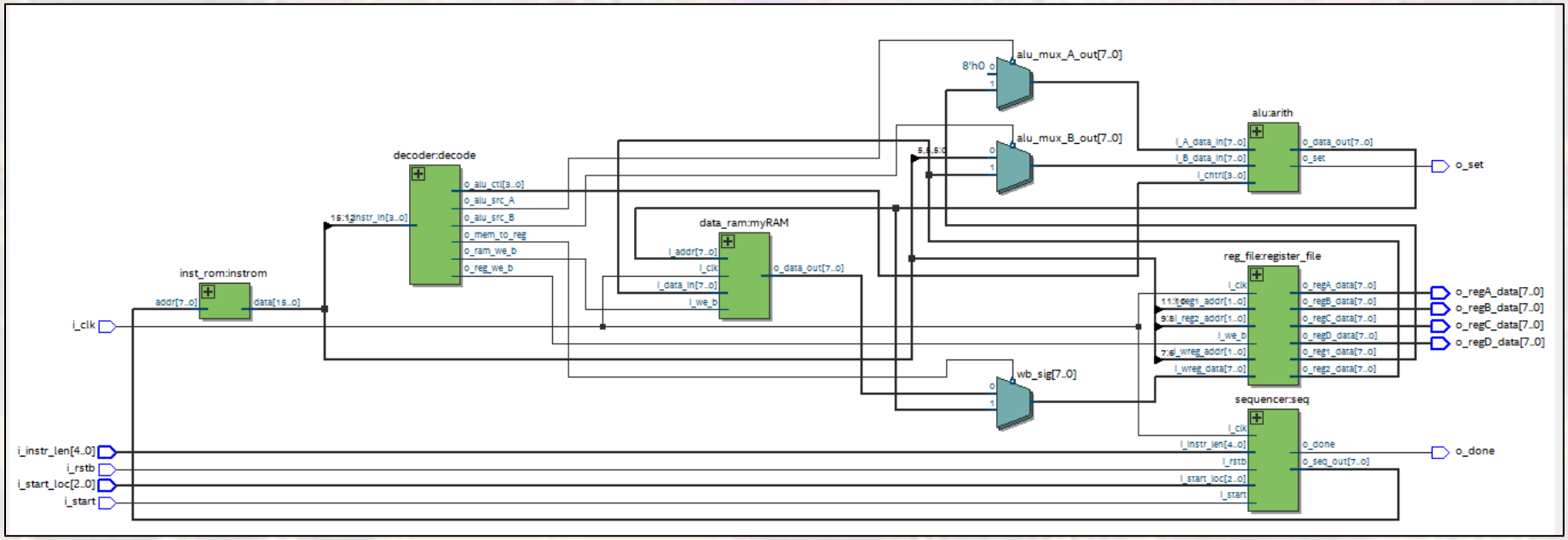
MidTerm Project Notes

- Decoder Simulation



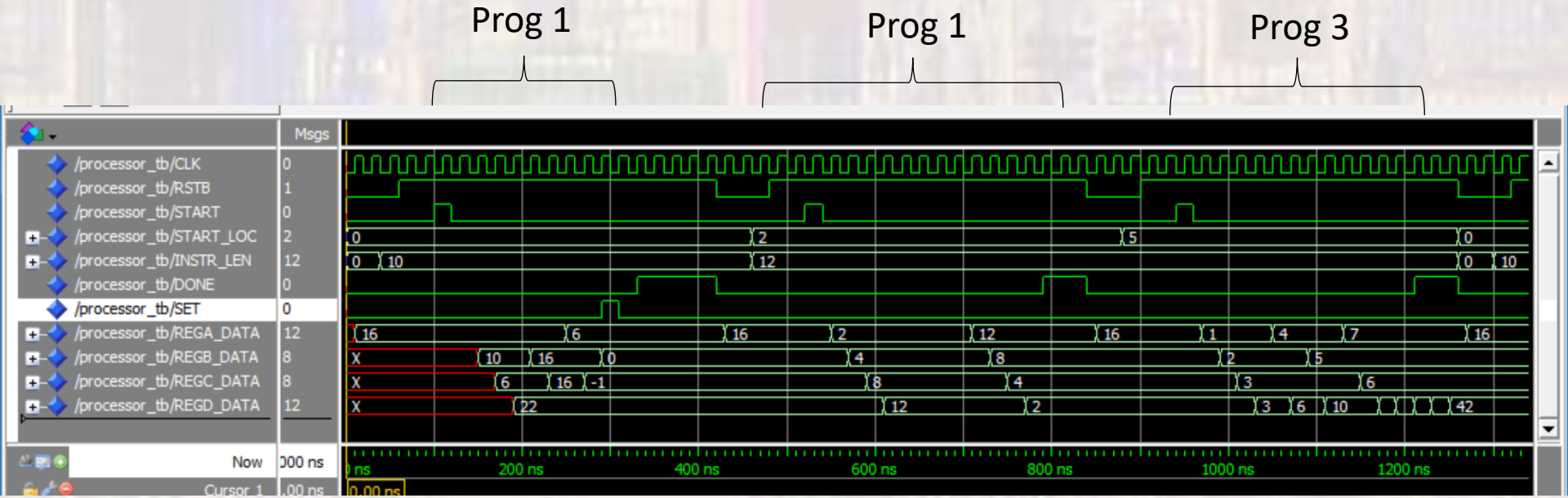
MidTerm Project Notes

- Processor RTL view



MidTerm Project Notes

- Processor Simulation



MidTerm Project Notes

- DE10 RTL view