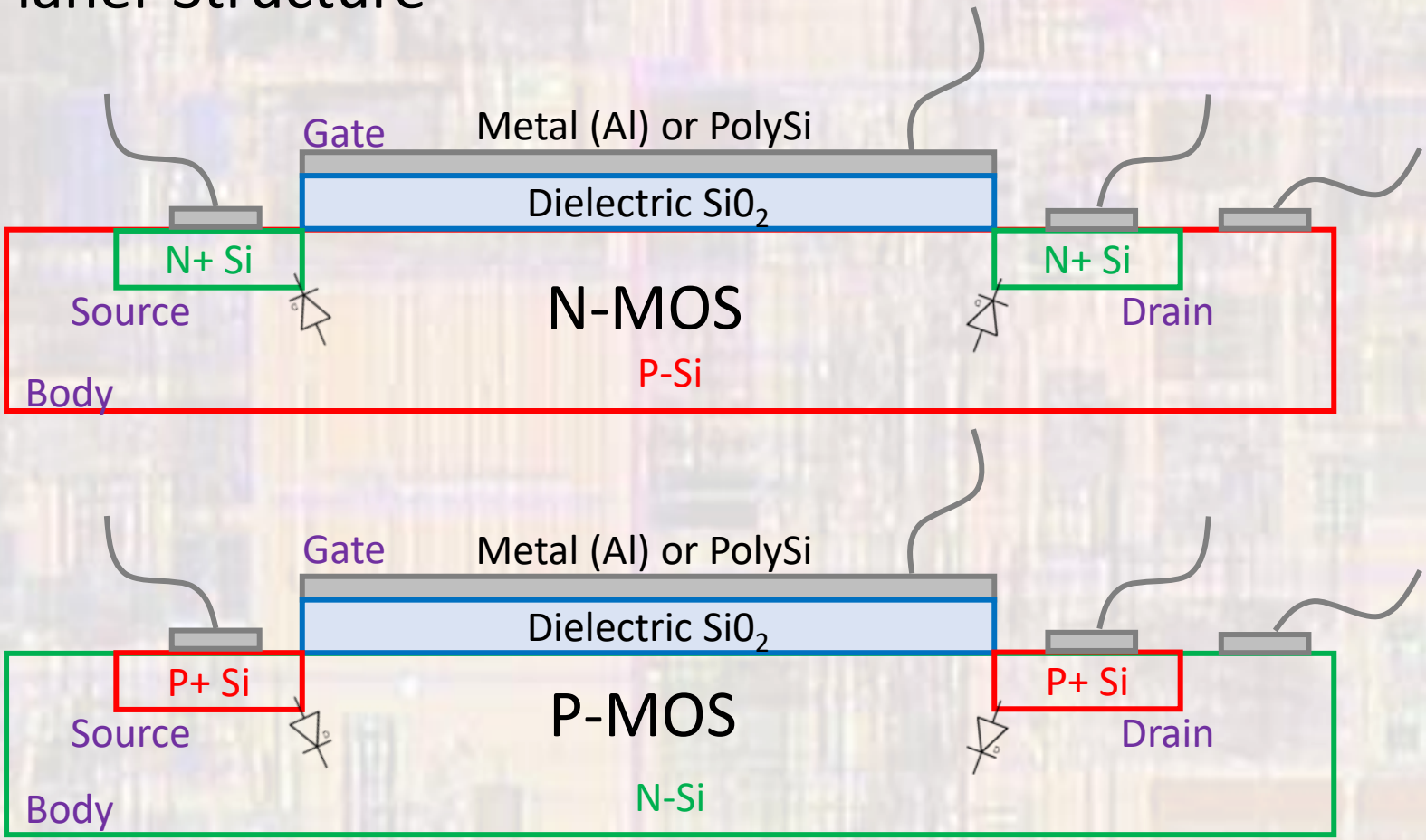
Metal Oxide Semiconductor Enhancement Mode Transistor

Last updated 12/22/23

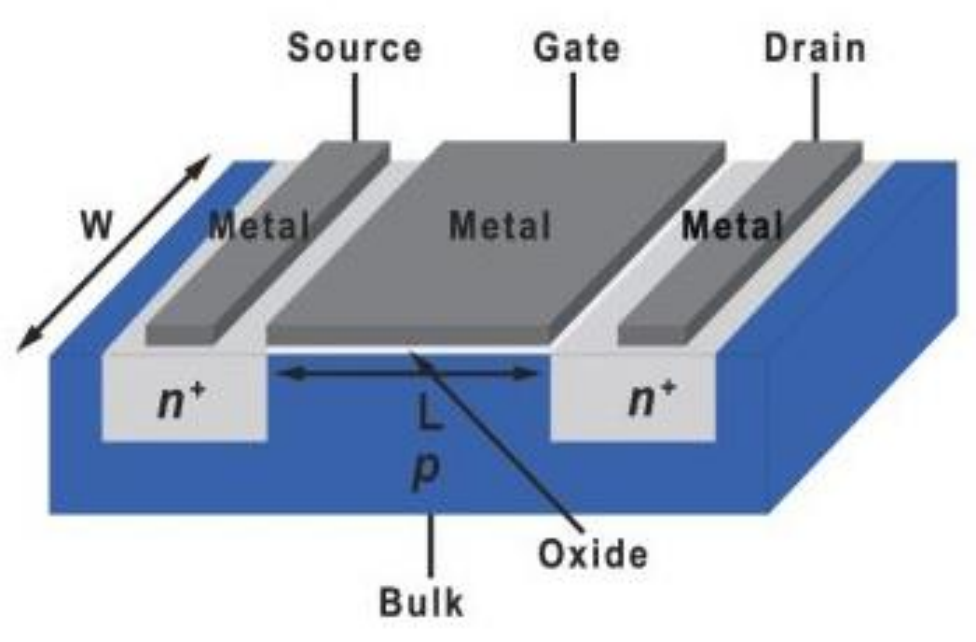
MOS Enhancement Mode Transistor

- Planer Structure



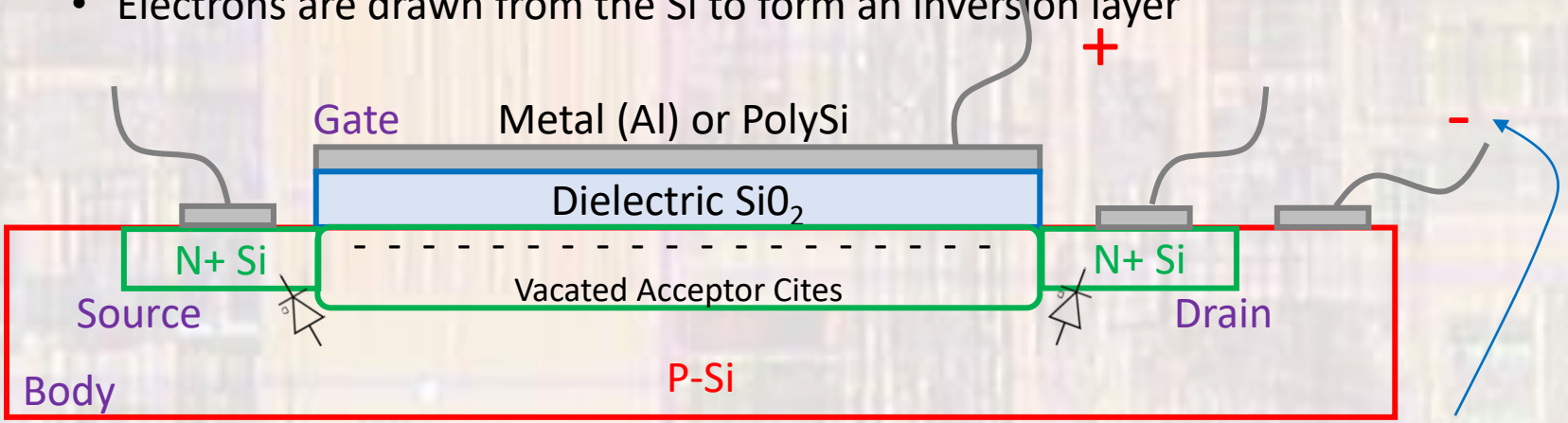
MOS Enhancement Mode Transistor

- Planer Structure
  - W – width – breadth of region for carriers to transit from Source to Drain
  - L – length – distance a carrier must travel to transit from Source to Drain



MOS Enhancement Mode Transistor

- Planer N-MOS Operation
  - Large Positive Gate Bias
    - Depletion region is formed
      - Mobile holes pushed away (region is depleted of holes)
      - Net negative (fixed) charge left behind
      - Electrons are drawn from the Si to form an inversion layer

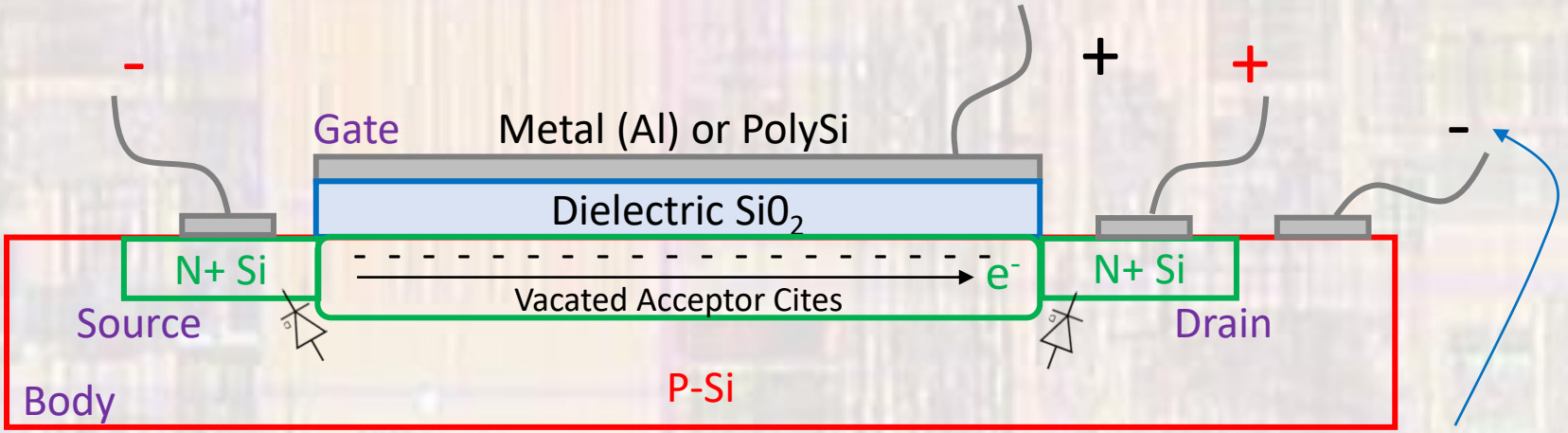


A channel is formed from Source to Drain
Electrons can flow through this channel

Body tied to 'gnd' to ensure the S/D diodes are reverse biased

MOS Enhancement Mode Transistor

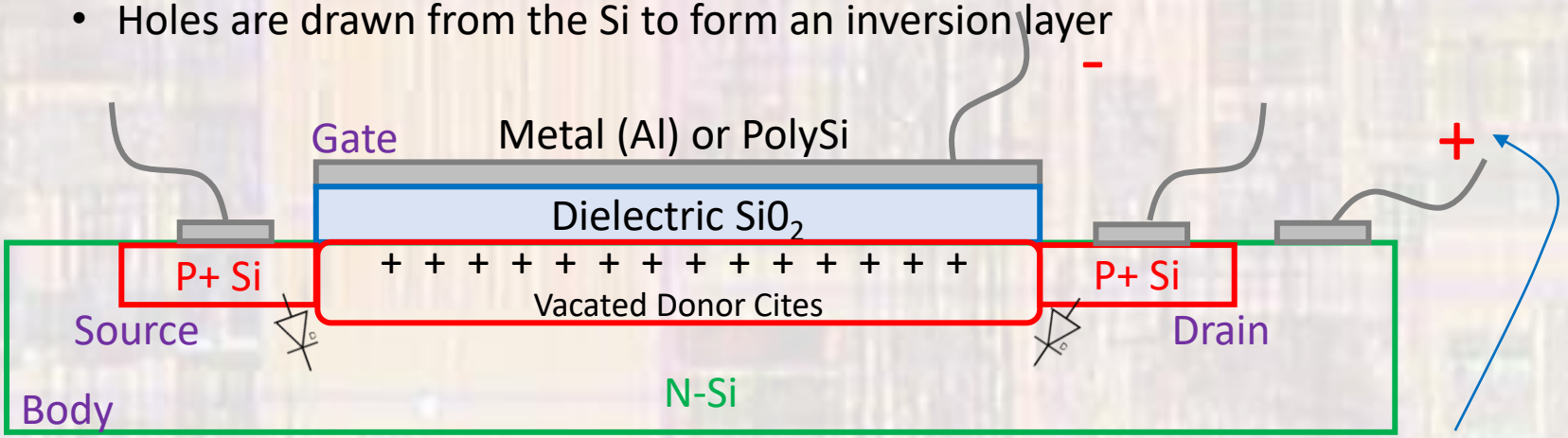
- Planer N-MOS Operation
  - Large Positive Gate Bias + Positive Bias from Drain to Source
    - Electrons move from Source to Drain
    - Current flows from Drain to Source



Body tied to 'gnd' to ensure the S/D diodes are reverse biased

MOS Enhancement Mode Transistor

- Planer P-MOS Operation
  - Large Negative Gate Bias
    - Depletion region is formed
      - Mobile electrons pushed away (region is depleted of electrons)
      - Net positive (fixed) charge left behind
      - Holes are drawn from the Si to form an inversion layer

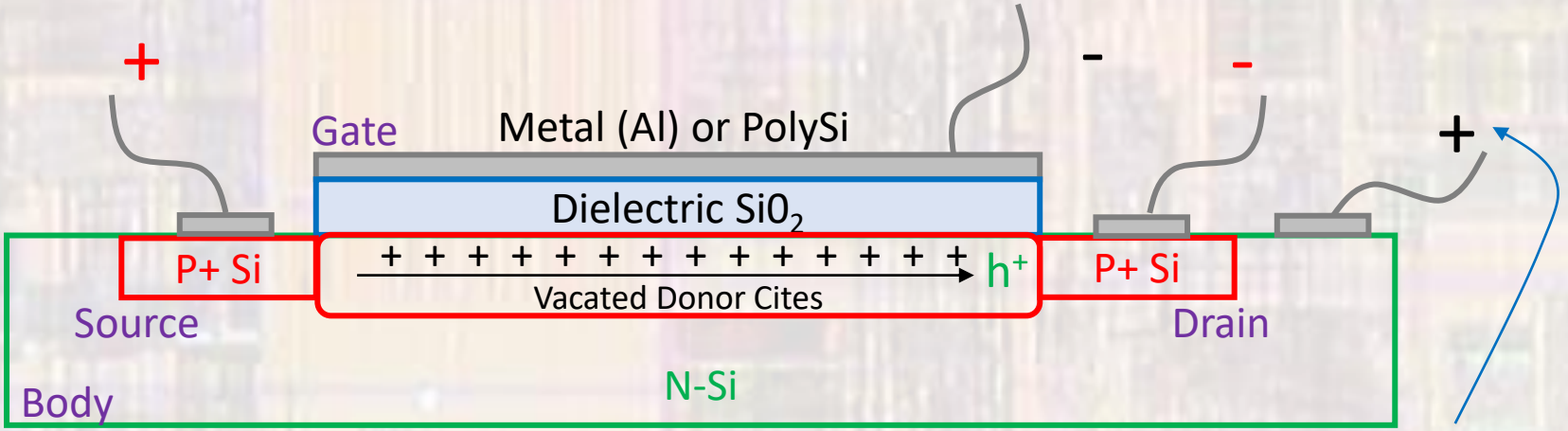


A channel is formed from Source to Drain
Holes can flow through this channel

Body tied to 'Vdd' to ensure the S/D diodes are reverse biased

MOS Enhancement Mode Transistor

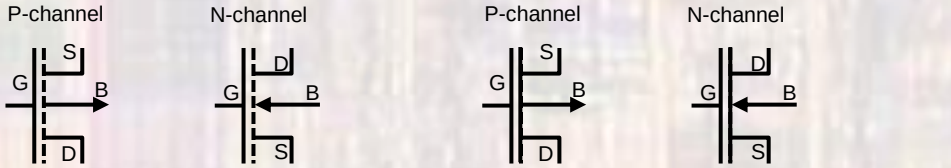
- Planer P-MOS Operation
  - Large Negative Gate Bias + Positive Bias from Source to Drain
    - Holes move from Source to Drain
    - Current flows from Source to Drain



Body tied to 'Vdd' to ensure the S/D diodes are reverse biased

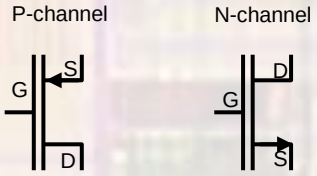
MOS Enhancement Mode Transistor

- Planer Enhancement Mode Transistors
  - A bias is required to form the channel
  - 4-terminal symbol

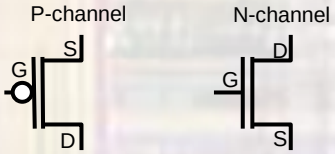


Note – almost all N-MOS and P-MOS devices used today are enhancement mode – so the dashed line is omitted

  - In digital applications the Body is typically tied to
    - Vdd for P-MOS
    - Gnd for N-MOS
    - 3-terminal symbol



  - Simplified logic symbols



MOS Enhancement Mode Transistor

- Planer Enhancement Mode Transistor Parameters
  - W – width of the transistor
  - L – length of the transistor (S to D)
  - V_{th} – threshold voltage (inversion layer formed)
  - Kn, Kp – conduction parameter

$$K_n = \frac{W \mu_n C_{ox}}{2L} \qquad K_p = \frac{W \mu_p C_{ox}}{2L}$$

$$K_n = \frac{k'_n}{2}\frac{W}{L} \qquad K_p = \frac{k'_p}{2}\frac{W}{L}$$

$$k'_n = \mu_n C_{ox} \qquad k'_p = \mu_p C_{ox}$$

$\mu_n \sim 3$ x μ_p, C_{ox} fixed for a given semiconductor process