NIOS V Processor

Last updated 7/16/26

NIOS V Processor

- FPGA Embedded processors
  - Soft Core
    - Core is built out of pre-configured blocks
    - The blocks are built out of standard FPGA fabric
    - Cores can be customized
    - Limited in frequency
  - Hard core
    - Core is a separate part of the chip
      - Not using the standard FPGA fabric
    - Fixed configuration
    - Physically optimized for performance
    - MAX10 does not have an embedded hard core processor

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NIOS V Processor

- RISC-V Processor
  - Pronounced "risk-five“
  - Open-source Instruction Set Architecture (ISA)
    - Allows companies and developers to design and manufacture custom microprocessors without paying royalties or licensing fees
  - Developed originally in 2010 at UC Berkeley
  - The standard is now governed by the Swiss-based non-profit RISC-V International
  - Features a small, simple core instruction set accompanied by optional extensions
    - vector processing, cryptography, AI acceleration, …
  - Growing in popularity but still small compared to Intel and ARM platforms

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NIOS V Processor

- Nios V Processor
  - Altera's next-generation soft-core processor
  - Built on the RISC-V architecture
  - 32-bit implementation
- Three variants
  - **Nios V/c:** A compact microcontroller variant appropriate for small, area-constrained applications (no interrupt support)
  - **Nios V/m:** A standard microcontroller core that supports pipelined or non-pipelined modes and Error Correction Code (ECC)
  - **Nios V/g:** A general-purpose processor with higher performance, instruction and data caches, tightly coupled memory, and custom instruction logic for accelerating time-critical algorithms

NIOS V Processor

- Footprint
  - **Nios V/c:**
    - 100,000 Bytes of memory
    - SYS ID, 8bit PIO
      → uses 2% of available LEs
      → uses 48% of available memory
  - **Nios V/m:**
    - Pipelined but no ECC
    - 100,000 Bytes of memory
    - JTAG UART, SYS ID, Timer, 8bit PIO
      → uses 11% of available LEs
      → uses 48% of available memory
  - **Nios V/g:**
    - Default configuration
    - 100,000 Bytes of memory
    - JTAG UART, SYS ID, Timer, 8bit PIO
      → uses 18% of available LEs
      → uses 52% of available memory

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NIOS V Processor

- Performance
  - NIOS V/m
    - Pipelined

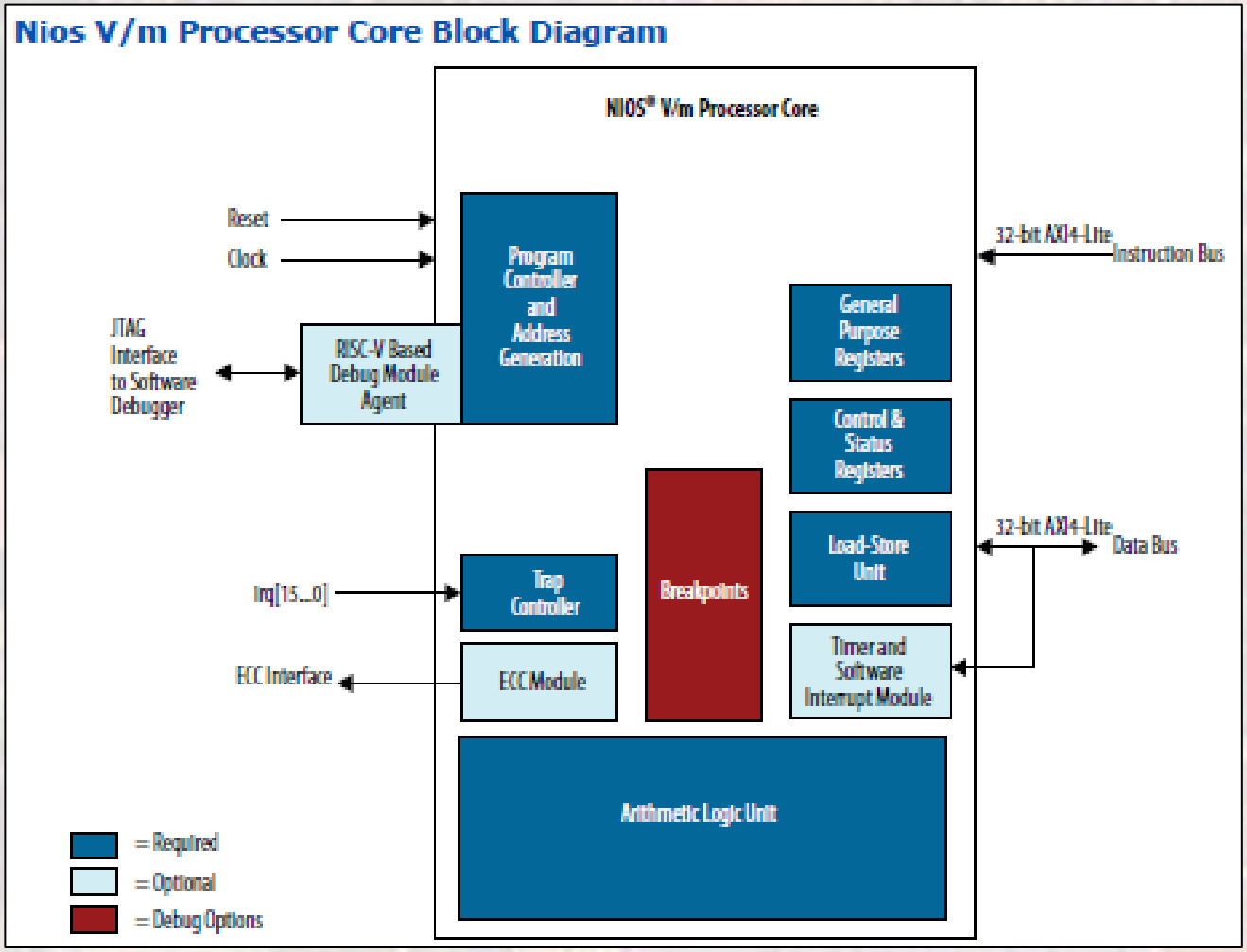
Quartus Prime Edition	FPGA Used	OPN	fMAX (MHz)	Logic Size	Architecture Performance	
					DMIPS/MHz Ratio	CoreMark/MHz Ratio
	MAX 10	10M50DAF484C7G	123	2864 LE	0.63	0.49

Stage	Denotation	Function
F	Instruction fetch	• PC+4 calculation • Next instruction fetch • Pre-decode for register file read
D	Instruction decode	• Decode the instruction • Register file read data available • Hazard resolution and data forwarding
E	Instruction execute	• ALU operations • Memory address calculation • Branch resolution • CSR read/write
M	Memory	• Memory and multicycle operations • Register file write • Branch redirection
W	Write back	• Facilitates data dependency resolution by providing general-purpose register value.

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NIOS V Processor

- NIOS V/m System



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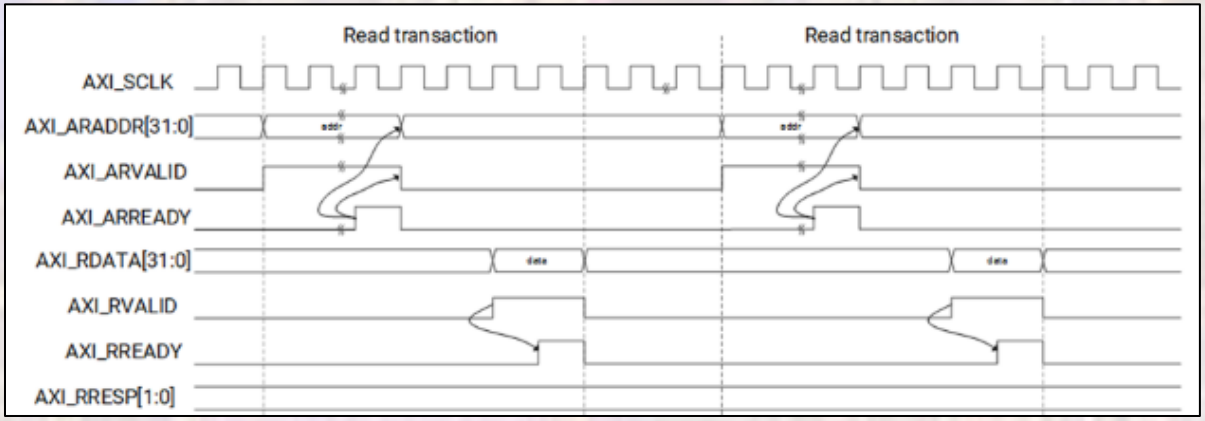
NIOS V Processor

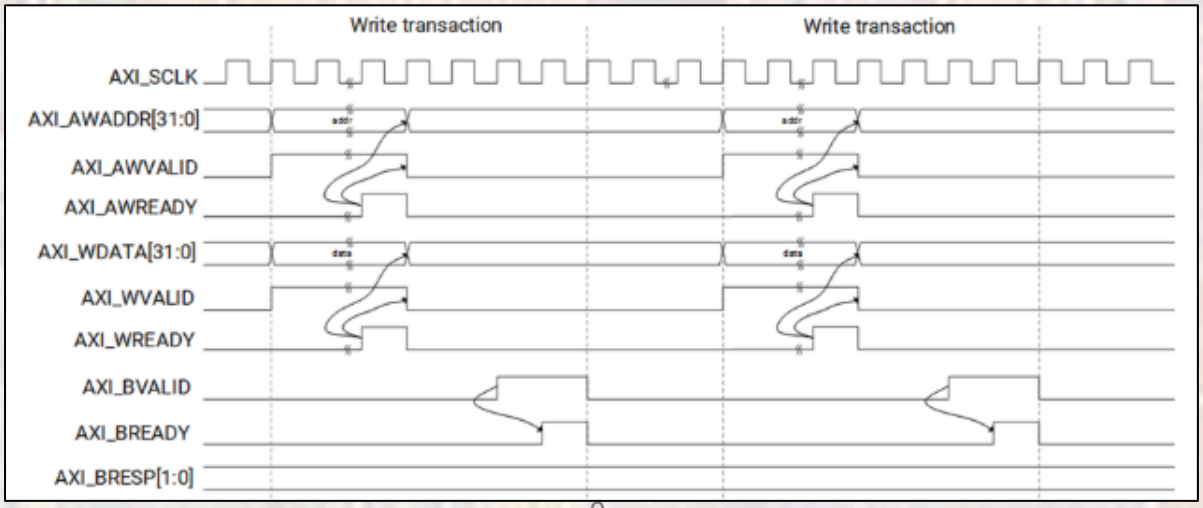
- NIOS V Interconnect Fabric
  - Uses the ARM AXI-Lite interconnect fabric
- Altera University IP Interconnect Fabric
  - Uses the legacy NIOS II interconnect fabric – 2 types
    - Memory Mapped
      - Master and Slave
    - Streaming
      - Non-packet and Packet
- The platform designer system automatically add interfaces to bridge the two interconnect fabrics

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NIOS V Processor

- NIOS V Interconnect Fabric
  - AXI-Lite

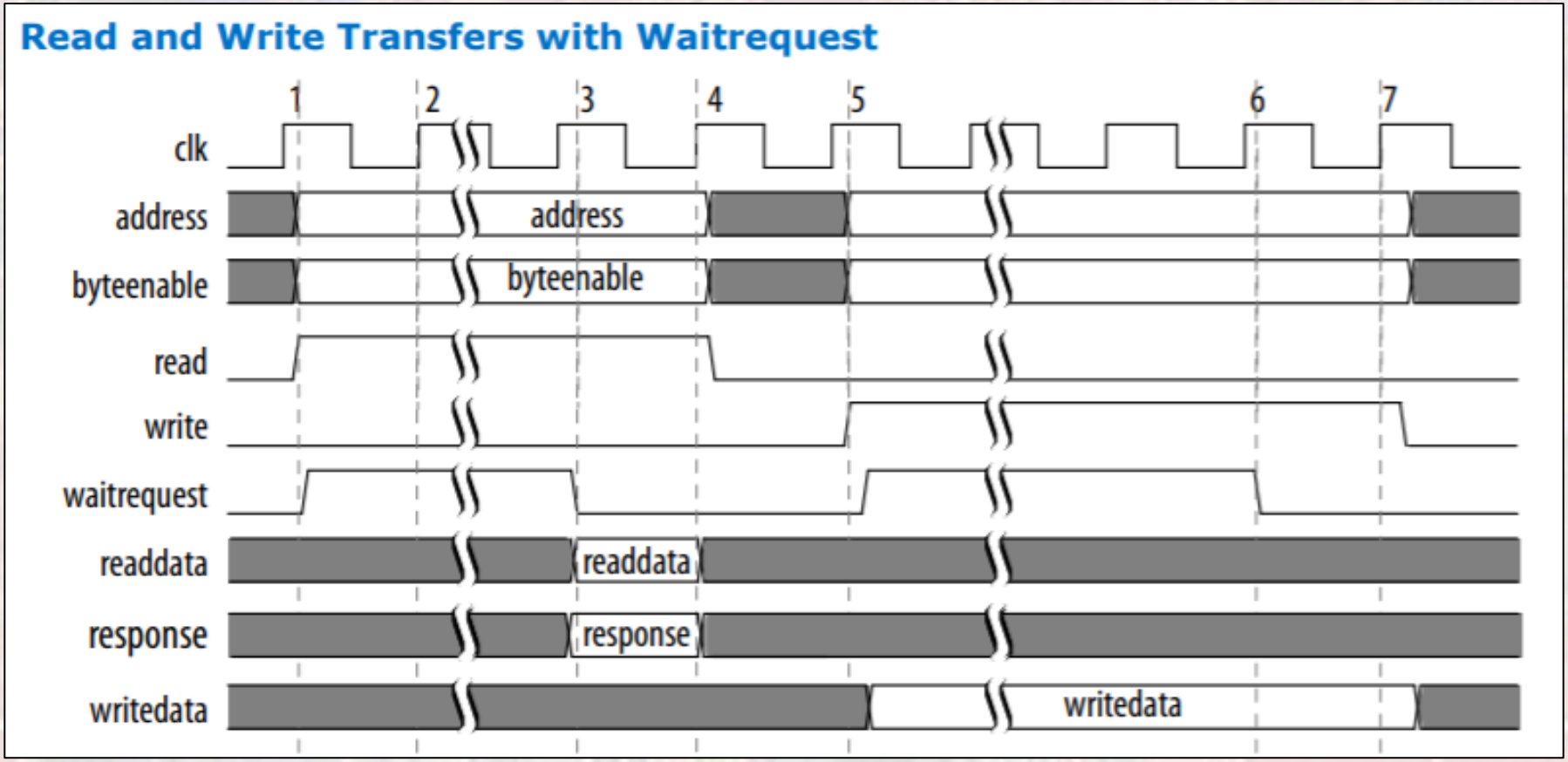




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NIOS V Processor

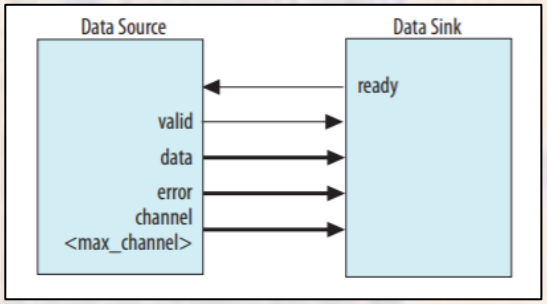
- NIOS II Interconnect Fabric
  - Memory mapped interface (master and slave)

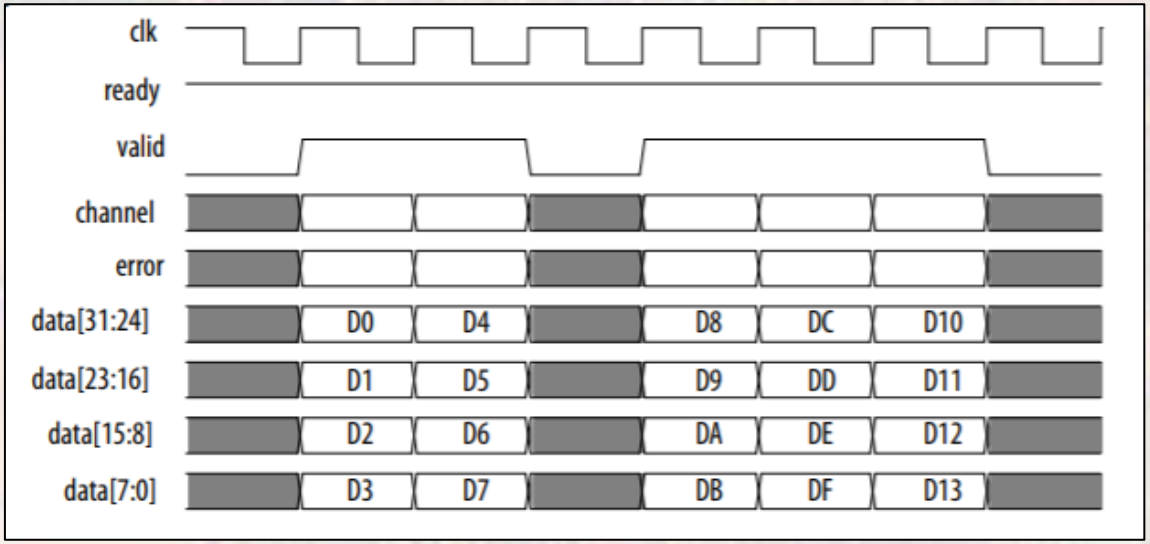


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NIOS V Processor

- NIOS II Interconnect Fabric
  - Streaming interface – non-packet

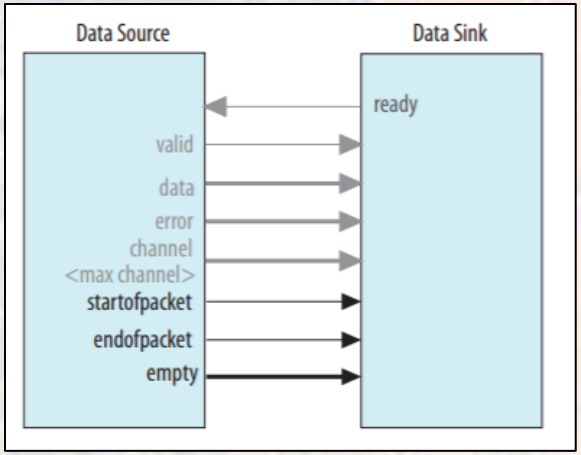


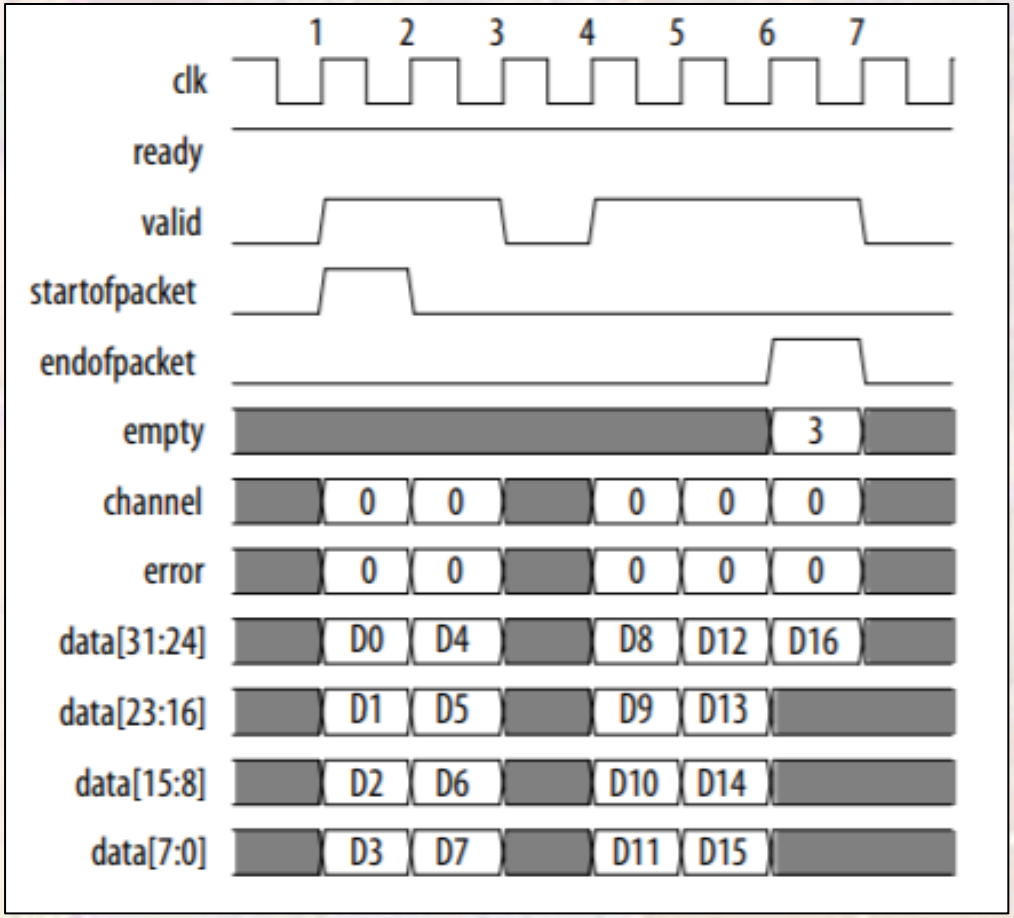


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NIOS V Processor

- NIOS II Interconnect Fabric
  - Streaming interface – packet based





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