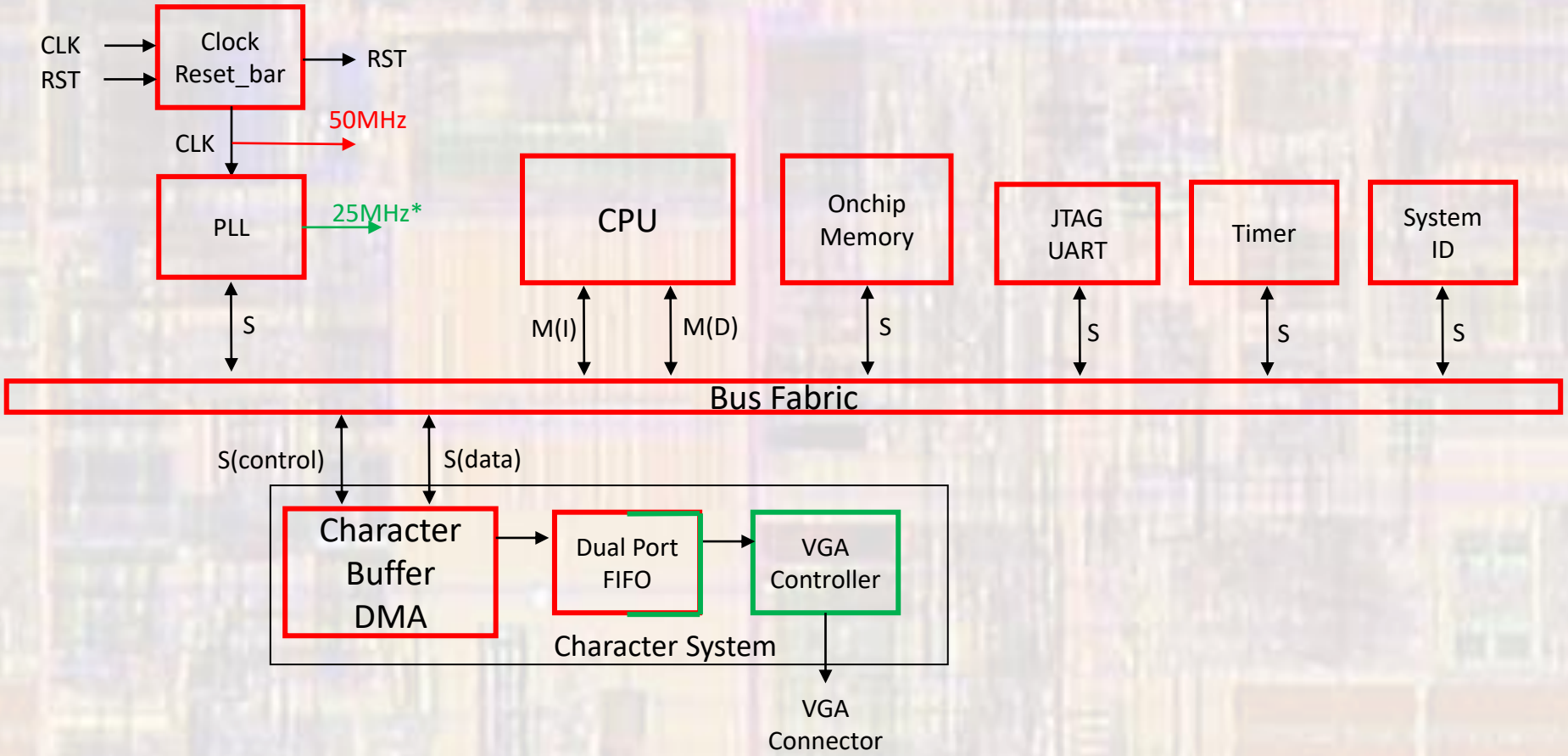
NIOS Character HW

Last updated 7/20/23

NIOS II Character Display - HW

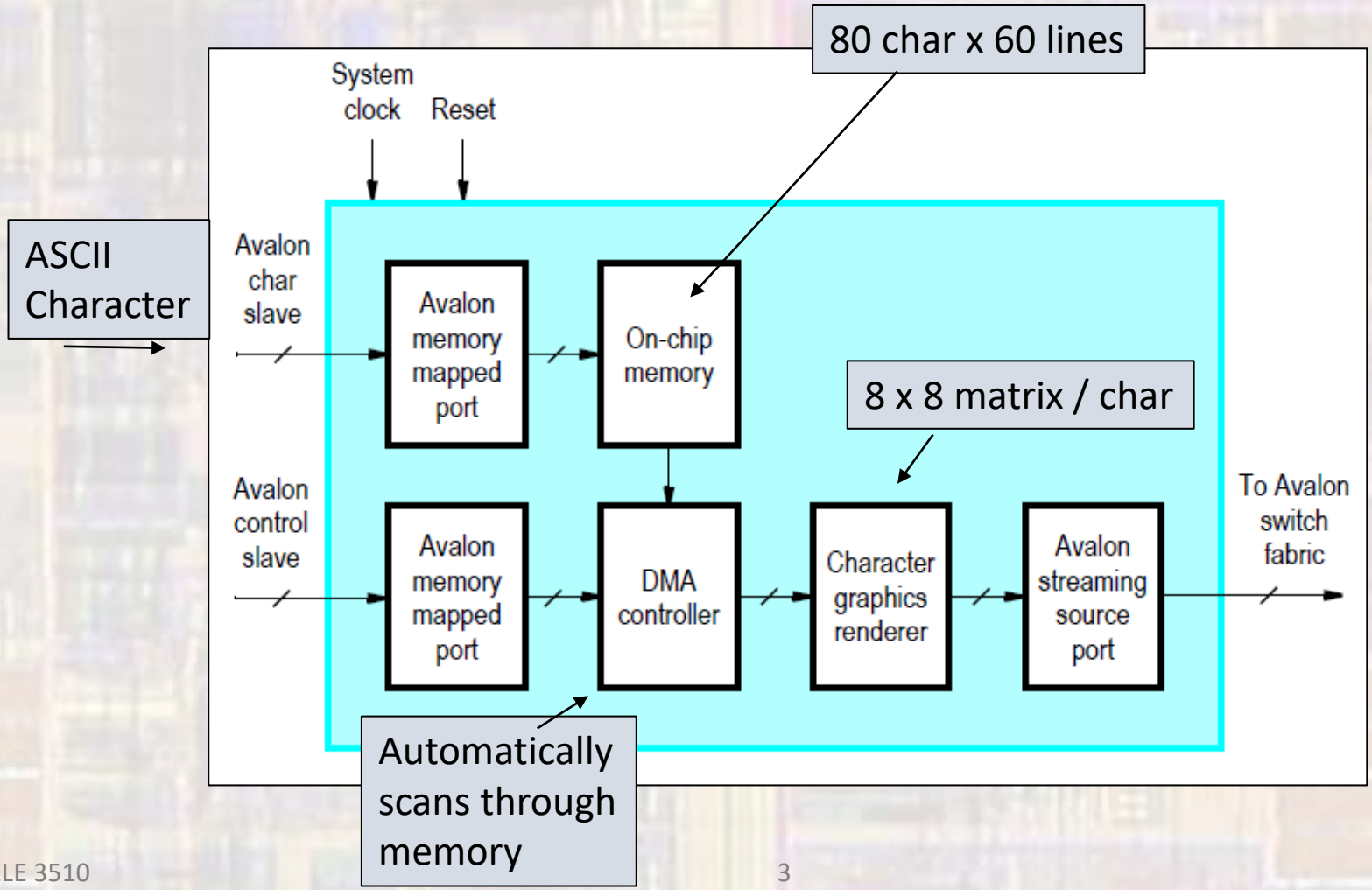
- Character Buffer Block Diagram



25MHz** - VGA clk

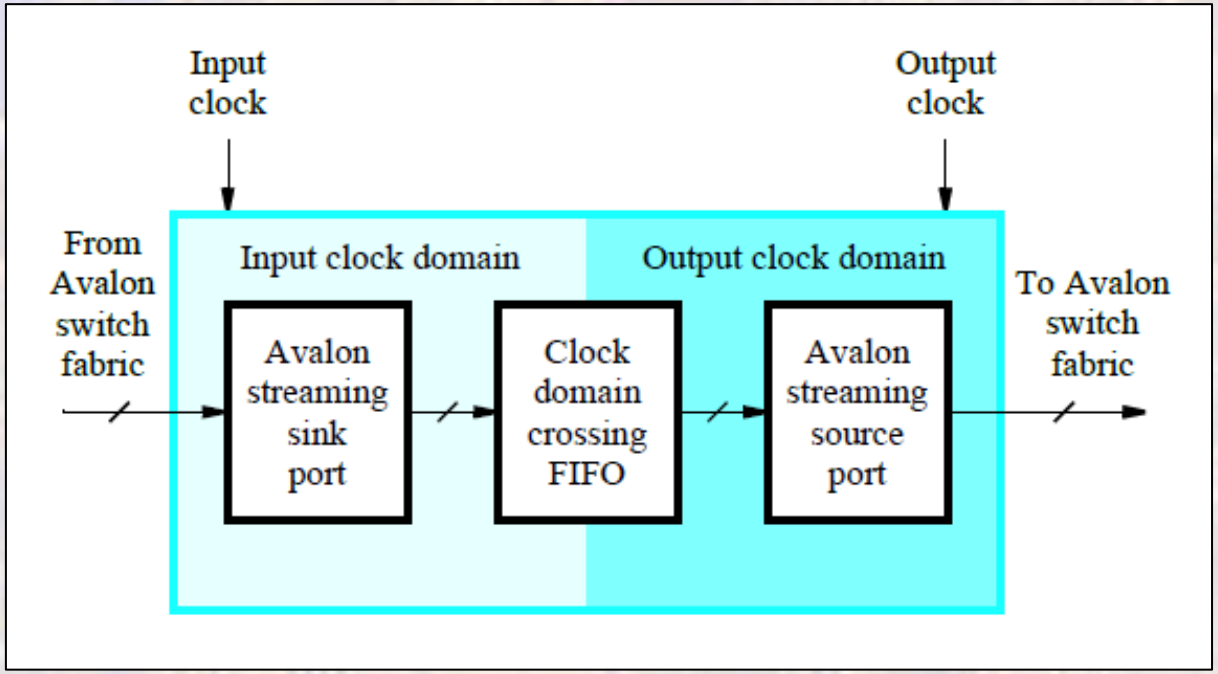
NIOS II Character Display - HW

- Character Buffer Block



NIOS II Character Display - HW

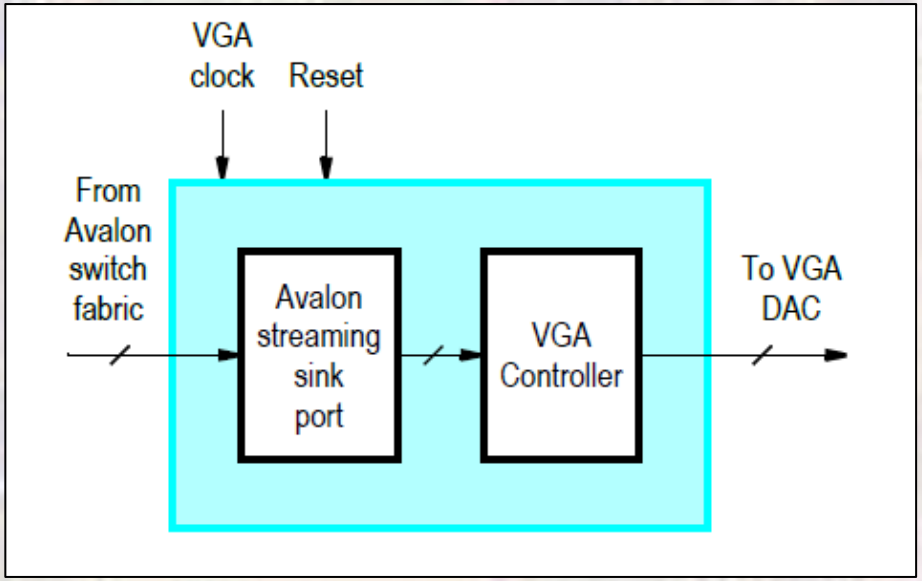
- Dual Clock FIFO



Allows different incoming and outgoing data rates

NIOS II Character Display - HW

- VGA Controller Block

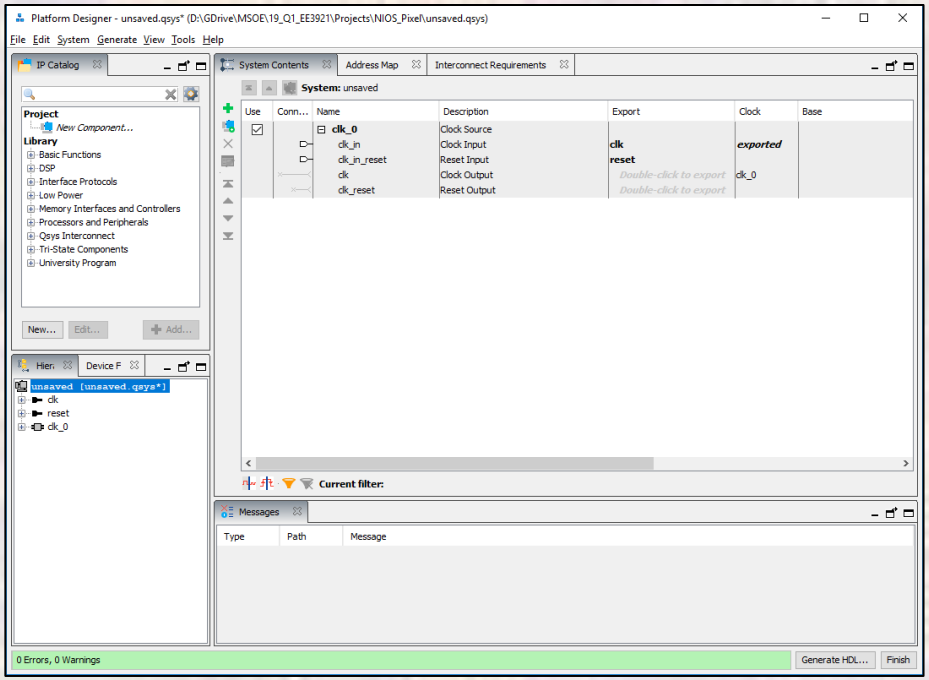


Creates and drives the required VGA signals

NIOS II Character Display - HW

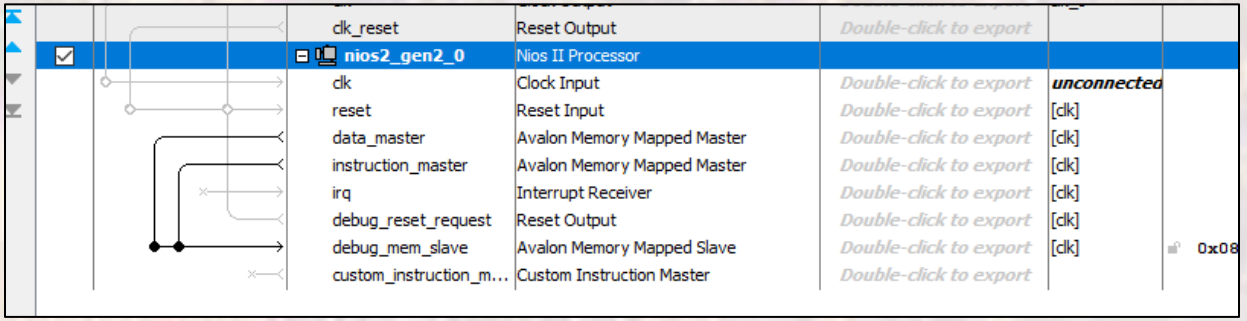
- Create a new Quartus project
  - Do not select a Simulation Tool in EDA Tool Settings

- Open Tools → Platform Designer



NIOS II Character Display - HW

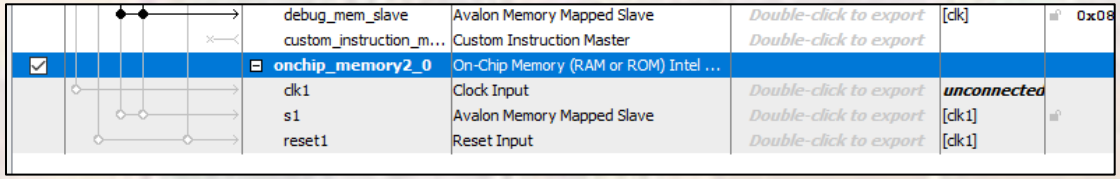
- Add NIOS
  - Processors and Peripherals → Embedded Processors → NIOS II Processor
  - NIOS II/f



- Add On-chip Memory
  - Basic Functions→ On Chip Memory → On Chip Memory (RAM or ROM)…

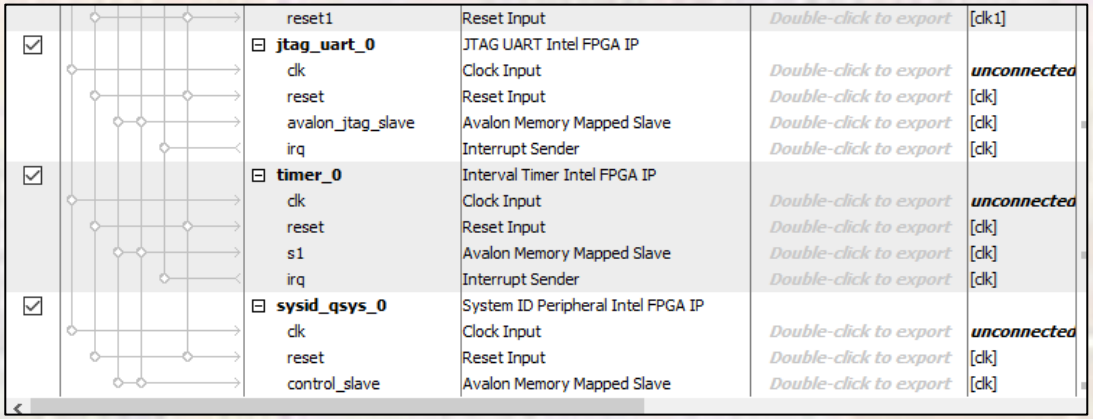
    RAM

    Size = 12,000 bytes



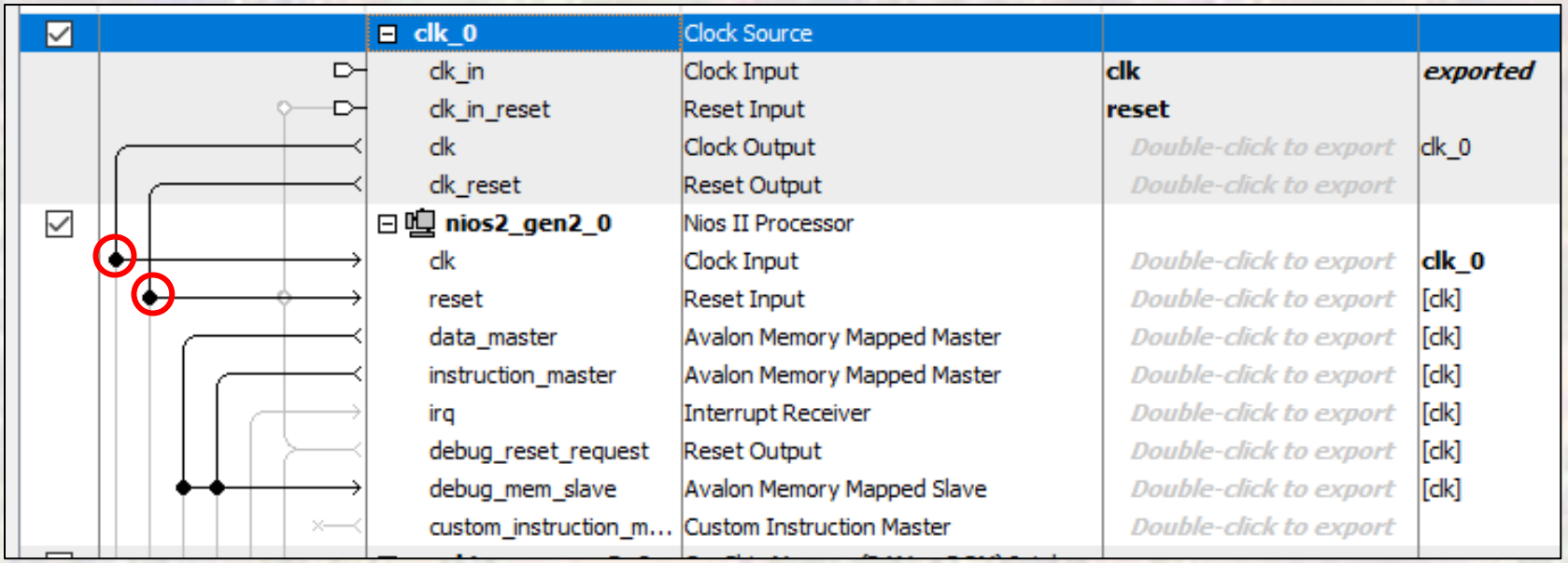
NIOS II Character Display - HW

- Add JTAG
  - Interface Protocols → Serial→ JTAG Uart Intel FPGA IP
- Add Timer
  - Processors and Peripherals → Peripherals → Interval Timer Intel FPGA IP
- Add System ID
  - Basic Functions → Simulation; Debug and Verification → Debug and Performance → System ID Peripheral Intel FPGA IP



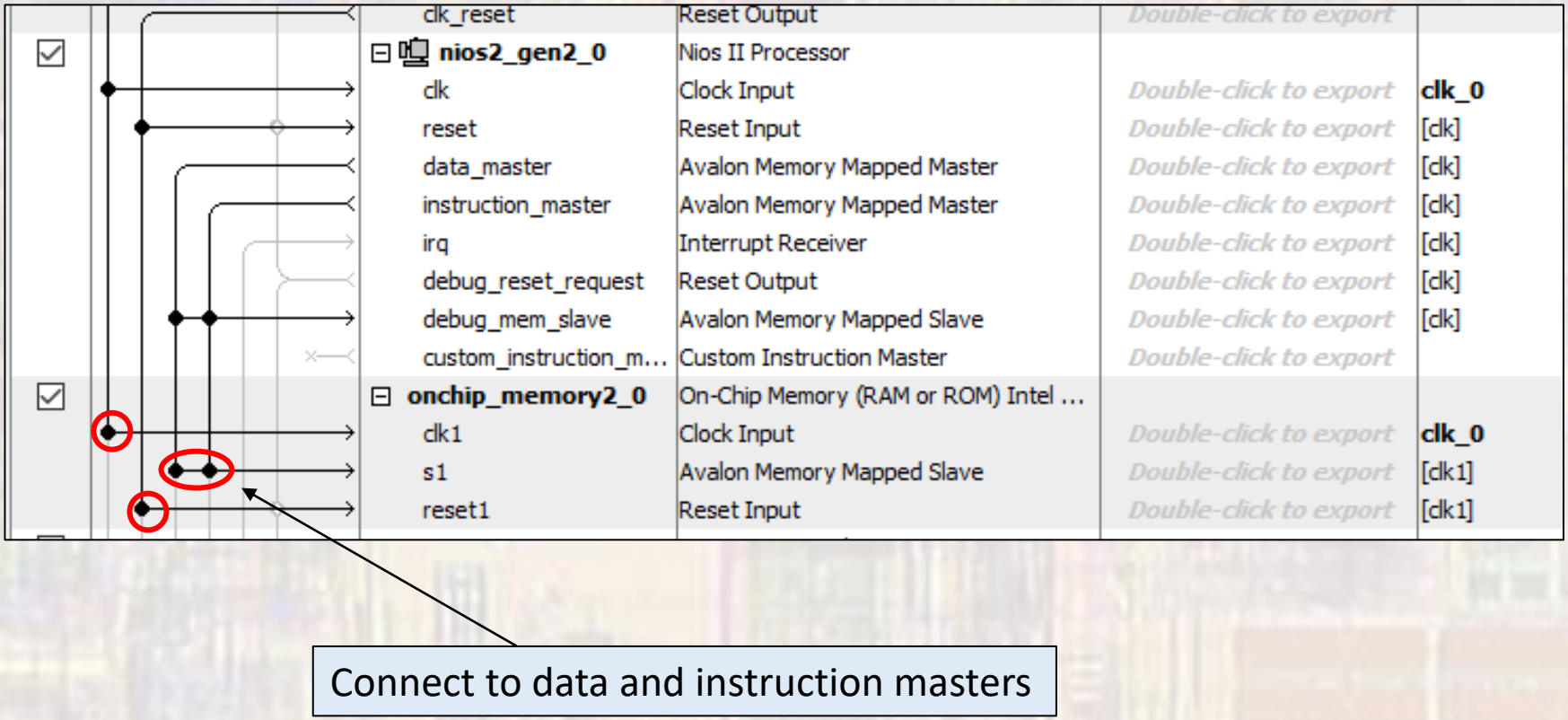
NIOS II Character Display - HW

- Connect up basic NIOS system
  - NIOS Inputs



NIOS II Character Display - HW

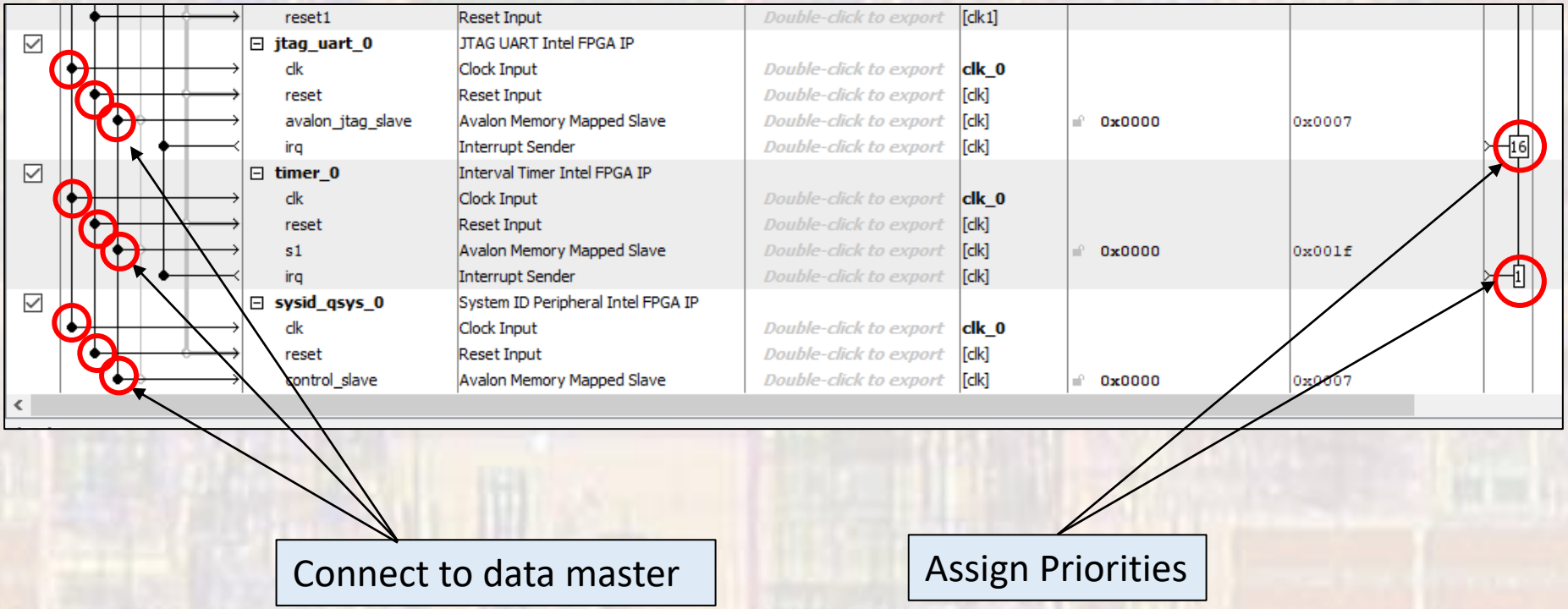
- Connect up basic NIOS system
  - On-chip Memory



Connect to data and instruction masters

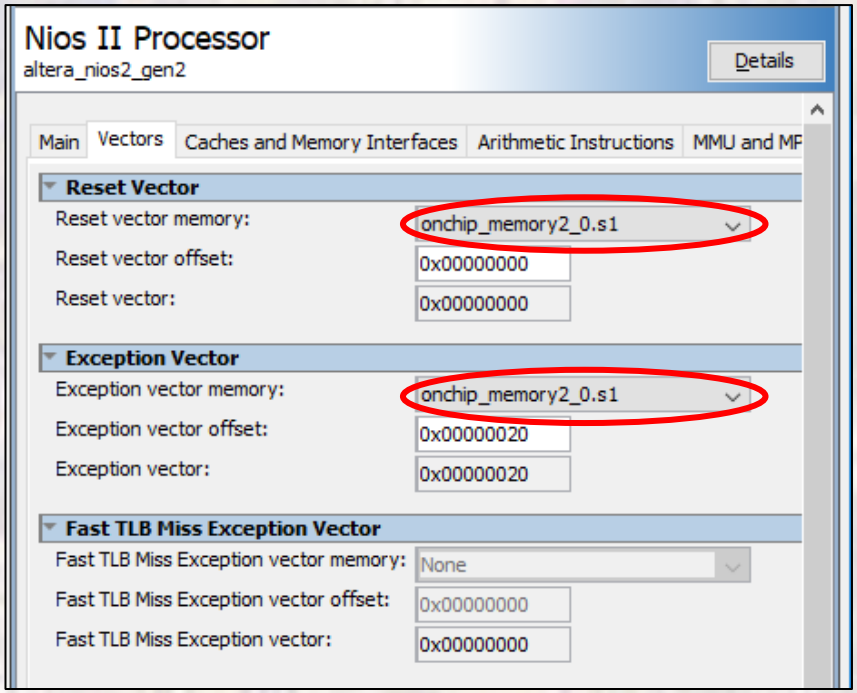
NIOS II Character Display - HW

- Connect up basic NIOS system
  - JTAG, Timer, SysID



NIOS II Character Display - HW

- Connect up basic NIOS system
  - Assign the NIOS II Reset and Exception vectors



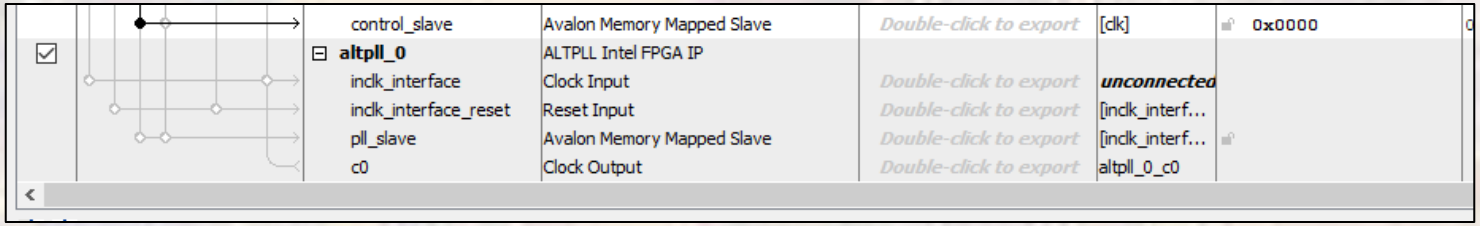
NIOS II Character Display - HW

- Create Character System
  - Add a PLL
    - Basic Functions → Clocks; PLLs and Resets → PLL → ALTPLL Intel FPGA IP

50MHz input clock

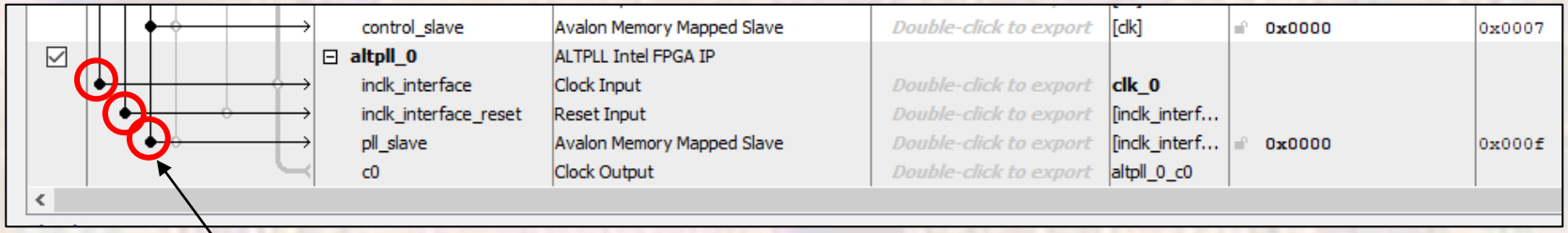
no areset or locked output

c0 → 25MHz : the VGA frequency



NIOS II Character Display - HW

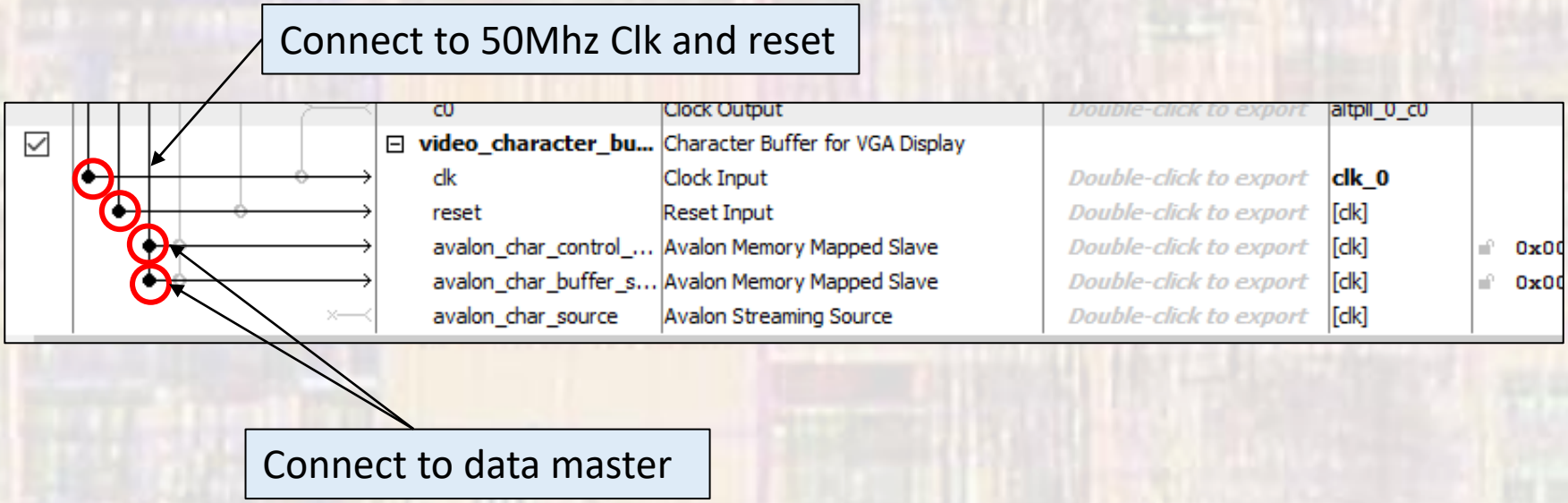
- Create Character System
  - Connect PLL



Connect to the 50MHz Clk, reset and the data master

NIOS II Character Display - HW

- Create Character System
  - Character Buffer
    - University Program → Audio and Video → Video → Character Buffer for VGA Display



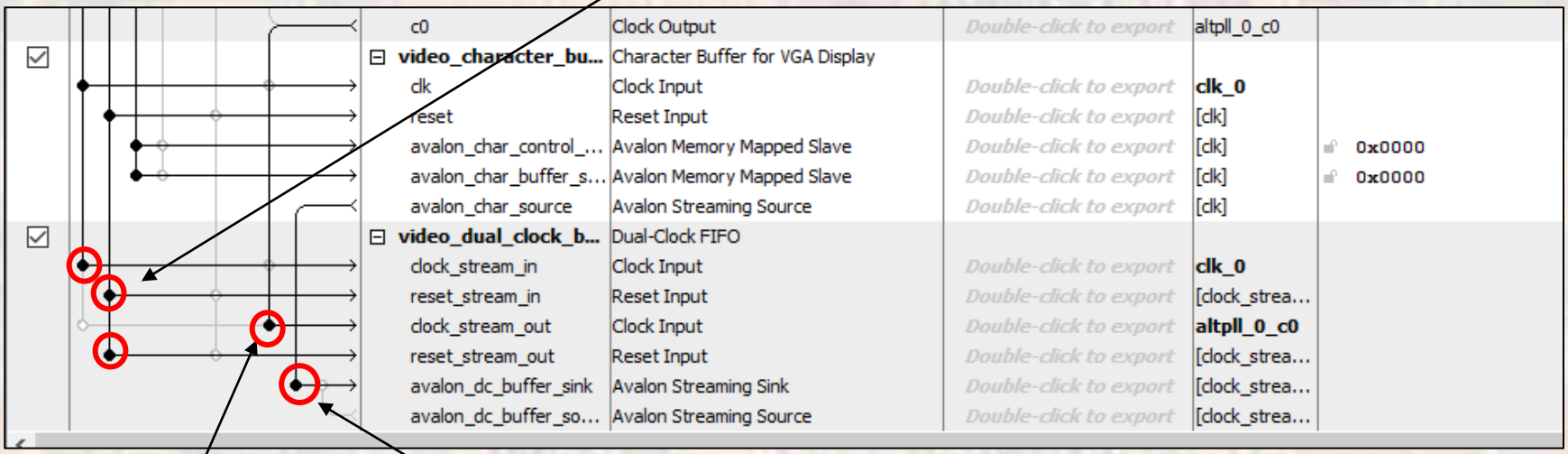
NIOS II Character Display - HW

- Create Character System
  - Dual Clock FIFO
    - University Program → Audio and Video → Video → Dual Clock FIFO

      Color Bits – 10

      Color Planes - 3

Connect to 50Mhz Clk and reset



Connect to c0
VGA – 25MHz

Connect to video character buffer streaming source

NIOS II Character Display - HW

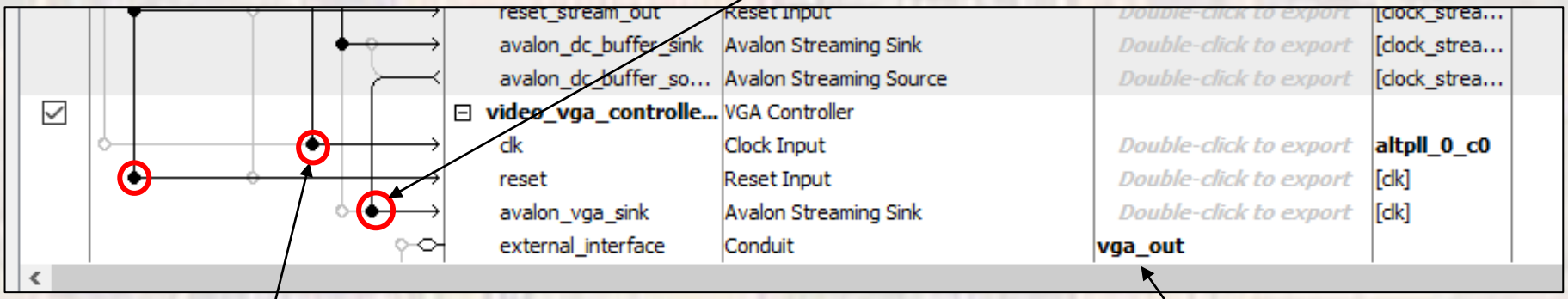
- Create Character System
  - VGA Controller
    - University Program → Audio and Video → Video → VGA Controller

      DE10-Lite

      VGA Connector

      VGA 640x480

Connect to dual_clock_buffer streaming source



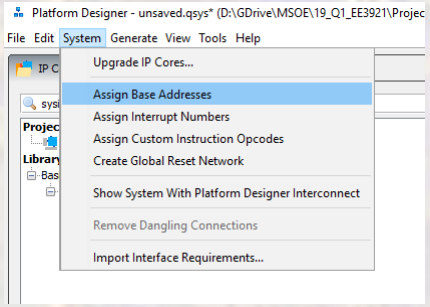
Export and rename

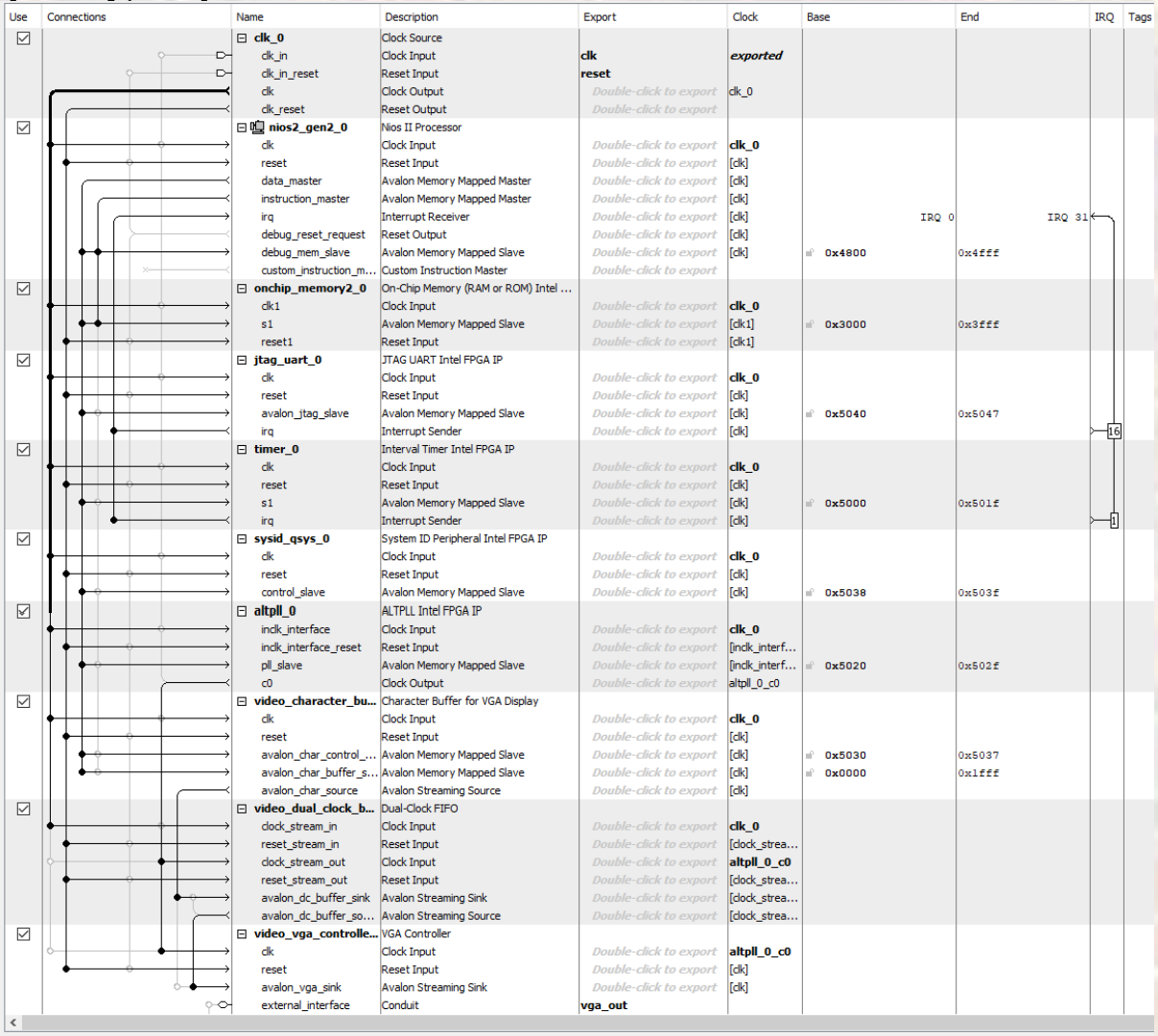
Connect to c0
VGA – 25MHz

NIOS II Character Display - HW

- Create Charac

Assign Base Addresses





NIOS II Character Display - HW

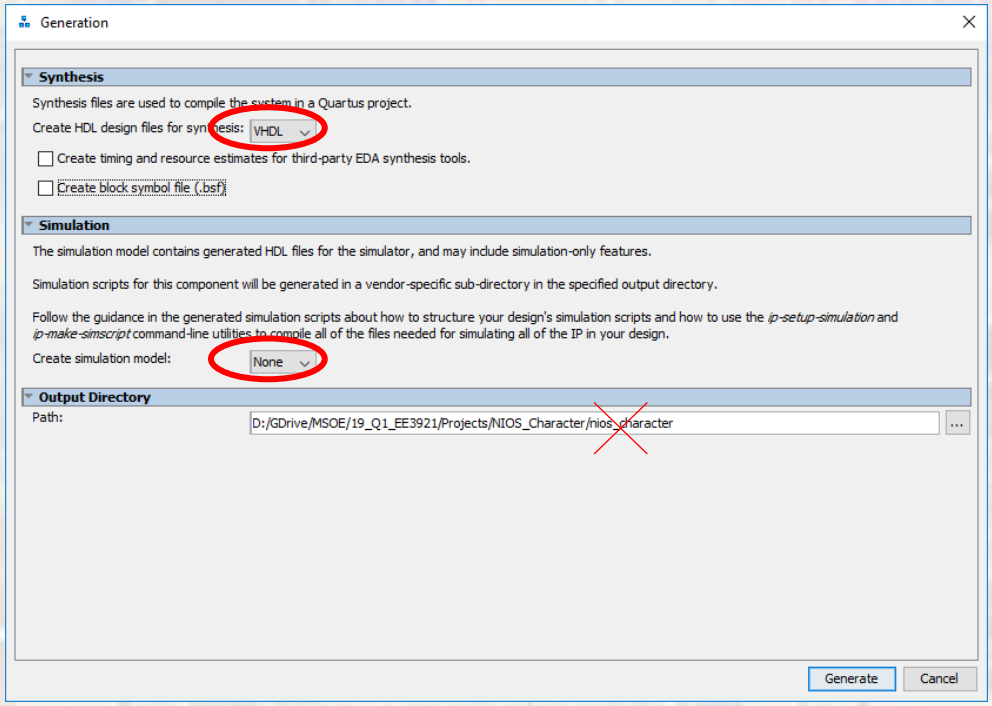
- Create Character System
  - Check for errors

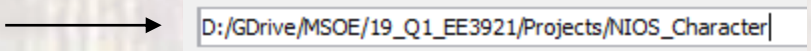
Messages

Type	Path	Message
	5 Info Messages	
	nios_character.jtag_uart_0	JTAG UART IP input clock need to be at least double (2x) the operating frequency of JTAG TCK on board
	nios_character.sysid_qsys_0	System ID is not assigned automatically. Edit the System ID parameter to provide a unique ID
	nios_character.sysid_qsys_0	Time stamp will be automatically updated when this component is generated.
	nios_character.video_character_buffer_with_dma_0	Character Resolution: 80 x 60
	nios_character.video_vga_controller_0	Video Output Stream: Format: 640 x 480 with Color: 10 (bits) x 3 (planes) converted to 4 (bits) per color plane

NIOS II Character Display - HW

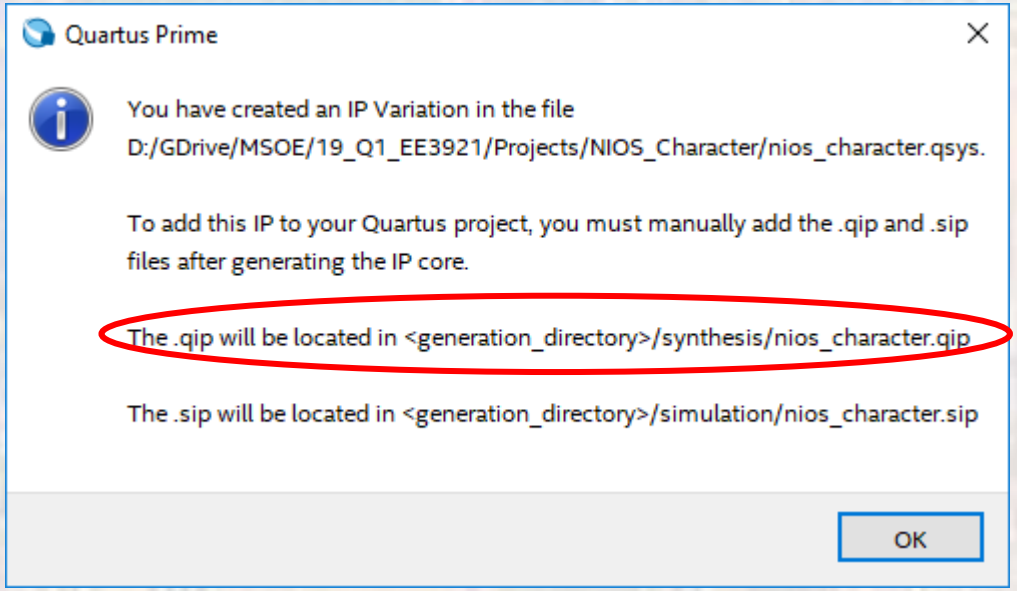
- Create Character System
  - Save the Platform Designer system
  - Generate the Platform Designer system
    - The first time you generate you must delete the last directory in the path – don't use the '…'





NIOS II Character Display - HW

- Create Character System
  - Add the .qip file to the project



NIOS II Character Display - HW

- Create DE10 Design
  - Instantiate into a VHDL file
    - Open a new VHDL design
    - In Platform Designer: Generate → Show Instantiation Template
    - Copy and Paste into the new design where appropriate

```
component nios_char is
   port (
      clk_clk               : in  std_logic                    := 'X'; -- clk
      reset_reset_n :     in  std_logic                    := 'X'; -- reset_n
      vga_out_CLK       : out std_logic;                          -- CLK
      vga_out_HS        : out std_logic;                          -- HS
      vga_out_VS        : out std_logic;                          -- VS
      vga_out_BLANK  : out std_logic;                          -- BLANK
      vga_out_SYNC    : out std_logic;                          -- SYNC
      vga_out_R         : out std_logic_vector(3 downto 0);       -- R
      vga_out_G        : out std_logic_vector(3 downto 0);       -- G
      vga_out_B        : out std_logic_vector(3 downto 0)        -- B
   );
end component nios_char;
```

```
u0 : component nios_char
      port map (
         clk_clk              => CONNECTED_TO_clk_clk,      --    clk.clk
         reset_reset_n     => CONNECTED_TO_reset_reset_n, --  reset.reset_n
         vga_out_CLK       => CONNECTED_TO_vga_out_CLK,   -- vga_out.CLK
         vga_out_HS        => CONNECTED_TO_vga_out_HS,    --       .HS
         vga_out_VS        => CONNECTED_TO_vga_out_VS,    --       .VS
         vga_out_BLANK   => CONNECTED_TO_vga_out_BLANK, --       .BLANK
         vga_out_SYNC     => CONNECTED_TO_vga_out_SYNC,  --       .SYNC
         vga_out_R         => CONNECTED_TO_vga_out_R,     --       .R
         vga_out_G         => CONNECTED_TO_vga_out_G,     --       .G
         vga_out_B         => CONNECTED_TO_vga_out_B      --       .B
      );
```

TEMPLATES

NIOS II Character Display - HW

- Create DE10 Design
  - Instantiate into a VHDL file

Instantiation template component

```
architecture behavioral of nios_char_de10 is
    --
    -- no signals

    component nios_char is
        port (
            clk_clk       : in  std_logic                     := 'X'; -- clk
            reset_reset_n : in  std_logic                     := 'X'; -- reset_n
            vga_out_CLK   : out std_logic;                            -- CLK
            vga_out_HS    : out std_logic;                            -- HS
            vga_out_VS    : out std_logic;                            -- VS
            vga_out_BLANK : out std_logic;                            -- BLANK
            vga_out_SYNC  : out std_logic;                            -- SYNC
            vga_out_R     : out std_logic_vector(3 downto 0);         -- R
            vga_out_G     : out std_logic_vector(3 downto 0);         -- G
            vga_out_B     : out std_logic_vector(3 downto 0)          -- B
        );
    end component nios_char;
```

```
-------------------------------------
--
-- nios_char_de10.vhdl
--
-- Created  9/18/18
-- by:      johnsontimoj
-- rev:     0
--
-------------------------------------
--
-- Nios character system - vga driver with charac
--
-------------------------------------

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;


entity nios_char_de10 is
    port(
        CLOCK_50 :      in std_logic;
        VGA_HS:         out std_logic;
        VGA_VS:         out std_logic;
        VGA_R:          out std_logic_vector(3 downto 0);
        VGA_G:          out std_logic_vector(3 downto 0);
        VGA_B:          out std_logic_vector(3 downto 0)
    );
end entity;
```

DE10 pin aliases from .qsf file

NIOS II Character Display - HW

- Create DE10 Design
  - Instantiate into a VHDL file

Instantiation template instance mapped to DE10 qsf pin aliases

```
begin

    u0 : component nios_char
        port map (
            clk_clk       => CLOCK_50, --     clk.clk
            reset_reset_n => '1',      --   reset.reset_n
            --vga_out_CLK   => CONNECTED_TO_vga_out_CLK,    -- vga_out.CLK
            vga_out_HS    => VGA_HS,     --         .HS
            vga_out_VS    => VGA_VS,     --         .VS
            --vga_out_BLANK => CONNECTED_TO_vga_out_BLANK, -- .BLANK
            --vga_out_SYNC  => CONNECTED_TO_vga_out_SYNC,  -- .SYNC
            vga_out_R     => VGA_R,      --         .R
            vga_out_G     => VGA_G,      --         .G
            vga_out_B     => VGA_B       --         .B
        );

end architecture;
```

Note: these 3 signals are not used - comment out or remove

NIOS II Character Display - HW

- Create DE10 Design
  - Prepare to synthesize
    - If you did not do these when you created the project be sure to do them now
      - assignments → device → device and Pin options
        - Single Uncompressed with memory initialization
      - Import the pin aliases (qsf file)
      - Setup the SDF file
  - Be sure to set your top level entity
  - Start Compilation

NIOS II Character Display - HW

- Create DE10 Design
  - Complete the HW setup
    - Download the HW project onto the board
    - DO NOT CLOSE either of these windows