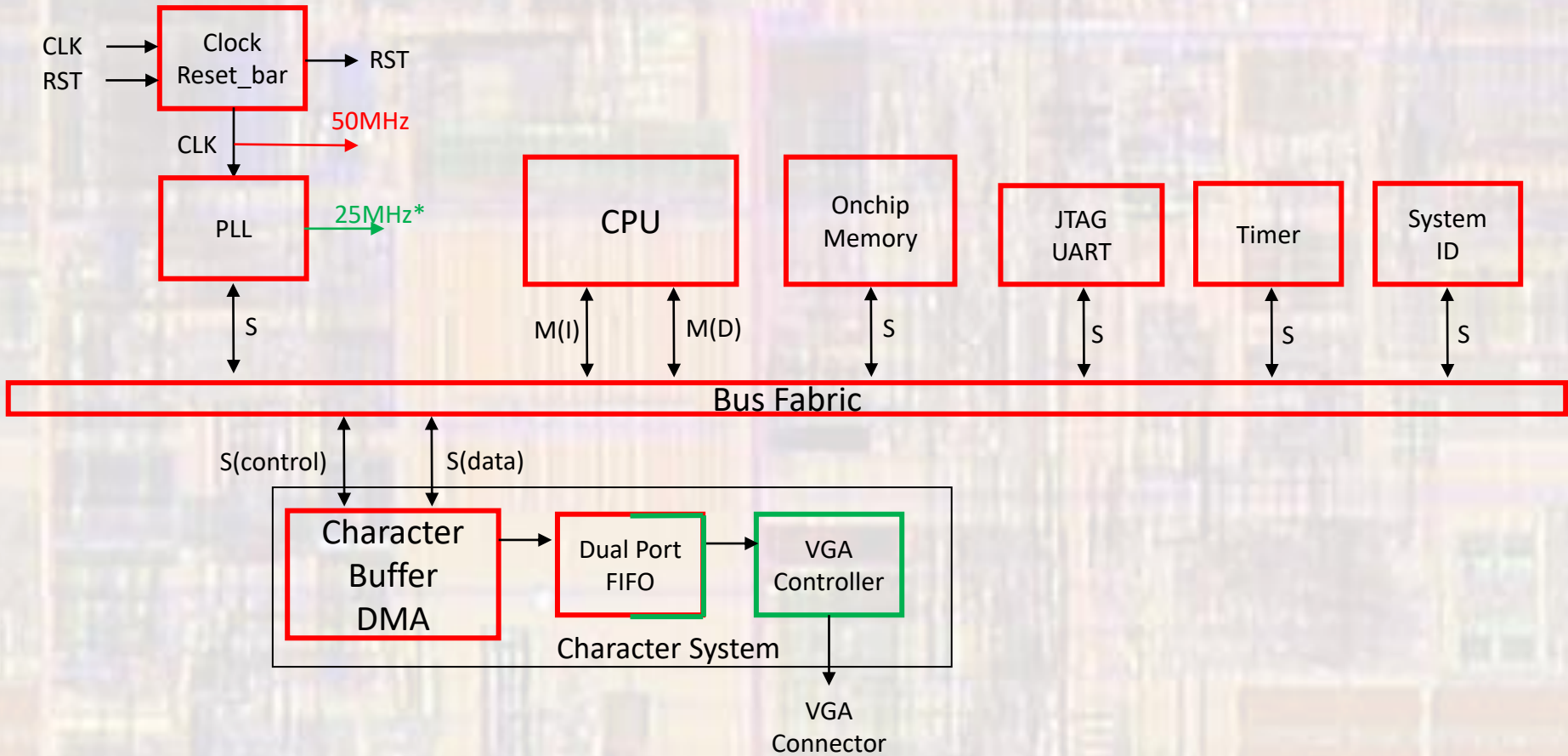


NIOS Character HW

Last updated 7/20/23

NIOS II Character Display - HW

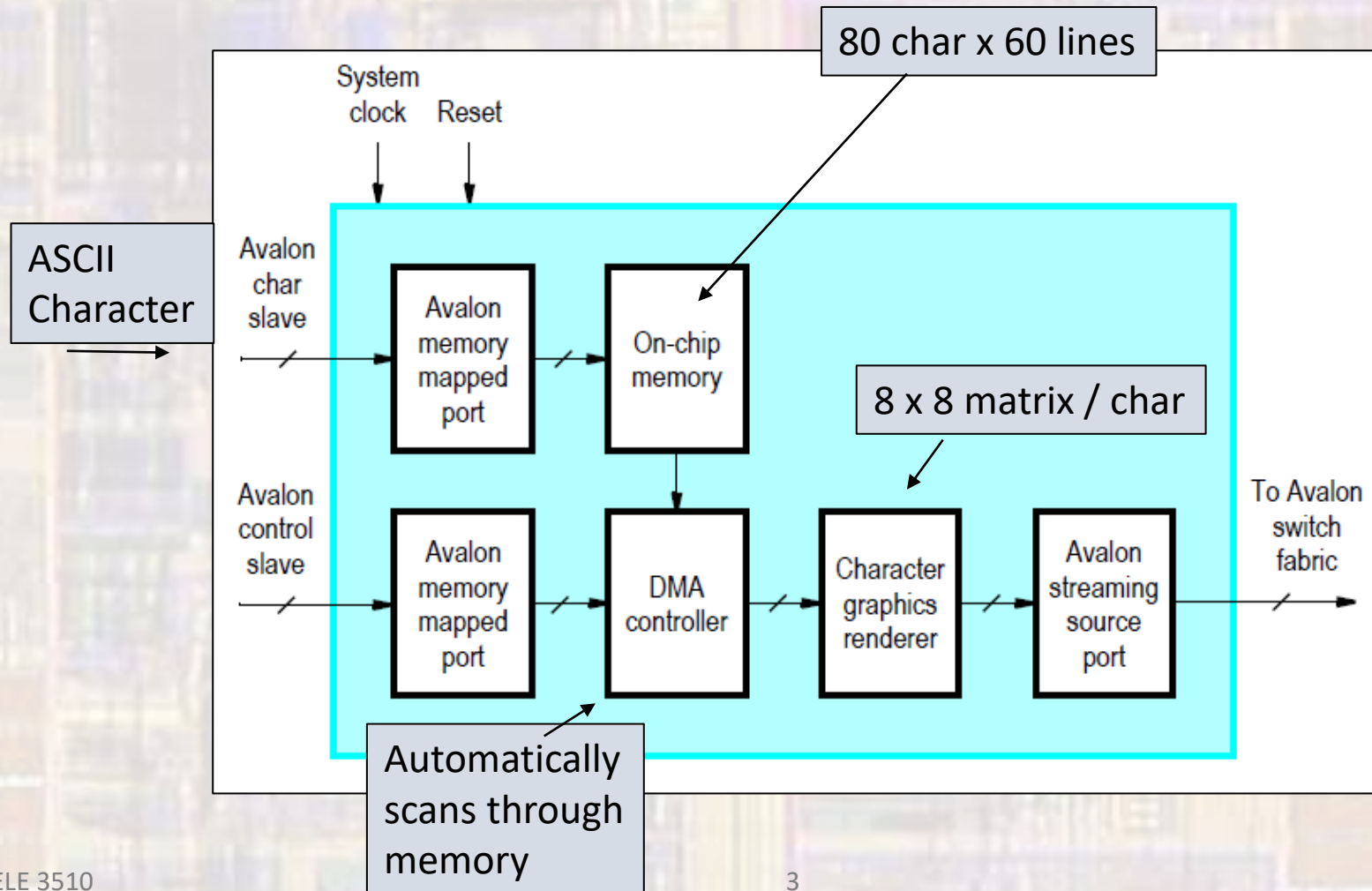
- Character Buffer Block Diagram



25MHz** - VGA clk

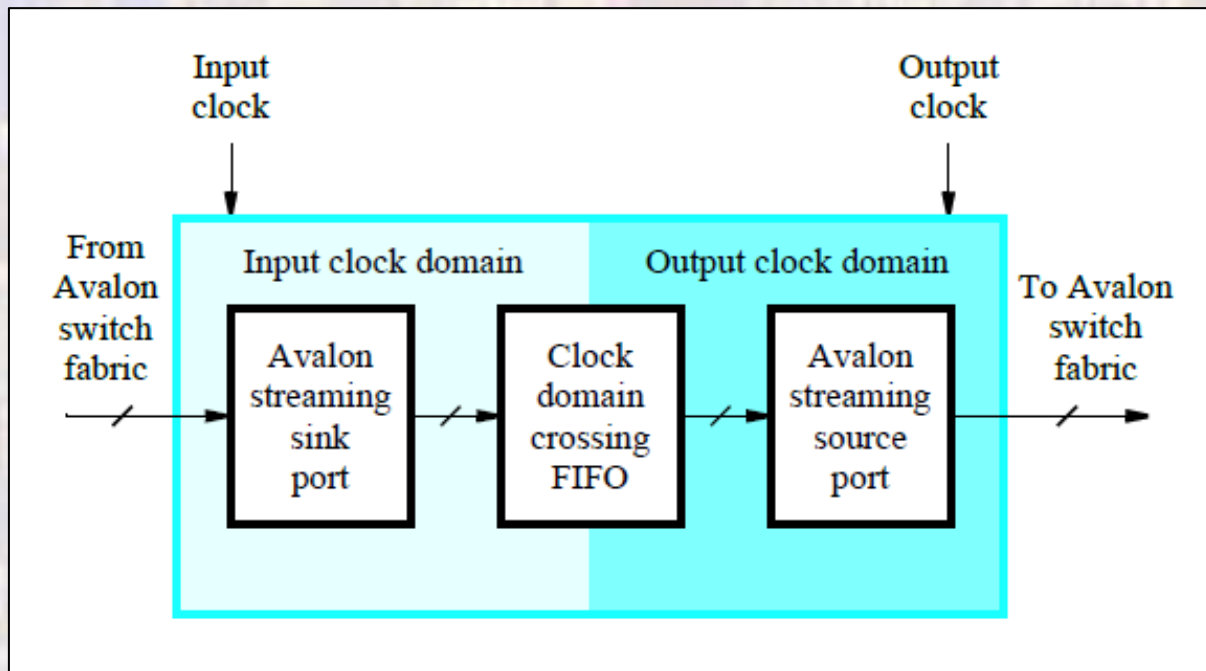
NIOS II Character Display - HW

- Character Buffer Block



NIOS II Character Display - HW

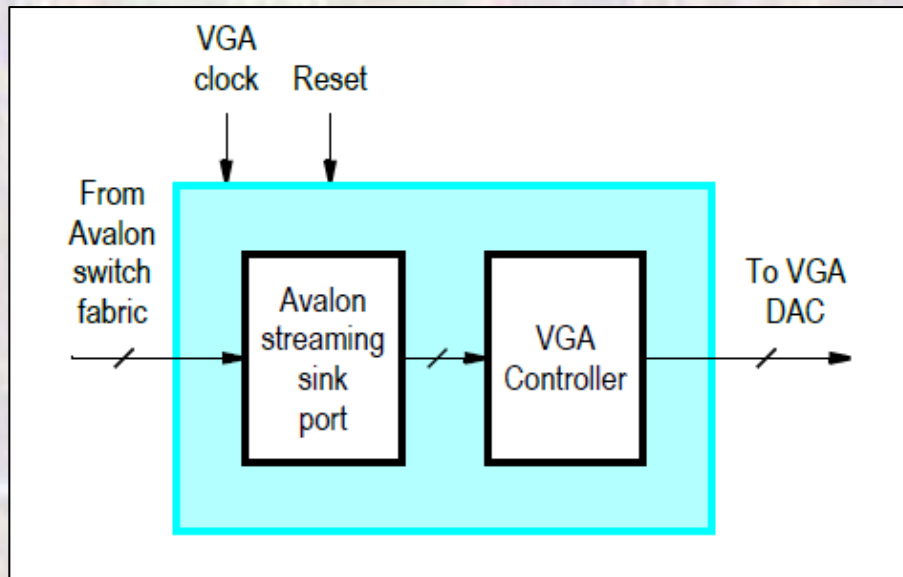
- Dual Clock FIFO



Allows different incoming and outgoing data rates

NIOS II Character Display - HW

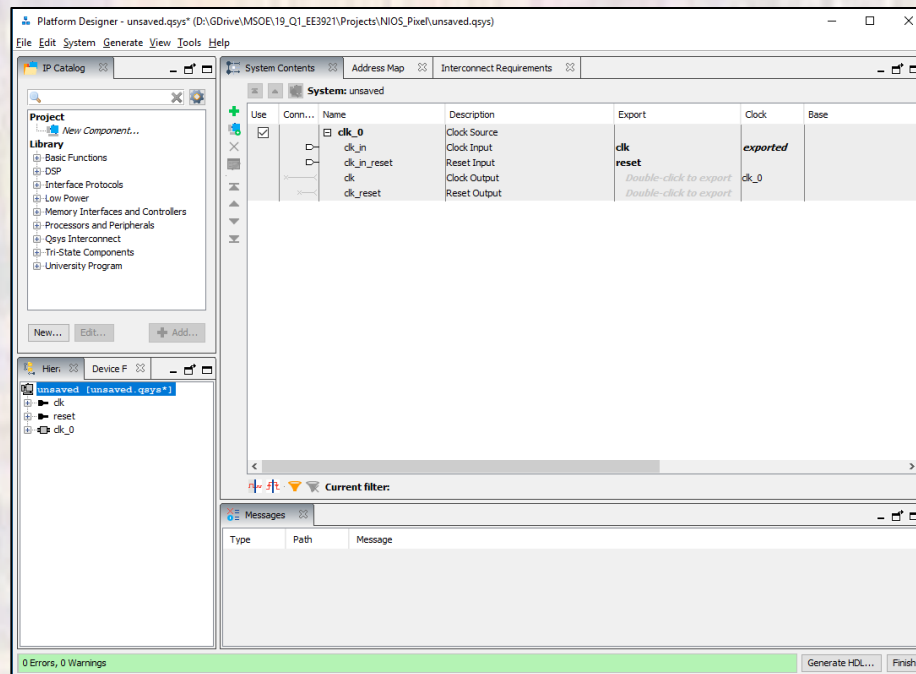
- VGA Controller Block



Creates and drives the required VGA signals

NIOS II Character Display - HW

- Create a new Quartus project
 - Do not select a Simulation Tool in EDA Tool Settings
- Open **Tools** → **Platform Designer**



NIOS II Character Display - HW

- Add NIOS
 - Processors and Peripherals → Embedded Processors → NIOS II Processor
 - NIOS II/f

<input type="checkbox"/>	clk_reset	Reset Output	<i>Double-click to export</i>		
<input checked="" type="checkbox"/>	nios2_gen2_0	Nios II Processor			
<input type="checkbox"/>	clk	Clock Input	<i>Double-click to export</i>	unconnected	
<input type="checkbox"/>	reset	Reset Input	<i>Double-click to export</i>	[clk]	
<input type="checkbox"/>	data_master	Avalon Memory Mapped Master	<i>Double-click to export</i>	[clk]	
<input type="checkbox"/>	instruction_master	Avalon Memory Mapped Master	<i>Double-click to export</i>	[clk]	
<input type="checkbox"/>	irq	Interrupt Receiver	<i>Double-click to export</i>	[clk]	
<input type="checkbox"/>	debug_reset_request	Reset Output	<i>Double-click to export</i>	[clk]	
<input type="checkbox"/>	debug_mem_slave	Avalon Memory Mapped Slave	<i>Double-click to export</i>	[clk]	0x08
<input type="checkbox"/>	custom_instruction_m...	Custom Instruction Master	<i>Double-click to export</i>		

- Add On-chip Memory
 - Basic Functions → On Chip Memory → On Chip Memory (RAM or ROM)...

RAM

Size = 12,000 bytes

<input type="checkbox"/>	debug_mem_slave	Avalon Memory Mapped Slave	<i>Double-click to export</i>	[clk]	0x08
<input type="checkbox"/>	custom_instruction_m...	Custom Instruction Master	<i>Double-click to export</i>		
<input checked="" type="checkbox"/>	onchip_memory2_0	On-Chip Memory (RAM or ROM) Intel ...			
<input type="checkbox"/>	clk1	Clock Input	<i>Double-click to export</i>	unconnected	
<input type="checkbox"/>	s1	Avalon Memory Mapped Slave	<i>Double-click to export</i>	[clk1]	
<input type="checkbox"/>	reset1	Reset Input	<i>Double-click to export</i>	[clk1]	

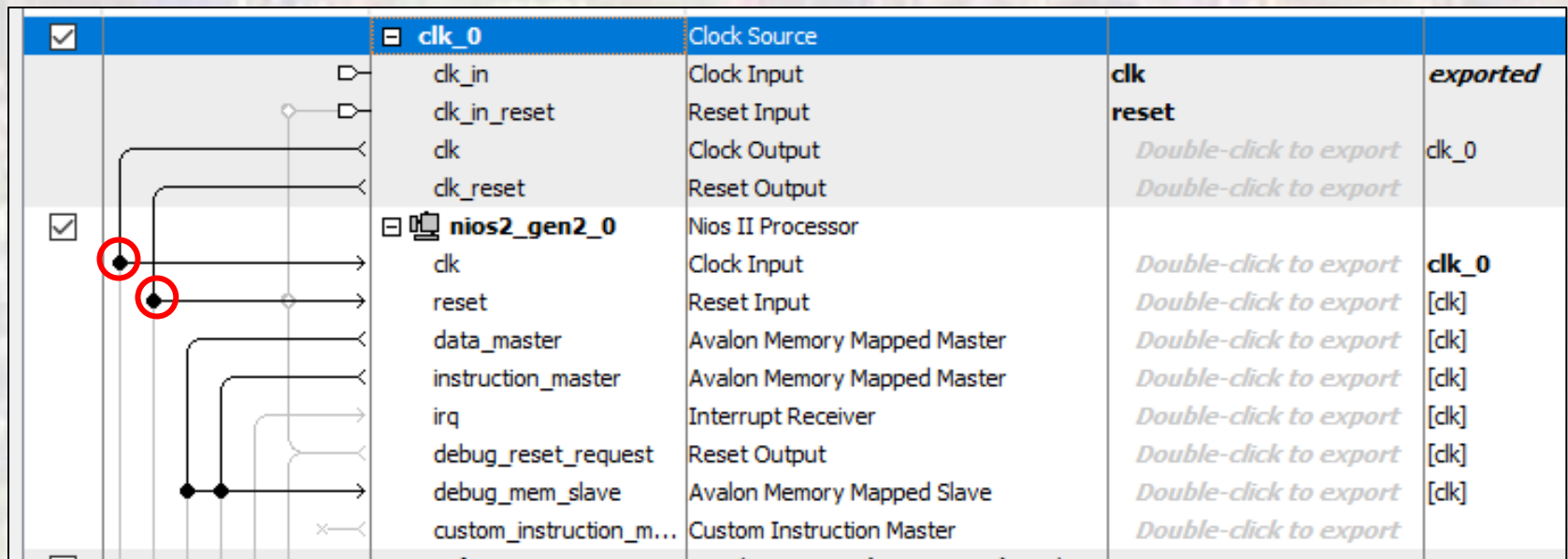
NIOS II Character Display - HW

- Add JTAG
 - Interface Protocols → Serial → JTAG Uart Intel FPGA IP
- Add Timer
 - Processors and Peripherals → Peripherals → Interval Timer Intel FPGA IP
- Add System ID
 - Basic Functions → Simulation; Debug and Verification → Debug and Performance → System ID Peripheral Intel FPGA IP

<input checked="" type="checkbox"/>		reset1	Reset Input	<i>Double-click to export</i>	[clk1]
<input checked="" type="checkbox"/>		jtag_uart_0 clk reset avalon_jtag_slave irq	JTAG UART Intel FPGA IP Clock Input Reset Input Avalon Memory Mapped Slave Interrupt Sender	<i>Double-click to export</i> <i>Double-click to export</i> <i>Double-click to export</i> <i>Double-click to export</i>	unconnected [clk] [clk] [clk]
<input checked="" type="checkbox"/>		timer_0 clk reset s1 irq	Interval Timer Intel FPGA IP Clock Input Reset Input Avalon Memory Mapped Slave Interrupt Sender	<i>Double-click to export</i> <i>Double-click to export</i> <i>Double-click to export</i> <i>Double-click to export</i>	unconnected [clk] [clk] [clk]
<input checked="" type="checkbox"/>		sysid_qsys_0 clk reset control_slave	System ID Peripheral Intel FPGA IP Clock Input Reset Input Avalon Memory Mapped Slave	<i>Double-click to export</i> <i>Double-click to export</i> <i>Double-click to export</i>	unconnected [clk] [clk]

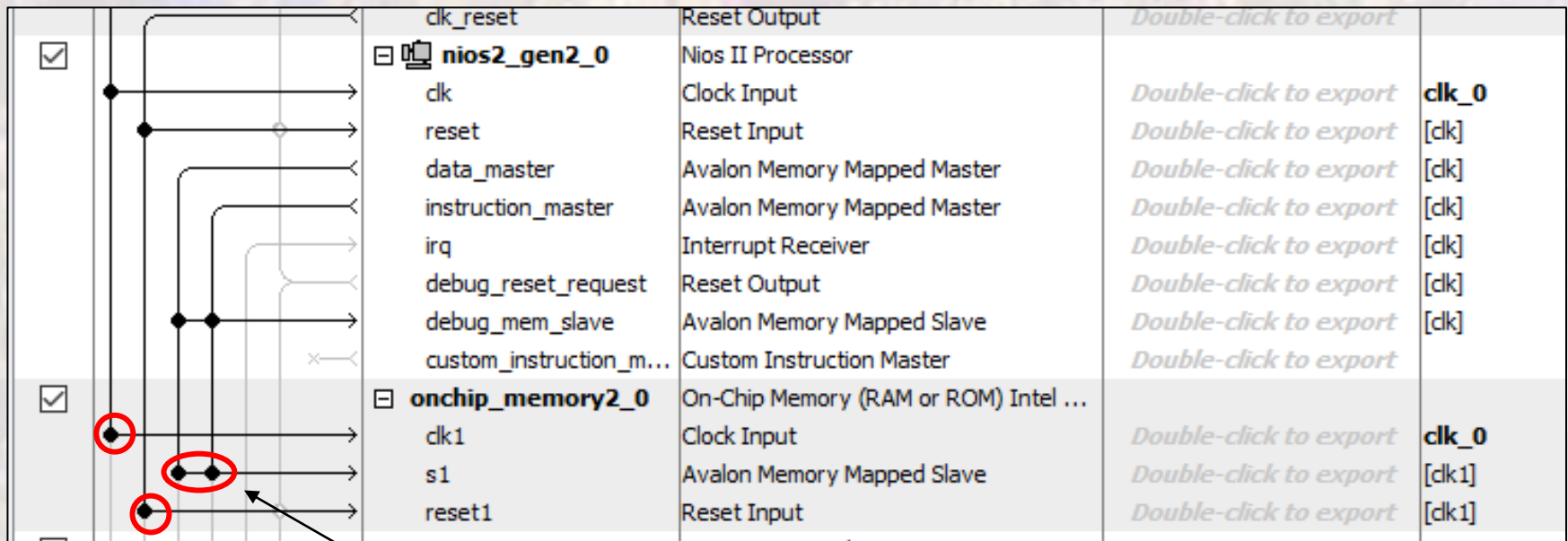
NIOS II Character Display - HW

- Connect up basic NIOS system
 - NIOS Inputs



NIOS II Character Display - HW

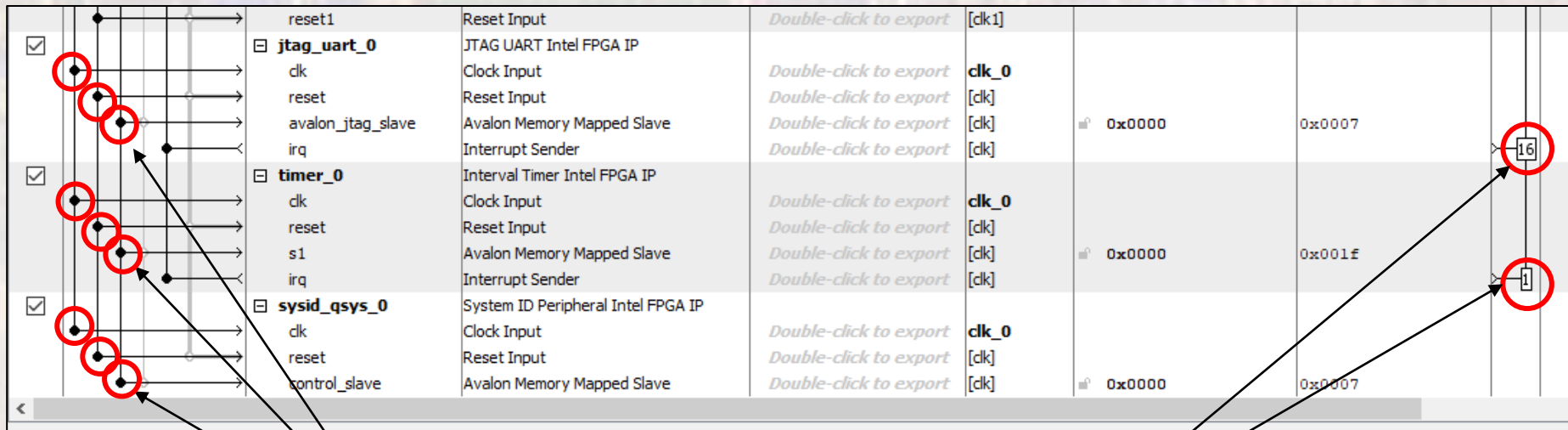
- Connect up basic NIOS system
 - On-chip Memory



Connect to data and instruction masters

NIOS II Character Display - HW

- Connect up basic NIOS system
 - JTAG, Timer, SysID

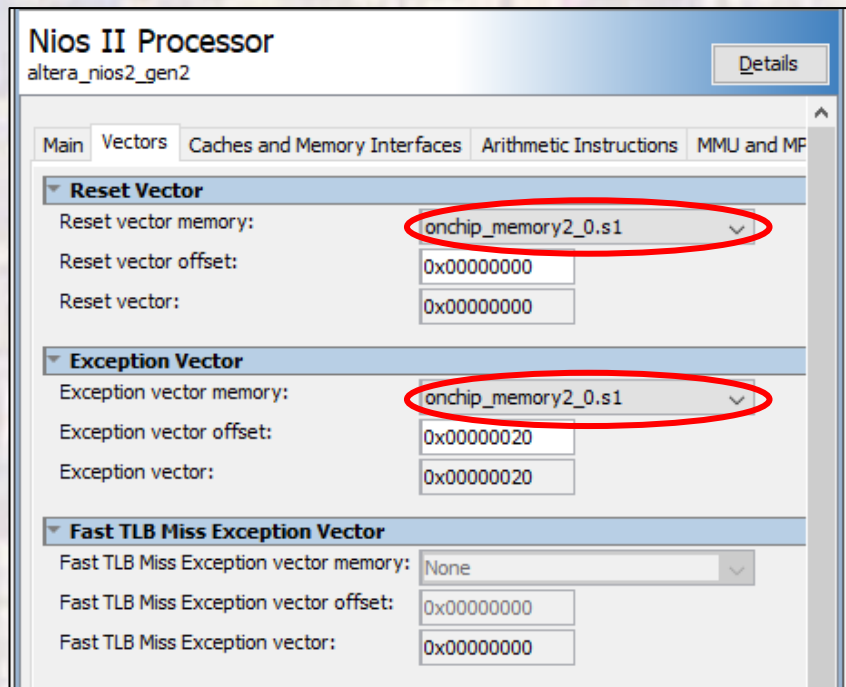


Connect to data master

Assign Priorities

NIOS II Character Display - HW

- Connect up basic NIOS system
 - Assign the NIOS II Reset and Exception vectors



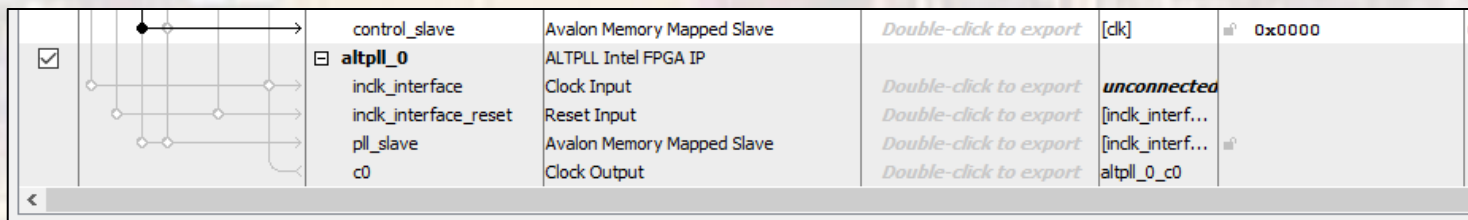
NIOS II Character Display - HW

- Create Character System
 - Add a PLL
 - [Basic Functions](#) → [Clocks; PLLs and Resets](#) → [PLL](#) → [ALTPLL Intel FPGA IP](#)

50MHz input clock

no areset or locked output

c0 → 25MHz : the VGA frequency

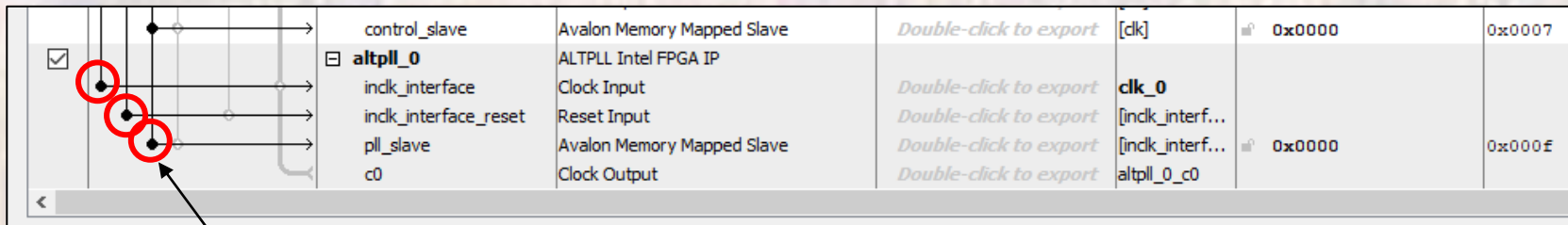


The screenshot shows the HW Config tool interface. On the left, a block diagram shows the connections for the ALTPLL_0 component. The main table lists the components and their connections:

Component	Description	Connection	Value
control_slave	Avalon Memory Mapped Slave	Double-click to export	[clk]
altpll_0	ALTPLL Intel FPGA IP	Double-click to export	0x0000
indk_interface	Clock Input	Double-click to export	unconnected
indk_interface_reset	Reset Input	Double-click to export	[indk_interf...]
pll_slave	Avalon Memory Mapped Slave	Double-click to export	[indk_interf...]
c0	Clock Output	Double-click to export	altpll_0_c0

NIOS II Character Display - HW

- Create Character System
 - Connect PLL



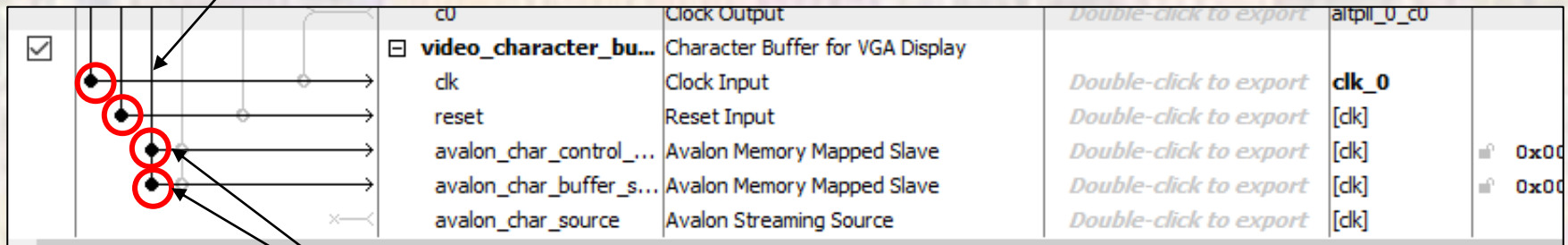
<input checked="" type="checkbox"/>	control_slave	Avalon Memory Mapped Slave	<i>Double-click to export</i>	[clk]	0x0000	0x0007
	altpll_0	ALTPLL Intel FPGA IP				
	indk_interface	Clock Input	<i>Double-click to export</i>	clk_0		
	indk_interface_reset	Reset Input	<i>Double-click to export</i>	[indk_interf...		
	pll_slave	Avalon Memory Mapped Slave	<i>Double-click to export</i>	[indk_interf...	0x0000	0x000F
	c0	Clock Output	<i>Double-click to export</i>	altpll_0_c0		

Connect to the 50MHz Clk, reset and the data master

NIOS II Character Display - HW

- Create Character System
 - Character Buffer
 - University Program → Audio and Video → Video → Character Buffer for VGA Display

Connect to 50Mhz Clk and reset



Connect to data master

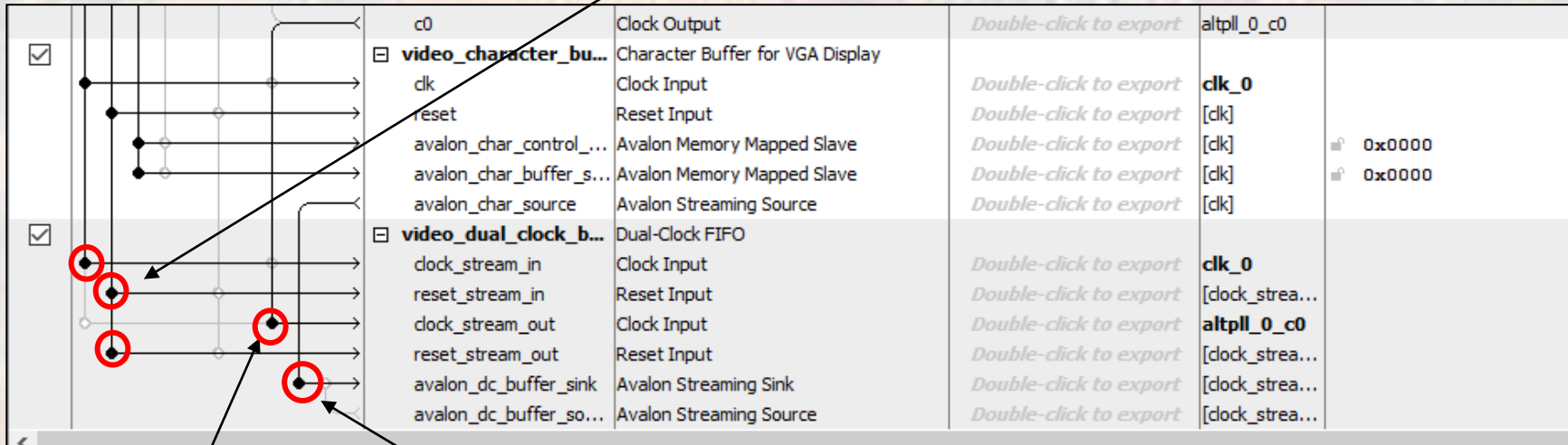
NIOS II Character Display - HW

- Create Character System
 - Dual Clock FIFO
 - University Program → Audio and Video → Video → Dual Clock FIFO

Color Bits – 10

Color Planes - 3

Connect to 50Mhz Clk and reset



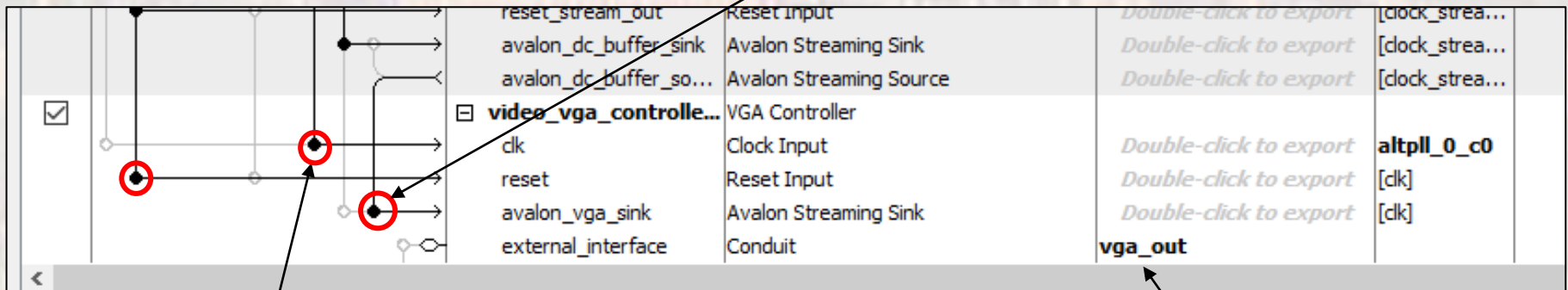
Connect to c0
VGA – 25MHz

Connect to video character buffer streaming source

NIOS II Character Display - HW

- Create Character System
 - VGA Controller
 - [University Program](#) → [Audio and Video](#) → [Video](#) → [VGA Controller](#)
- DE10-Lite
VGA Connector
VGA 640x480

Connect to dual_clock_buffer streaming source



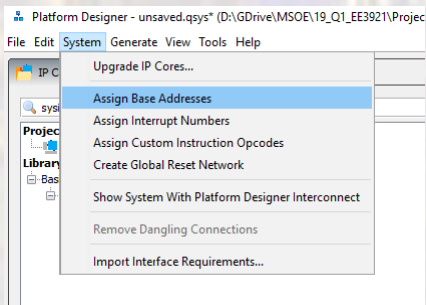
Connect to c0
VGA – 25MHz

Export and rename

NIOS II Character Display - HW

- Create Character

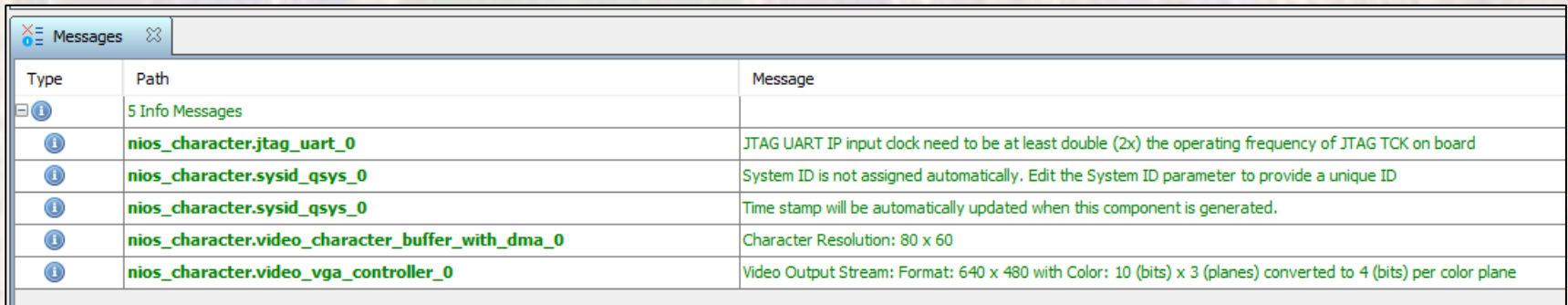
Assign Base Addresses



Use	Connections	Name	Description	Export	Clock	Base	End	IRQ	Tags
<input checked="" type="checkbox"/>		clk_0	Clock Source	clk	exported				
<input checked="" type="checkbox"/>		clk_in	Clock Input	clk	Double-click to export	clk_0			
<input checked="" type="checkbox"/>		clk_in_reset	Reset Input	reset	Double-click to export				
<input checked="" type="checkbox"/>		clk	Clock Output	clk_0	Double-click to export				
<input checked="" type="checkbox"/>		clk_reset	Reset Output		Double-click to export				
<input checked="" type="checkbox"/>		nios2_gen2_0	Nios II Processor						
<input checked="" type="checkbox"/>		clk	Clock Input	clk_0	Double-click to export				
<input checked="" type="checkbox"/>		reset	Reset Input	[clk]	Double-click to export				
<input checked="" type="checkbox"/>		data_master	Avalon Memory Mapped Master	[clk]	Double-click to export				
<input checked="" type="checkbox"/>		instruction_master	Avalon Memory Mapped Master	[clk]	Double-click to export				
<input checked="" type="checkbox"/>		irq	Interrupt Receiver	IRQ 0	Double-click to export				IRQ 31
<input checked="" type="checkbox"/>		debug_reset_request	Reset Output	[clk]	Double-click to export				
<input checked="" type="checkbox"/>		debug_mem_slave	Avalon Memory Mapped Slave	[clk]	Double-click to export				
<input checked="" type="checkbox"/>		custom_instruction_m...	Custom Instruction Master	[clk]	Double-click to export		0x4800	0x4fff	
<input checked="" type="checkbox"/>		onchip_memory2_0	On-Chip Memory (RAM or ROM) Intel ...						
<input checked="" type="checkbox"/>	clk1	Clock Input	clk_0	Double-click to export					
<input checked="" type="checkbox"/>	s1	Avalon Memory Mapped Slave	[clk1]	Double-click to export		0x3000	0x3fff		
<input checked="" type="checkbox"/>	reset1	Reset Input	[clk1]	Double-click to export					
<input checked="" type="checkbox"/>	jtag_uart_0	JTAG UART Intel FPGA IP							
<input checked="" type="checkbox"/>	clk	Clock Input	clk_0	Double-click to export					
<input checked="" type="checkbox"/>	reset	Reset Input	[clk]	Double-click to export					
<input checked="" type="checkbox"/>	avalon_jtag_slave	Avalon Memory Mapped Slave	[clk]	Double-click to export		0x5040	0x5047		
<input checked="" type="checkbox"/>	irq	Interrupt Sender	[clk]	Double-click to export					
<input checked="" type="checkbox"/>	timer_0	Interval Timer Intel FPGA IP							
<input checked="" type="checkbox"/>	clk	Clock Input	clk_0	Double-click to export					
<input checked="" type="checkbox"/>	reset	Reset Input	[clk]	Double-click to export					
<input checked="" type="checkbox"/>	s1	Avalon Memory Mapped Slave	[clk]	Double-click to export		0x5000	0x501f		
<input checked="" type="checkbox"/>	irq	Interrupt Sender	[clk]	Double-click to export					
<input checked="" type="checkbox"/>	sysid_qsys_0	System ID Peripheral Intel FPGA IP							
<input checked="" type="checkbox"/>	clk	Clock Input	clk_0	Double-click to export					
<input checked="" type="checkbox"/>	reset	Reset Input	[clk]	Double-click to export					
<input checked="" type="checkbox"/>	control_slave	Avalon Memory Mapped Slave	[clk]	Double-click to export		0x5038	0x503f		
<input checked="" type="checkbox"/>	altpll_0	ALTPLL Intel FPGA IP							
<input checked="" type="checkbox"/>	indk_interface	Clock Input	clk_0	Double-click to export					
<input checked="" type="checkbox"/>	indk_interface_reset	Reset Input	[indk_interf...	Double-click to export					
<input checked="" type="checkbox"/>	pll_slave	Avalon Memory Mapped Slave	[indk_interf...	Double-click to export		0x5020	0x502f		
<input checked="" type="checkbox"/>	c0	Clock Output	altpll_0_c0	Double-click to export					
<input checked="" type="checkbox"/>	video_character_bu...	Character Buffer for VGA Display							
<input checked="" type="checkbox"/>	clk	Clock Input	clk_0	Double-click to export					
<input checked="" type="checkbox"/>	reset	Reset Input	[clk]	Double-click to export					
<input checked="" type="checkbox"/>	avalon_char_control...	Avalon Memory Mapped Slave	[clk]	Double-click to export		0x5030	0x5037		
<input checked="" type="checkbox"/>	avalon_char_buffer_s...	Avalon Memory Mapped Slave	[clk]	Double-click to export		0x0000	0x1fff		
<input checked="" type="checkbox"/>	avalon_char_source	Avalon Streaming Source	[clk]	Double-click to export					
<input checked="" type="checkbox"/>	video_dual_clock_b...	Dual-Clock FIFO							
<input checked="" type="checkbox"/>	dock_stream_in	Clock Input	clk_0	Double-click to export					
<input checked="" type="checkbox"/>	reset_stream_in	Reset Input	[dock_strea...	Double-click to export					
<input checked="" type="checkbox"/>	dock_stream_out	Clock Input	altpll_0_c0	Double-click to export					
<input checked="" type="checkbox"/>	reset_stream_out	Reset Input	[dock_strea...	Double-click to export					
<input checked="" type="checkbox"/>	avalon_dc_buffer_sink	Avalon Streaming Sink	[dock_strea...	Double-click to export					
<input checked="" type="checkbox"/>	avalon_dc_buffer_so...	Avalon Streaming Source	[dock_strea...	Double-click to export					
<input checked="" type="checkbox"/>	video_vga_controll...	VGA Controller							
<input checked="" type="checkbox"/>	clk	Clock Input	altpll_0_c0	Double-click to export					
<input checked="" type="checkbox"/>	reset	Reset Input	[clk]	Double-click to export					
<input checked="" type="checkbox"/>	avalon_vga_sink	Avalon Streaming Sink	[clk]	Double-click to export					
<input checked="" type="checkbox"/>	external_interface	Conduit	vga_out	Double-click to export					

NIOS II Character Display - HW

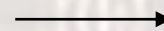
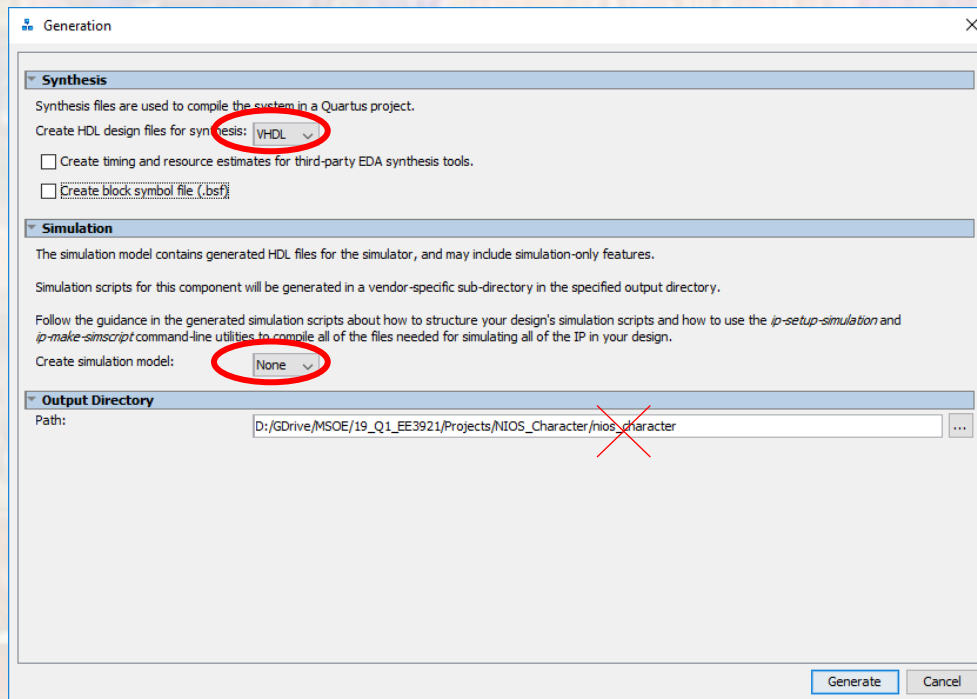
- Create Character System
 - Check for errors



Type	Path	Message
5 Info Messages		
i	nios_character.jtag_uart_0	JTAG UART IP input clock need to be at least double (2x) the operating frequency of JTAG TCK on board
i	nios_character.sysid_qsys_0	System ID is not assigned automatically. Edit the System ID parameter to provide a unique ID
i	nios_character.sysid_qsys_0	Time stamp will be automatically updated when this component is generated.
i	nios_character.video_character_buffer_with_dma_0	Character Resolution: 80 x 60
i	nios_character.video_vga_controller_0	Video Output Stream: Format: 640 x 480 with Color: 10 (bits) x 3 (planes) converted to 4 (bits) per color plane

NIOS II Character Display - HW

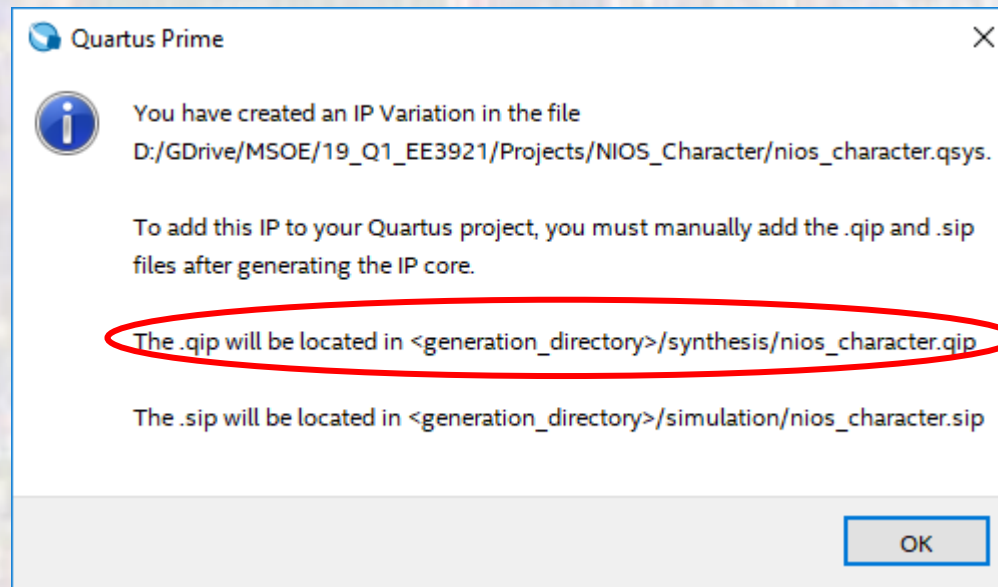
- Create Character System
 - Save the Platform Designer system
 - Generate the Platform Designer system
 - The first time you generate you must delete the last directory in the path – **don't use the '...'**



D:/GDrive/MSOE/19_Q1_EE3921/Projects/NIOS_Character

NIOS II Character Display - HW

- Create Character System
 - Add the .qip file to the project



NIOS II Character Display - HW

- Create DE10 Design
 - Instantiate into a VHDL file
 - Open a new VHDL design
 - In Platform Designer: **Generate** → **Show Instantiation Template**
 - Copy and Paste into the new design where appropriate

```
component nios_char is
  port (
    clk_clk      : in std_logic      := 'X'; -- clk
    reset_reset_n : in std_logic      := 'X'; -- reset_n
    vga_out_CLK   : out std_logic;    -- CLK
    vga_out_HS    : out std_logic;    -- HS
    vga_out_VS    : out std_logic;    -- VS
    vga_out_BLANK : out std_logic;    -- BLANK
    vga_out_SYNC  : out std_logic;    -- SYNC
    vga_out_R     : out std_logic_vector(3 downto 0); -- R
    vga_out_G     : out std_logic_vector(3 downto 0); -- G
    vga_out_B     : out std_logic_vector(3 downto 0); -- B
  );
end component nios_char;
```

```
u0 : component nios_char
  port map (
    clk_clk      => CONNECTED_TO_clk_clk,  -- clk.clk
    reset_reset_n => CONNECTED_TO_reset_reset_n, -- reset.reset_n
    vga_out_CLK   => CONNECTED_TO_vga_out_CLK, -- vga_out.CLK
    vga_out_HS    => CONNECTED_TO_vga_out_HS,  -- .HS
    vga_out_VS    => CONNECTED_TO_vga_out_VS,  -- .VS
    vga_out_BLANK => CONNECTED_TO_vga_out_BLANK, -- .BLANK
    vga_out_SYNC  => CONNECTED_TO_vga_out_SYNC, -- .SYNC
    vga_out_R     => CONNECTED_TO_vga_out_R,  -- .R
    vga_out_G     => CONNECTED_TO_vga_out_G,  -- .G
    vga_out_B     => CONNECTED_TO_vga_out_B,  -- .B
  );
```

TEMPLATES

NIOS II Character Display - HW

- Create DE10 Design
 - Instantiate into a VHDL file

Instantiation template component

```
-----  
-- nios_char_de10.vhd1  
--  
-- Created 9/18/18  
-- by: johnsontimoj  
-- rev: 0  
-----  
-- Nios character system - vga driver with charac  
--  
-----  
library ieee;  
use ieee.std_logic_1164.all;  
use ieee.numeric_std.all;  
  
entity nios_char_de10 is  
  port(  
    CLOCK_50 : in std_logic;  
    VGA_HS: out std_logic;  
    VGA_VS: out std_logic;  
    VGA_R: out std_logic_vector(3 downto 0);  
    VGA_G: out std_logic_vector(3 downto 0);  
    VGA_B: out std_logic_vector(3 downto 0)  
  );  
end entity;
```

```
architecture behavioral of nios_char_de10 is  
  --  
  -- no signals  
  
  component nios_char is  
    port (  
      clk_clk : in std_logic := 'X'; -- clk  
      reset_reset_n : in std_logic := 'X'; -- reset_n  
      vga_out_CLK : out std_logic; -- CLK  
      vga_out_HS : out std_logic; -- HS  
      vga_out_VS : out std_logic; -- VS  
      vga_out_BLANK : out std_logic; -- BLANK  
      vga_out_SYNC : out std_logic; -- SYNC  
      vga_out_R : out std_logic_vector(3 downto 0); -- R  
      vga_out_G : out std_logic_vector(3 downto 0); -- G  
      vga_out_B : out std_logic_vector(3 downto 0); -- B  
    );  
  end component nios_char;
```

DE10 pin aliases from .qsf file

NIOS II Character Display - HW

- Create DE10 Design
 - Instantiate into a VHDL file

Instantiation template instance mapped to DE10 qsf pin aliases

```
begin
  u0 : component nios_char
    port map (
      clk_clk      => CLOCK_50, -- clk.clk
      reset_reset_n => '1',    -- reset.reset_n
      --vga_out_CLK => CONNECTED_TO_vga_out_CLK, -- vga_out.CLK
      vga_out_HS   => VGA_HS,   -- .HS
      vga_out_VS   => VGA_VS,   -- .VS
      --vga_out_BLANK => CONNECTED_TO_vga_out_BLANK, -- .BLANK
      --vga_out_SYNC => CONNECTED_TO_vga_out_SYNC, -- .SYNC
      vga_out_R    => VGA_R,    -- .R
      vga_out_G    => VGA_G,    -- .G
      vga_out_B    => VGA_B,    -- .B
    );
end architecture;
```

Note: these 3 signals are not used
- comment out or remove

NIOS II Character Display - HW

- Create DE10 Design
 - Prepare to synthesize
 - If you did not do these when you created the project be sure to do them now
 - assignments → device → device and Pin options
 - Single Uncompressed with memory initialization
 - Import the pin aliases (qsf file)
 - Setup the SDF file
 - Be sure to set your top level entity
 - Start Compilation

NIOS II Character Display - HW

- Create DE10 Design
 - Complete the HW setup
 - Download the HW project onto the board
 - **DO NOT CLOSE** either of these windows

