Power and Power Distribution

Last updated 1/9/24

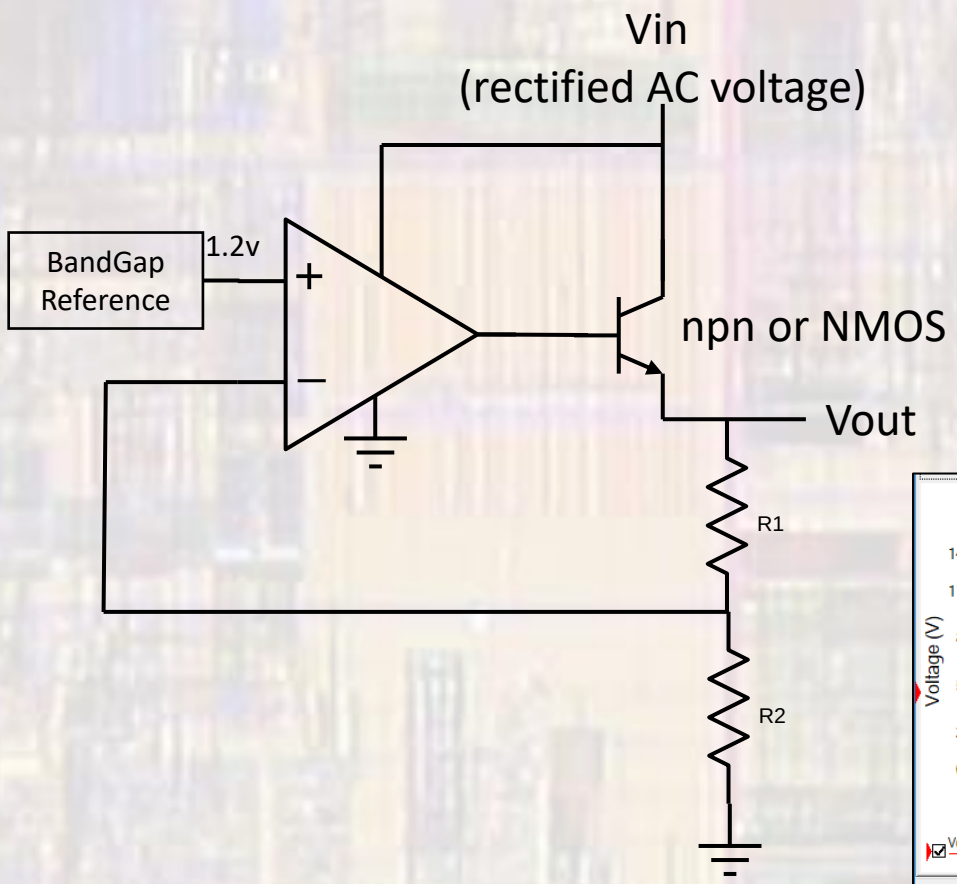
Power Generation

- DC Power
  - Essentially all digital systems run on DC power internally
    - I can't think of any that run on AC – but all is a hard statement
  - Even DC power solutions vary over time
    - Batteries run down
  - AC power solutions need to be converted to DC

→ Voltage regulation

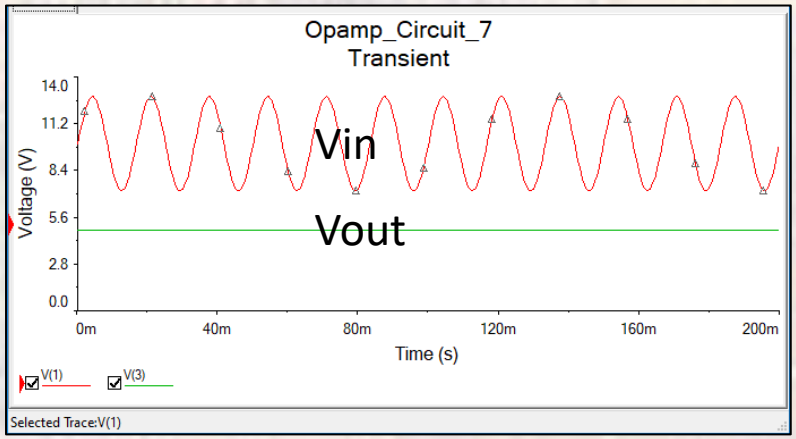
Power Generation

- DC Power – Voltage Regulation
  - Super simple voltage regulator



$$\frac{R2}{R1+R2}Vout = Vbg$$

$$Vout = Vbg\frac{R1+R2}{R2}$$



Power Generation

- DC Power – Voltage Regulation
  - Parametrics
    - Output Voltage
      - Fixed for a given regulator
    - Line Regulation
      - Variation in the output voltage (%)
    - Input Voltage
      - Maximum input voltage level
    - Output Current
      - Max current to load
    - Dropout Voltage
      - Minimum input voltage level ABOVE the specified output voltage

Table 3. Electrical characteristics of LD1117#12

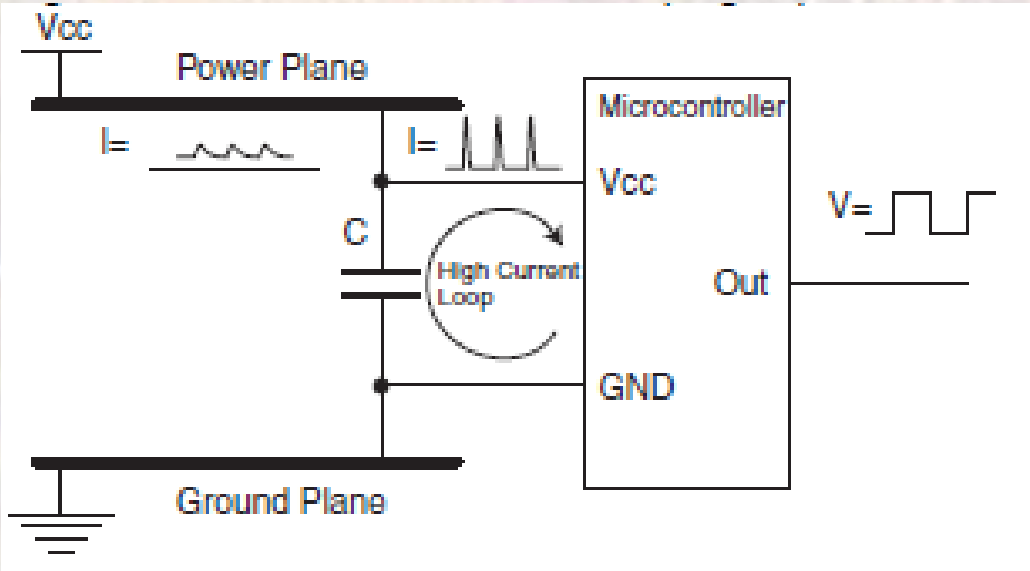
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_{in} = 3.2 V, I_O = 10 mA, T_J = 25 °C	1.188	1.20	1.212	V
V_O	Output voltage	I_O = 10 to 800 mA V_{in} - V_O = 1.4 to 10 V	1.140	1.20	1.260	V
ΔV_O	Line regulation	V_{in} - V_O = 1.5 to 13.75 V, I_O = 10 mA		0.035	0.2	%
ΔV_O	Load regulation	V_{in} - V_O = 3 V, I_O = 10 to 800 mA		0.1	0.4	%
ΔV_O	Temperature stability			0.5		%
ΔV_O	Long term stability	1000 hrs, T_J = 125 °C		0.3		%
V_{in}	Operating input voltage				15	V
I_{adj}	Adjustment pin current	$V_{in} \leq$ 15 V		60	120	µA
ΔI_{adj}	Adjustment pin current change	V_{in} - V_O = 1.4 to 10 V I_O = 10 to 800 mA		1	5	µA
$I_{O(min)}$	Minimum load current	V_{in} = 15 V		2	5	mA
I_O	Output current	V_{in} - V_O = 5 V, T_J = 25 °C	800	950	1300	mA
eN	Output noise (%V_O)	B = 10 Hz to 10 kHz, T_J = 25 °C		0.003		%
SVR	Supply voltage rejection	I_O = 40 mA, f = 120 Hz, T_J = 25 °C V_{in} - V_O = 3 V, V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout voltage	I_O = 100 mA		1	1.1	V
		I_O = 500 mA		1.05	1.15	
		I_O = 800 mA		1.10	1.2	
	Thermal regulation	T_a = 25 °C, 30 ms Pulse		0.01	0.1	%/W

Power Generation

- DC Power – Supply Bypassing
  - Digital circuits create current spikes on the supply pins
    - Shoot through current
    - Charging and discharging current
    - I/O switching
  - While the average supply current may be a few tens of milliamps, spikes associated with an 8 bit I/O switching can be hundreds of milliamps and a few nanoseconds wide
  - Power supplies and realistic circuit board traces cannot support these current spikes → noise on the supply voltage
  - Supply voltage noise can disrupt the normal operation of the processor or other circuits

Power Generation

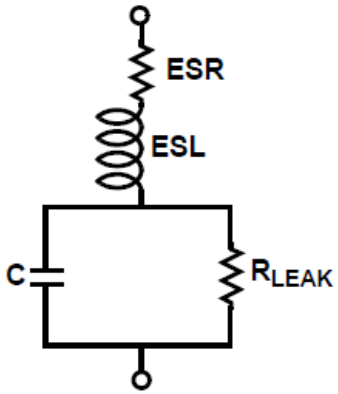
- DC Power – Supply Bypassing
  - Bypass capacitors are used to supply these spikes of current, preventing noise on the supply voltage pins



Power Generation

- DC Power – Supply Bypassing
  - Realistic capacitor model

ABBREVIATION	EXPLANATION	SOURCE AND DETAILS
ESR	Equivalent Series Resistance	Wire and connections to the plate Produces heat
ESL	Equivalent Series Inductance	Depends on package type Surface mount better Smaller SMD better
RLEAK	Leakage Resistance	Type of dielectric



Power Generation

- DC Power – Supply Bypassing
  - Realistic capacitor model

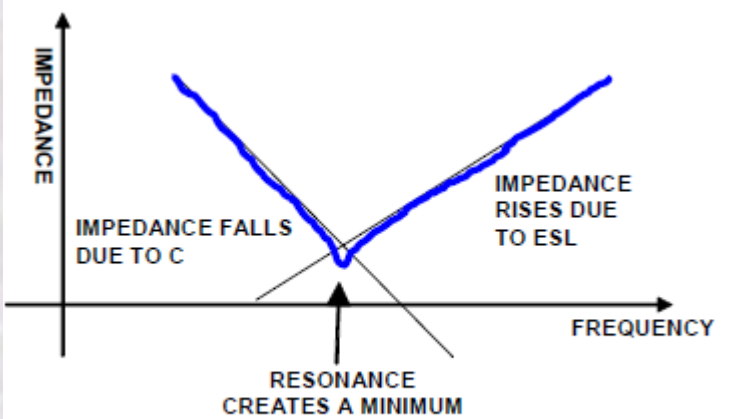


FIGURE 8. IMPEDANCE OF AN ACTUAL CAPACITOR (NON-IDEAL)

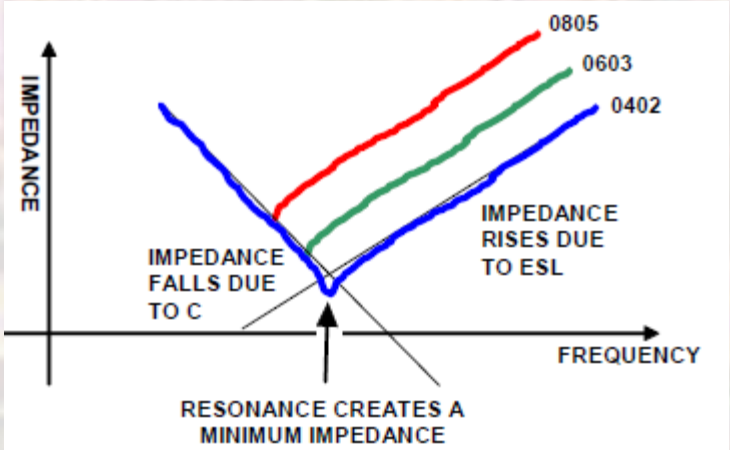


FIGURE 9. IMPEDANCE OF AN ACTUAL CAPACITOR (NON-IDEAL) IN DIFFERENT SURFACE-MOUNT PACKAGES

Power Generation

- DC Power – Supply Bypassing
  - Realistic capacitor model

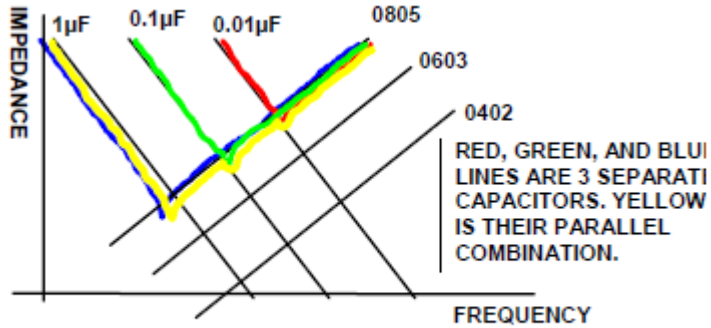


FIGURE 10. IMPEDANCE OF THREE CAPACITORS, THE SAME SURFACE-MOUNT PACKAGES

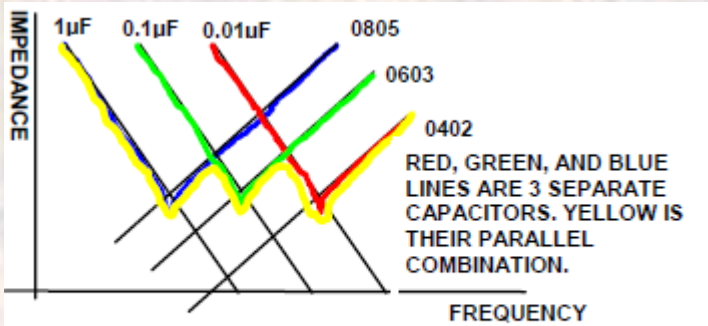


FIGURE 11. IMPEDANCE OF THREE CAPACITORS, SCALED SURFACE-MOUNT PACKAGES

Power Generation

- DC Power – Supply Bypassing
  - Most systems use 2 bypass capacitors
    - 1uF - 10uF for low frequency high current spikes
    - .001uF - .01uF for high frequency spikes
  - Placed as close to the IC as possible to reduce inductance

Values dependent on the system frequencies

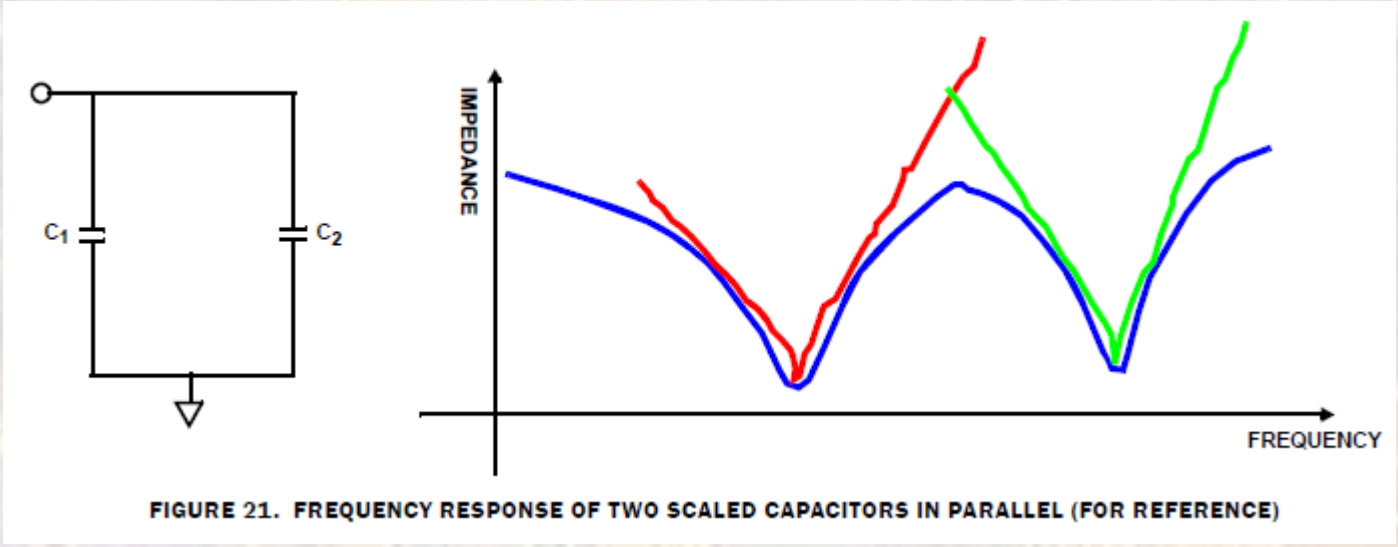
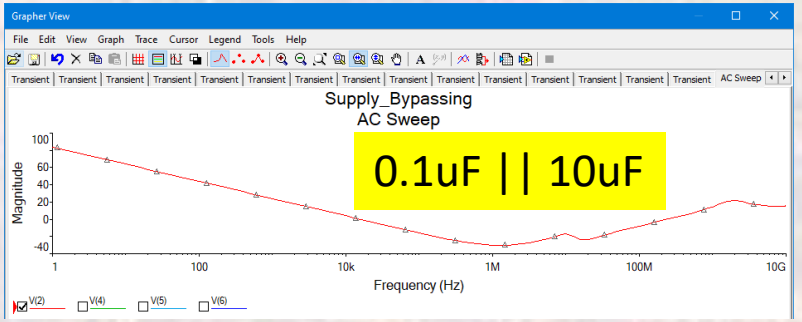
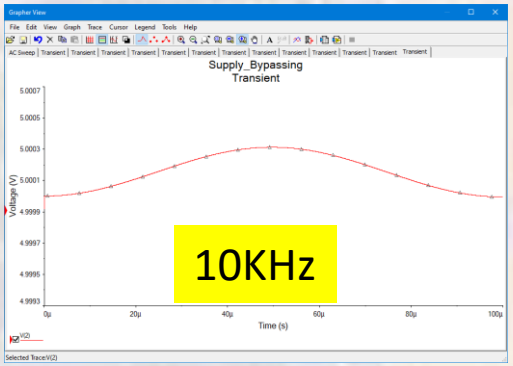


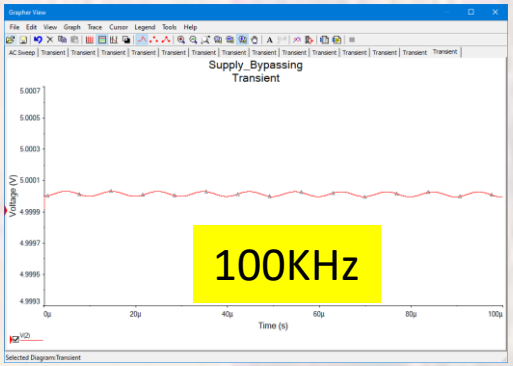
FIGURE 21. FREQUENCY RESPONSE OF TWO SCALED CAPACITORS IN PARALLEL (FOR REFERENCE)

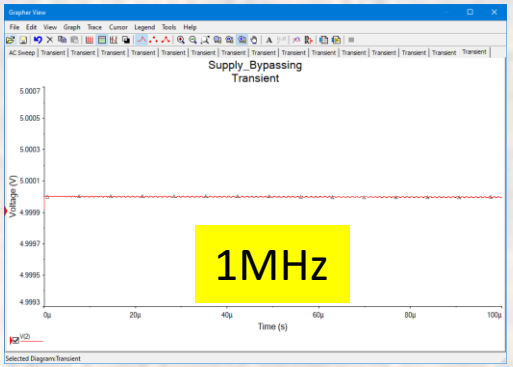
Power Generation

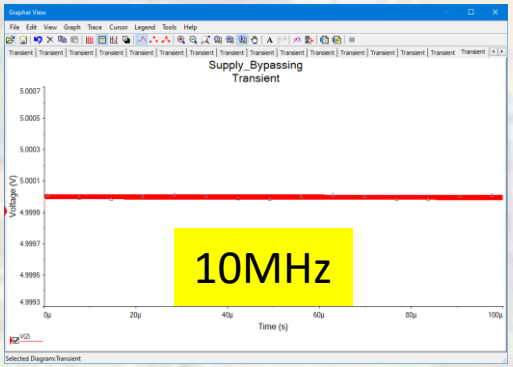
- DC Power – Supply Bypassing
  - Attenuation of supply noise at different frequencies











Power Distribution

- Board Level / System Level
  - Partition the design so that precise power (voltage) matching is not required between components or boards
    - I/Os with significant Noise Margin and PSRR
    - Can use 1 or more regulators
  - If voltage matching is required
    - Short, balanced traces may work – but very tricky due to input impedances shifting over temp, components, …
    - Trimmable regulators
  - In both cases – multiple supply entry ports
    - Tied together on the board or in the system

Power Distribution

- Chip Level
  - Grid structure for power
    - Multiple input locations (around the edges of the IC)
    - Internally tied together
    - Routed across many metal levels
    - Wide wires