Quartus Project Setup

Last updated 7/1/26

Quartus Project Setup

- Before creating your first Quartus project:
  - Install the Quartus software using the "Quartus Software Setup" slides
  - Setup your Quartus Project Hierarchy using the "Quartus Project File System Setup" slides

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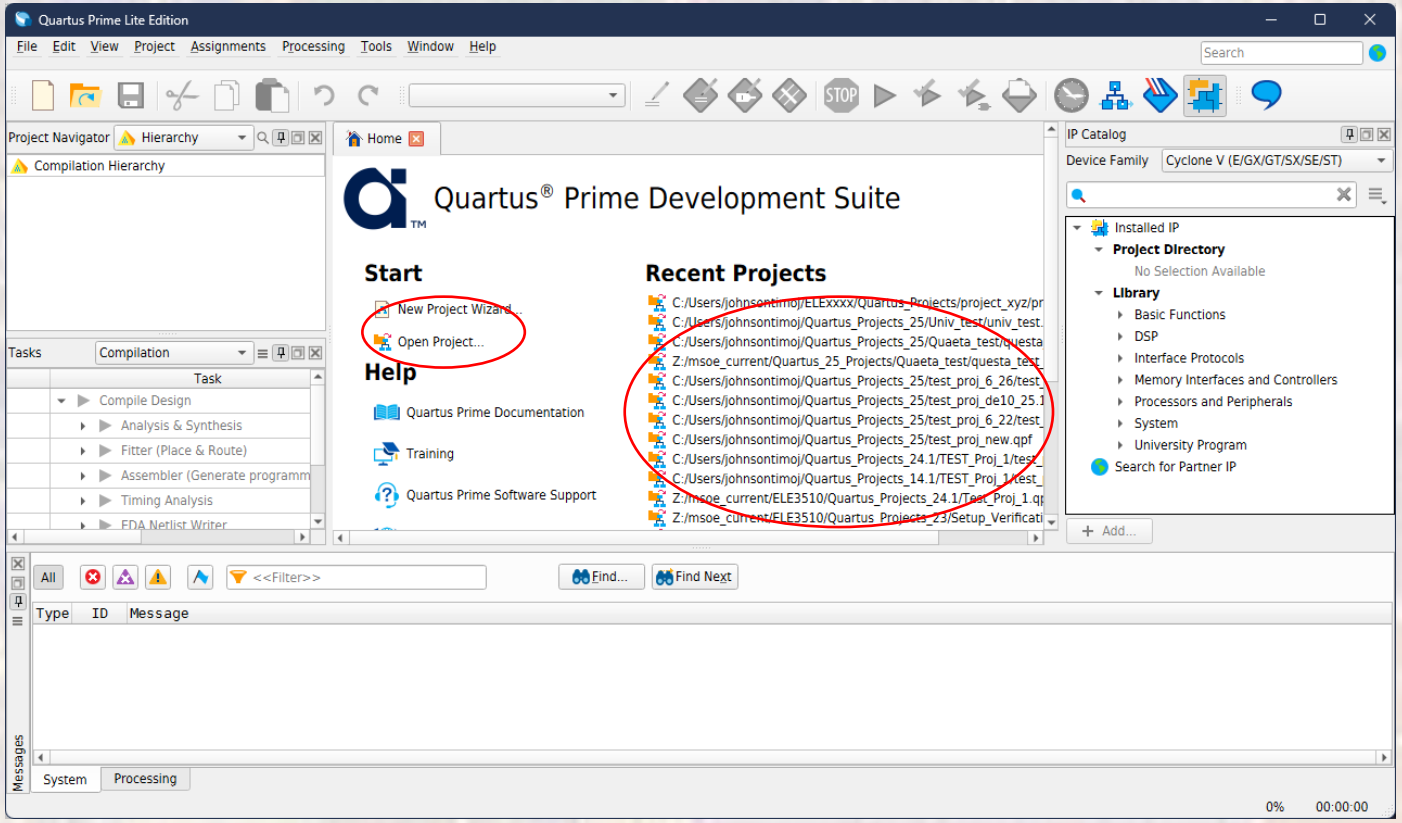
Quartus Project Setup

- Hierarchy
  - Each project must be in it's own folder
  - To create a new project folder
    - Do this for every new project
    - create a new folder in your ELE3510/Quartus_Projects folder
    - Use appropriate names
      - Lab2_Project
      - HW11_Vending_Machine

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Quartus Project Setup

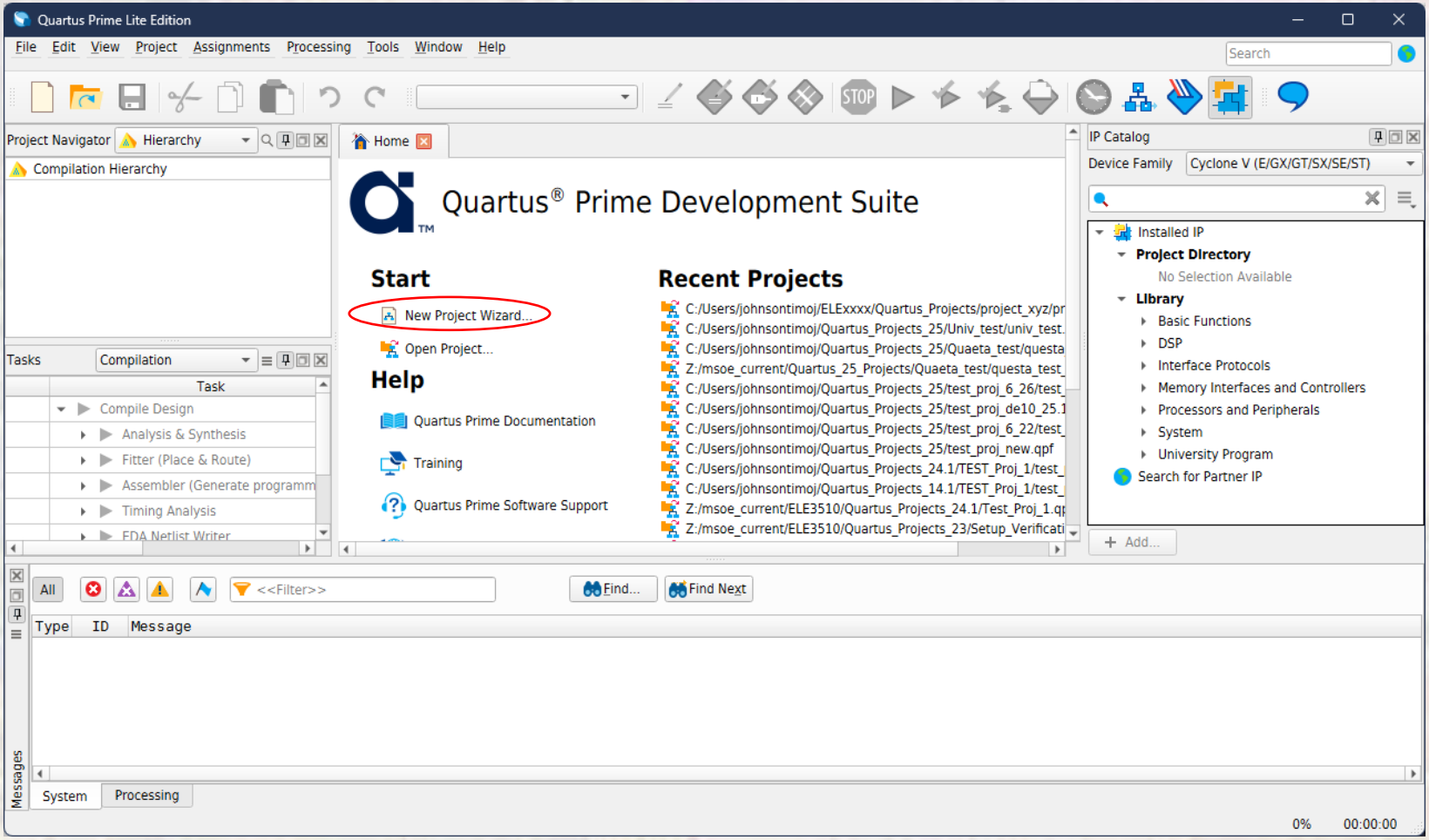
- Quartus Startup
  - When you start Quartus it will ask you to open a new or existing project
  - It also lists recent projects to choose from



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Quartus Project Setup

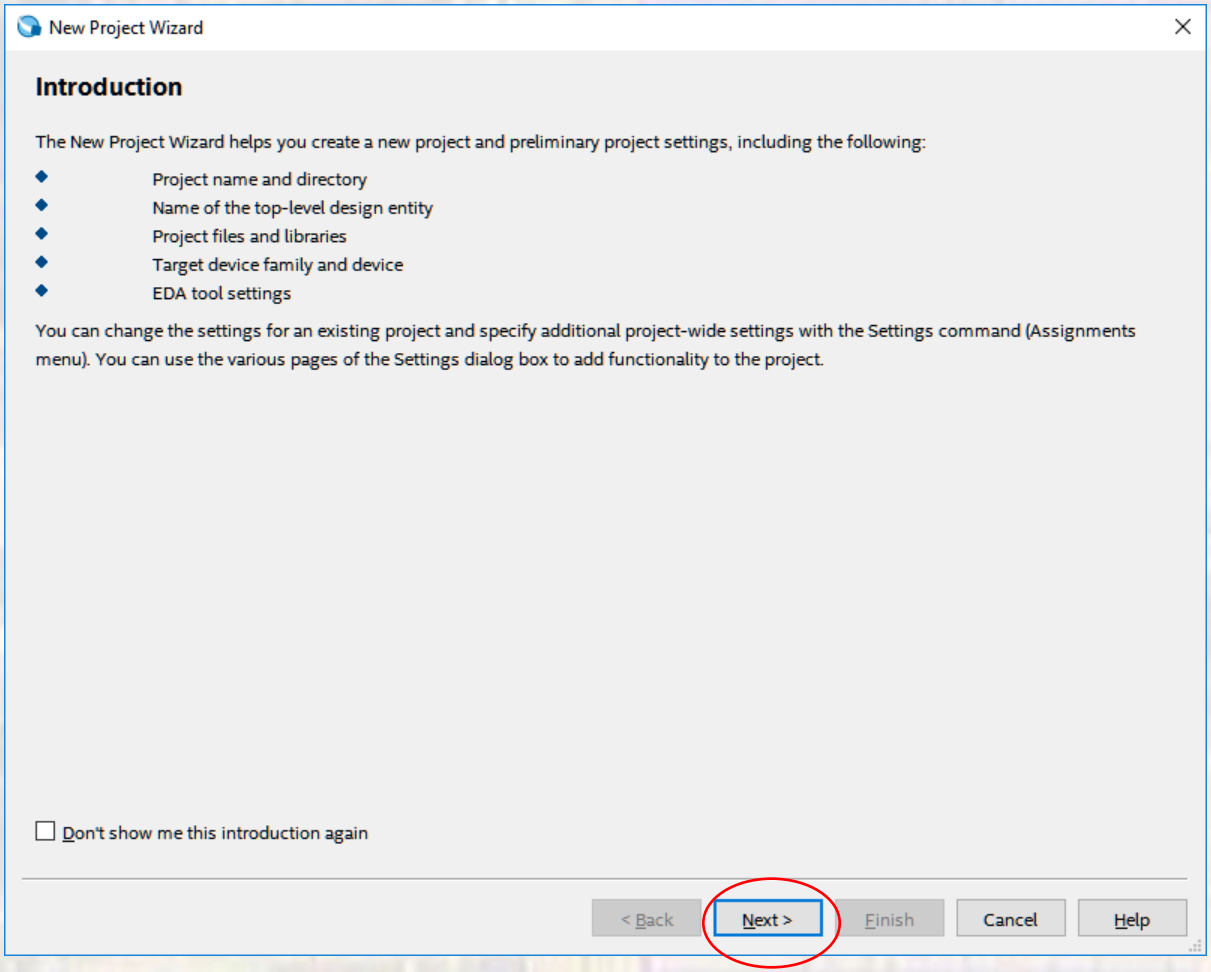
- Quartus Startup
  - Select New Project Wizard



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Quartus Project Setup

- Quartus Startup
  - Select Next



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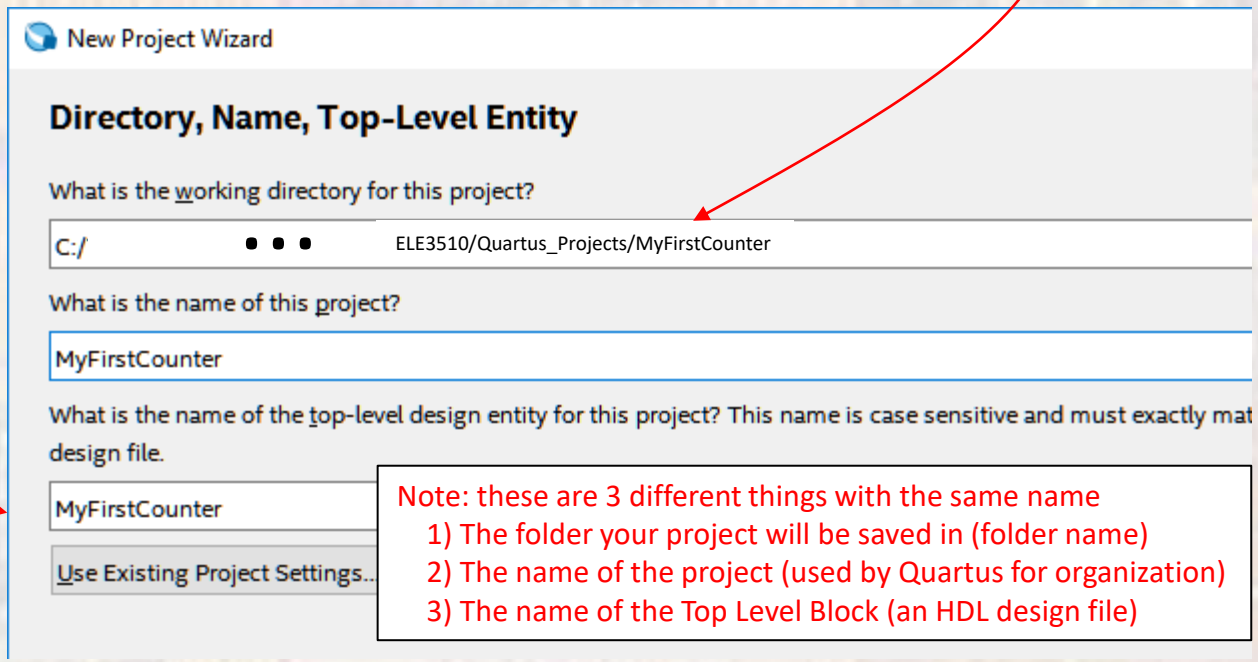
Quartus Project Setup

- Project Names
  - Select your previously created project directory
  - Name your project
  - Name your top level entity (top level block)
    - Your project name and top level entity name should be the same
  - Click Next

1

2

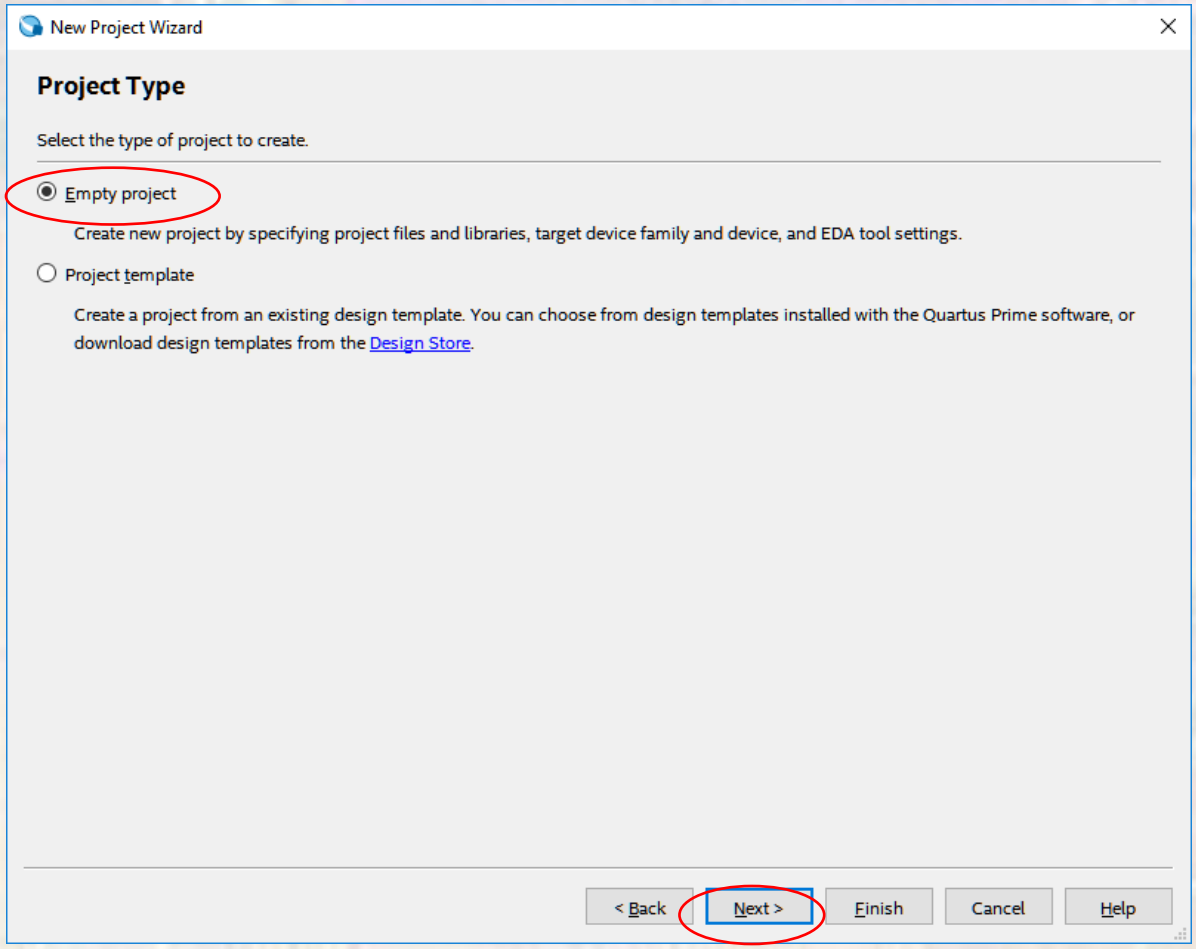
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Quartus Project Setup

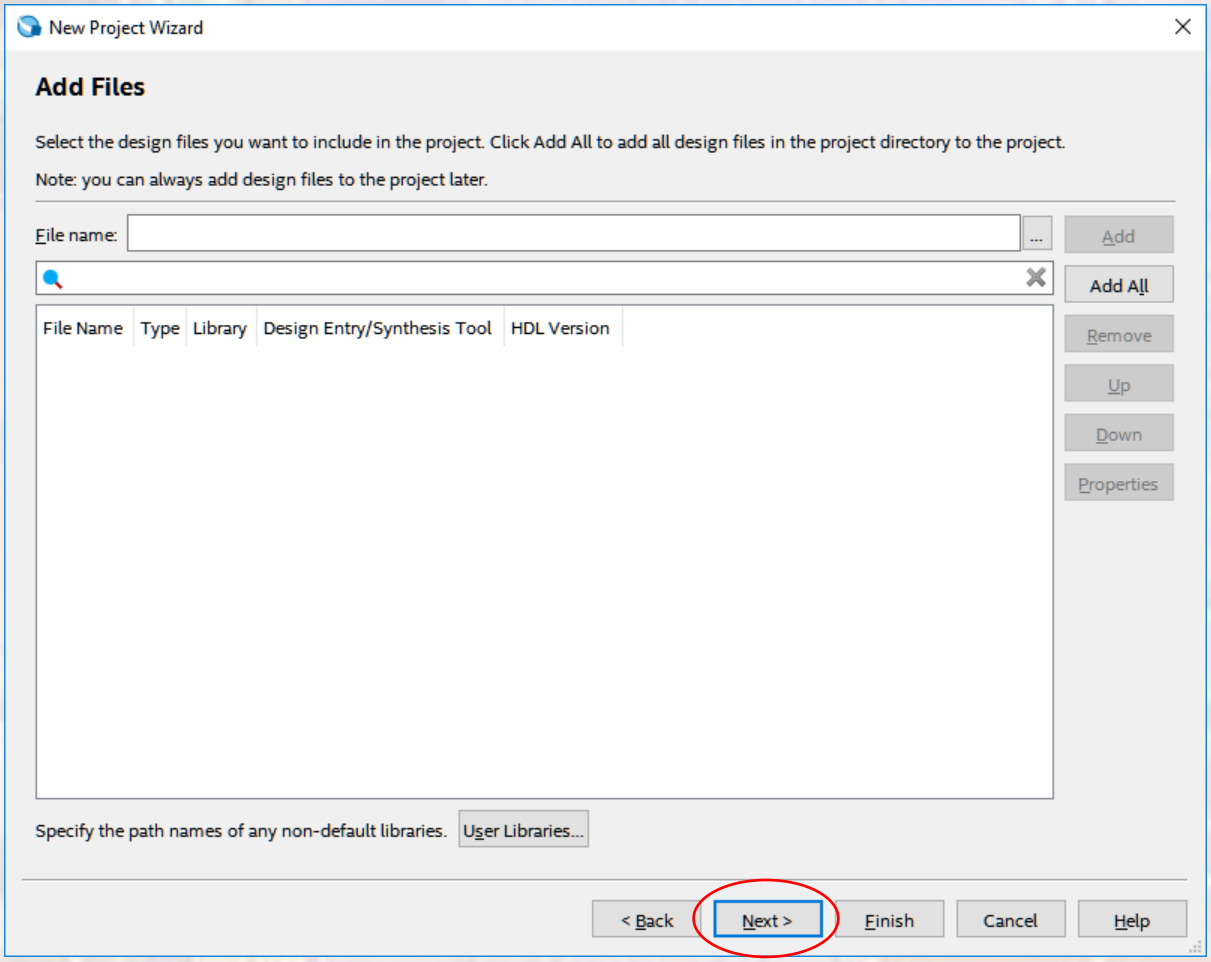
- Start with an Empty project
  - Select Empty project
  - Click Next



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Quartus Project Setup

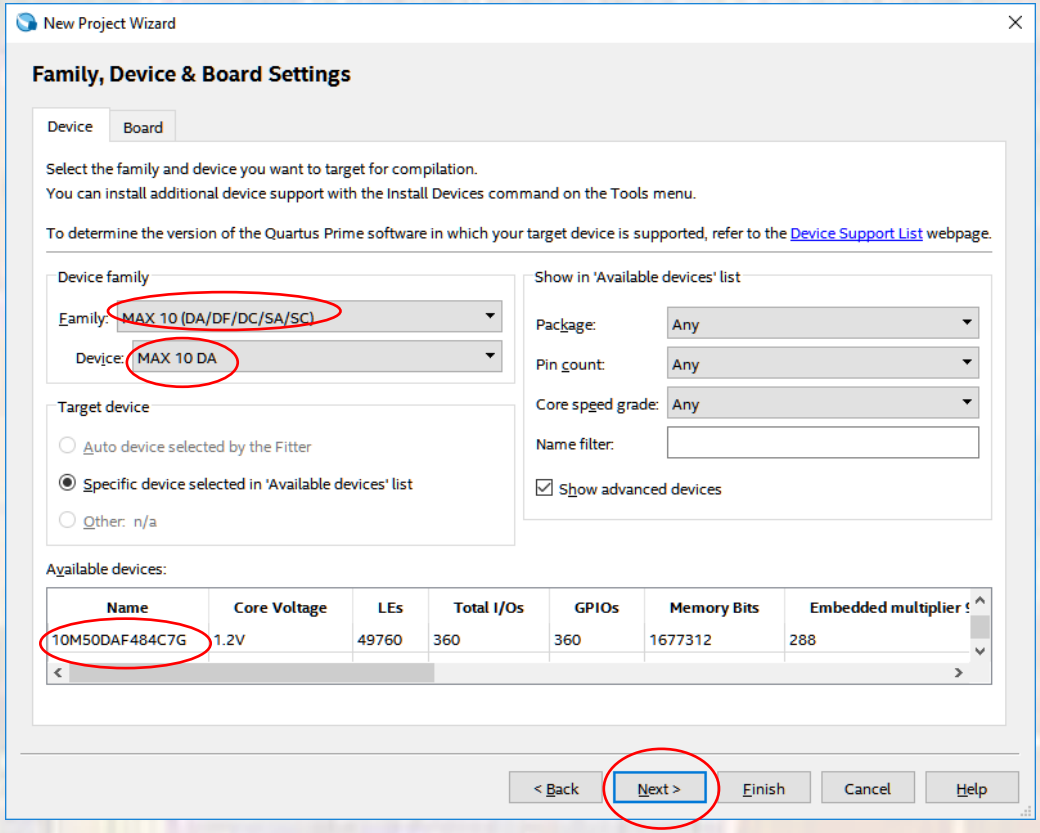
- Start with an Empty project
  - We will not add any files right now
  - Click Next



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Quartus Project Setup

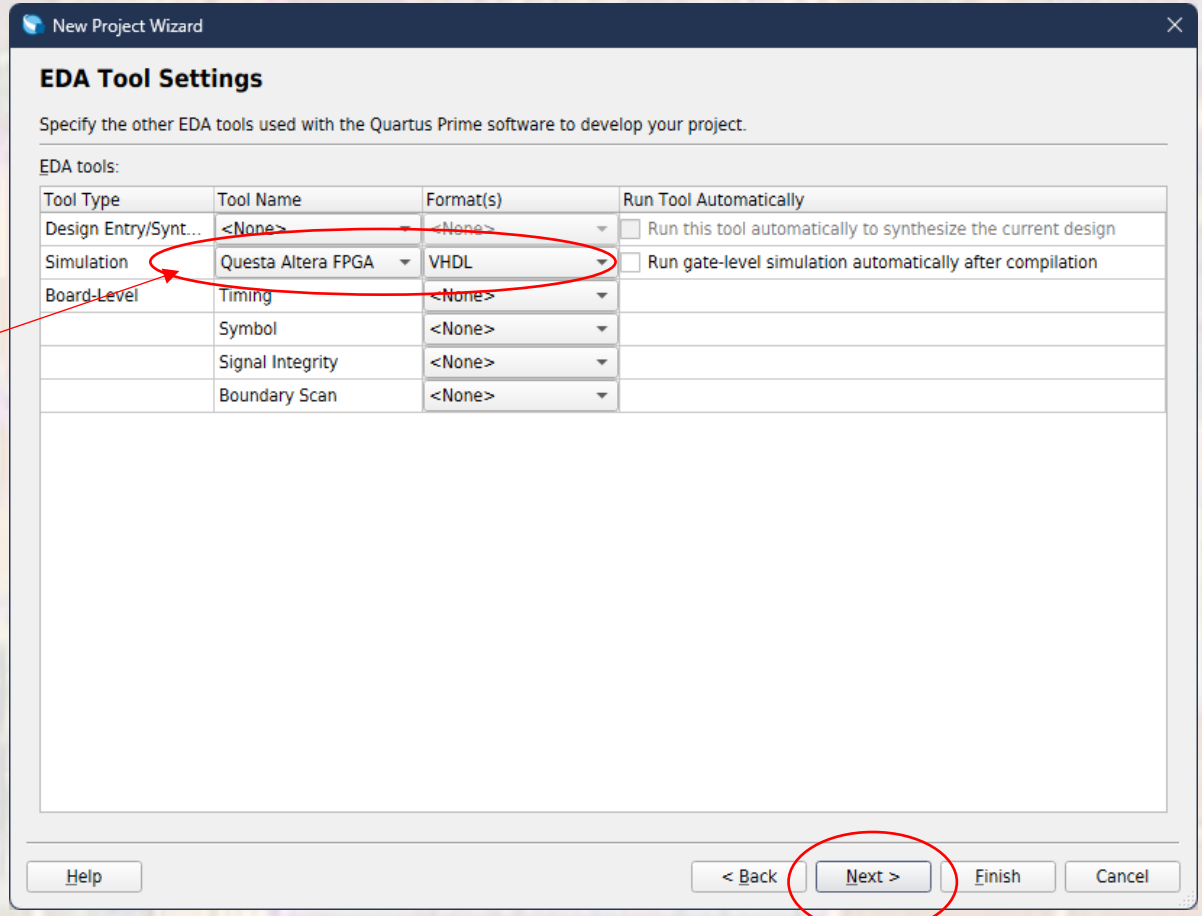
- Device Information
  - Select Max 10 (DA/DF/DC/SA/SC) under Family
  - Select Max 10 DA under Device
  - Scroll down and select 10M50DAF484C7G under Available devices
  - Click Next



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Quartus Project Setup

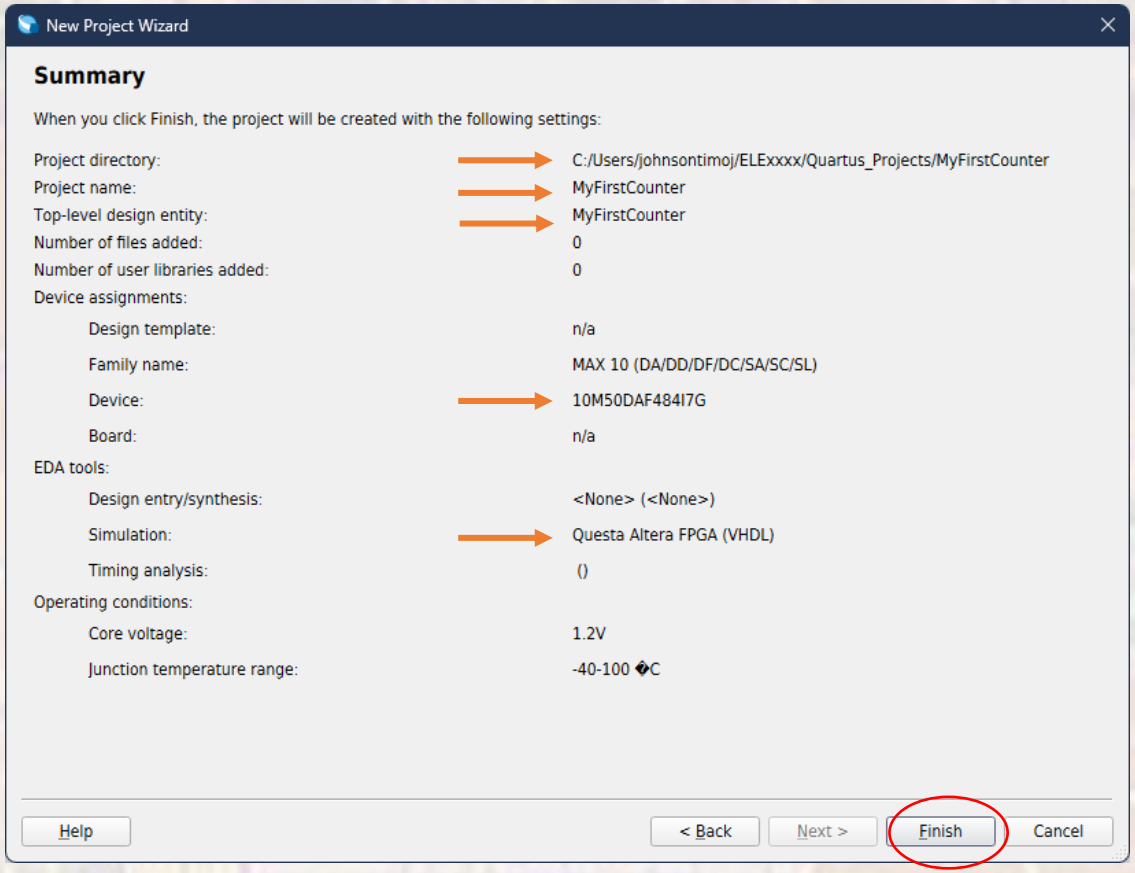
- Tool Settings
  - Under simulation – select Questa Altera FPGA and VHDL
  - Click Next



Note: Questa Altera_FPGA not Questa

Quartus Project Setup

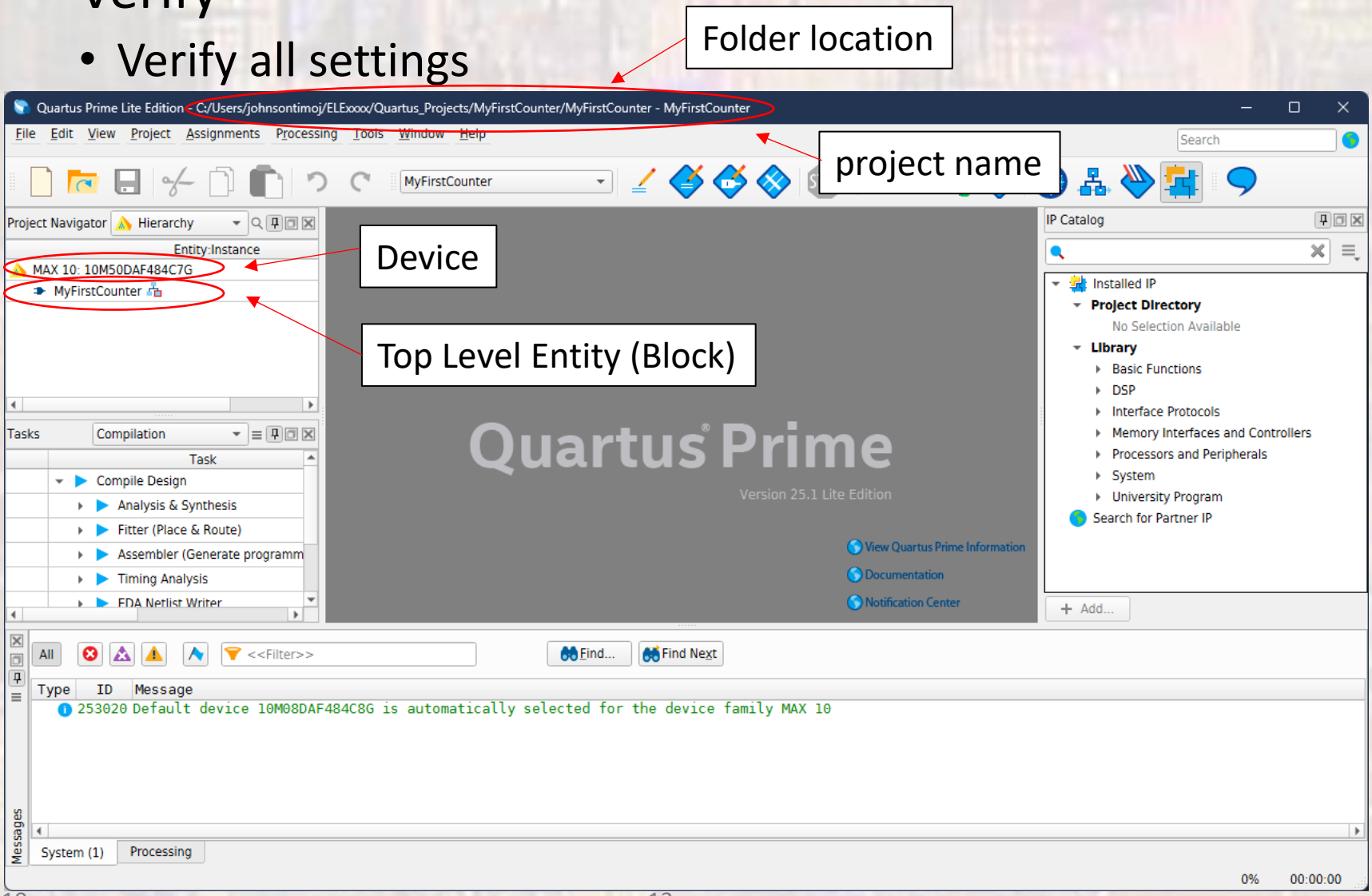
- Verify
  - You will get a summary window
  - Check the values
  - Click Finish



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Quartus Project Setup

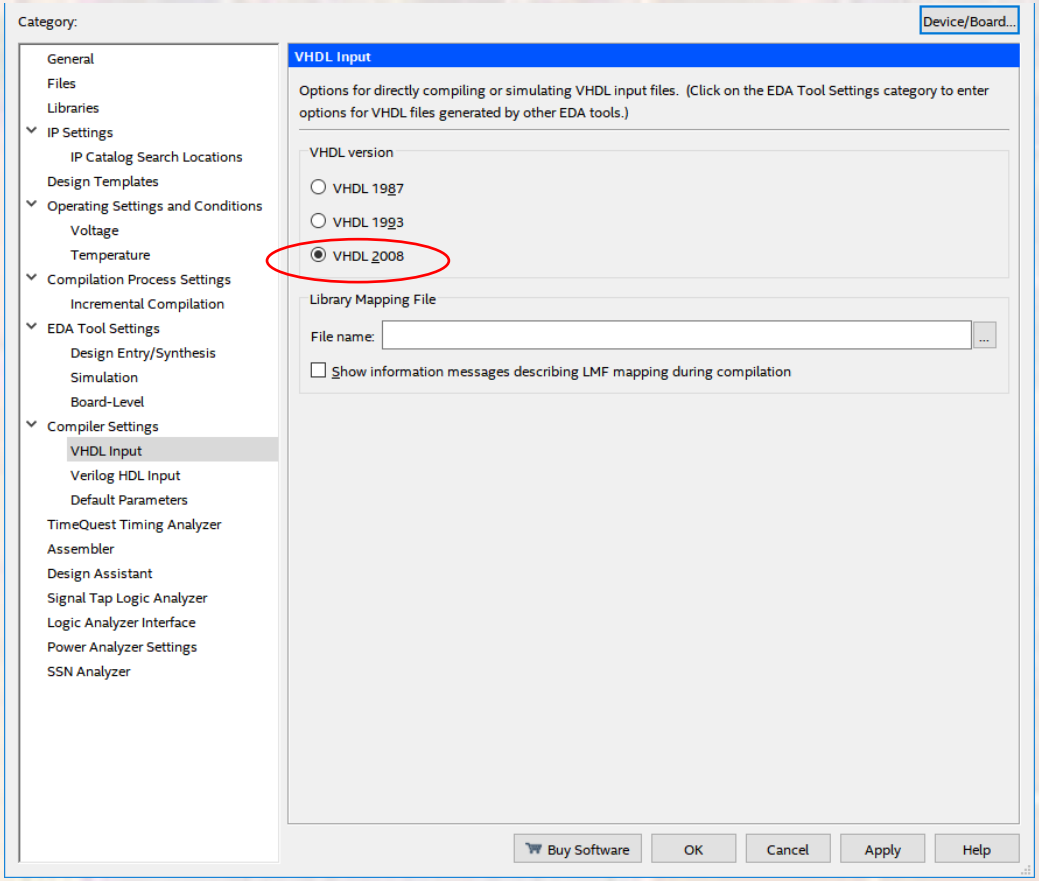
- Verify
  - Verify all settings



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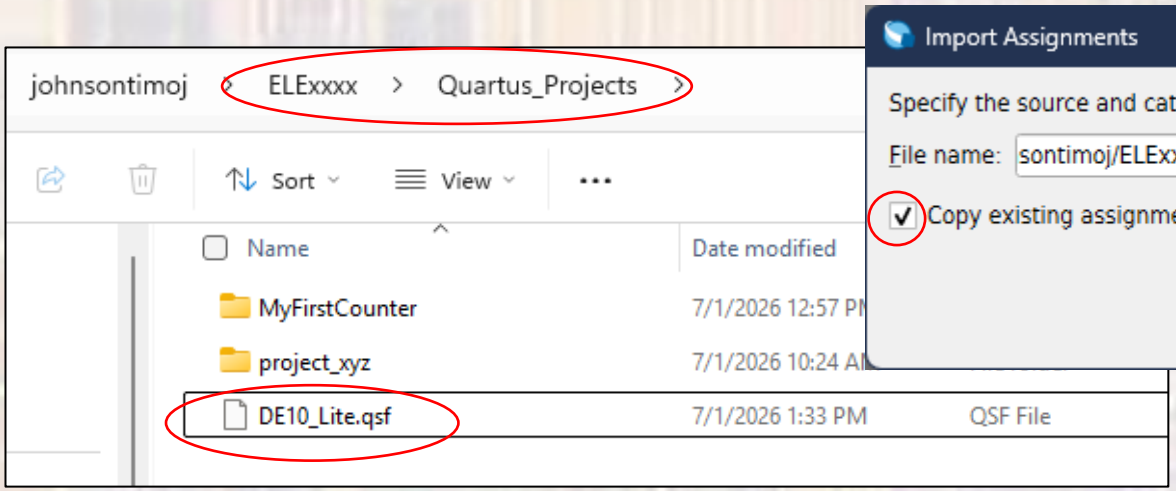
Quartus Project Setup

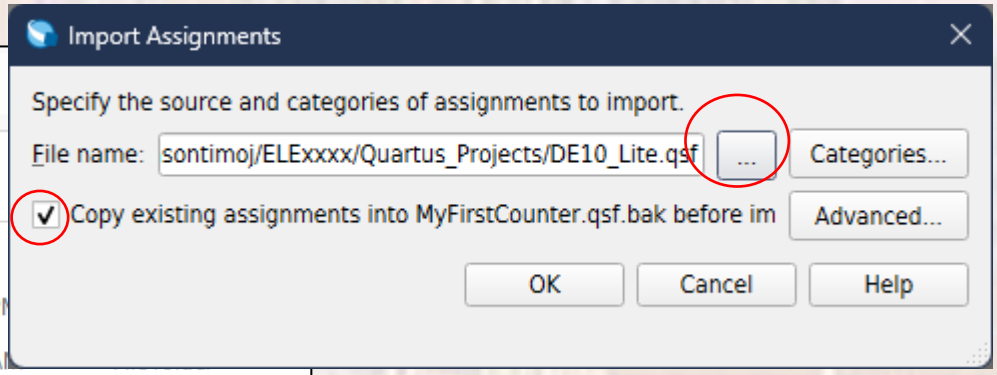
- Additional Settings
  - We will be using the 2008 version of VHDL
  - Assignments -> Settings -> Compiler Settings -> VHDL Input
    - Select VHDL 2008



Quartus Project Setup

- QSF (Pin Planner) Setup
  - You should have previously downloaded the DE10_Lite.qsf file from the Quartus Project FileSystem Setup slides
  - Do this for each new project
  - Assignments -> Import Assignments
    - Click … next to File name
    - Traverse and select the downloaded DE10_Lite.qsf file located up one level from your current project directory





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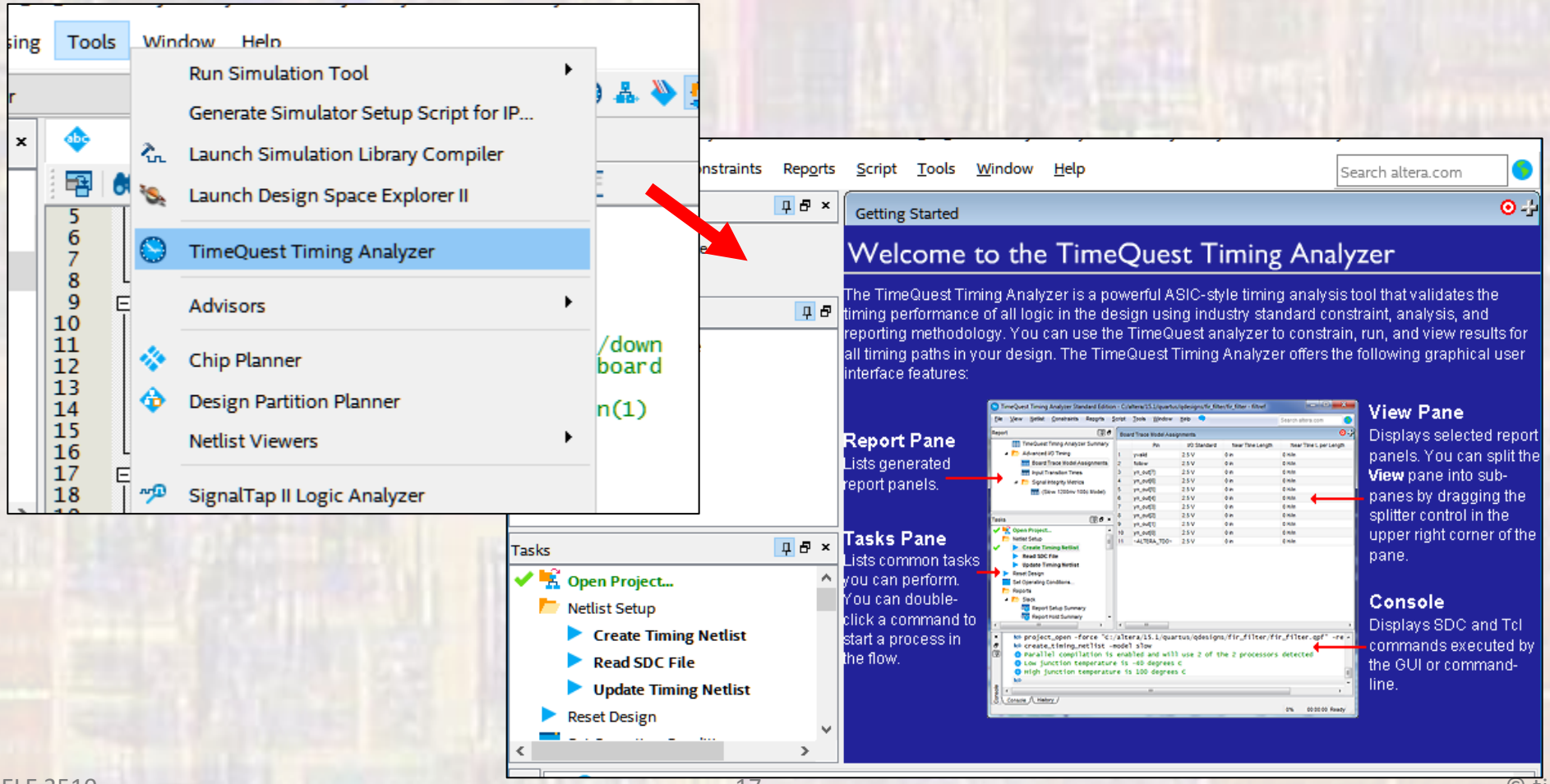
Quartus Project Setup

- Timing Analysis Setup
  - Timing
    - Proper placement and routing requires that the design meets a set of timing requirements
    - A very basic set of timing requirements is available in the file Basic_SDC.sdc on the web site
    - You will use this as a starting point for each project you create
  - Do this for each project

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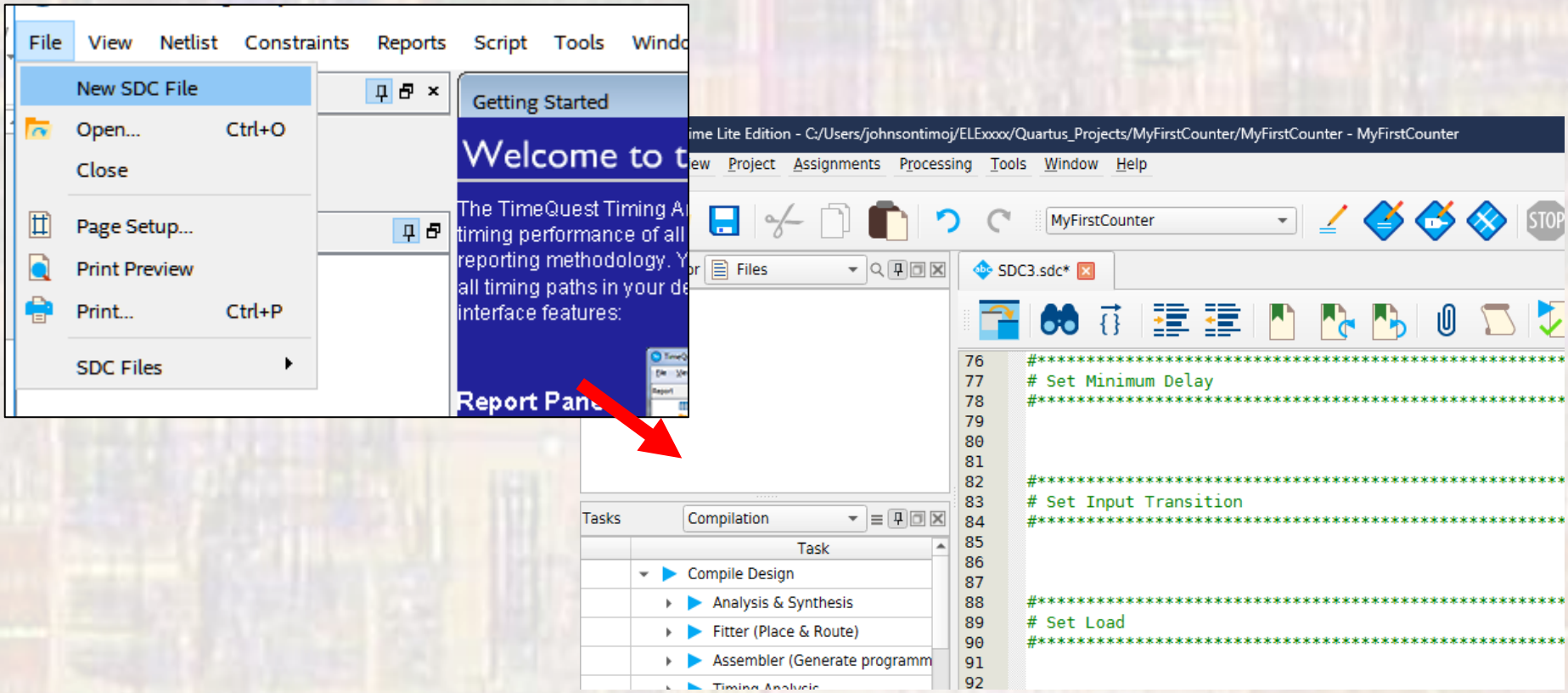
Quartus Project Setup

- Timing Analysis Setup
  - Select Tools -> TimeQuest Timing Analyzer



Quartus Project Setup

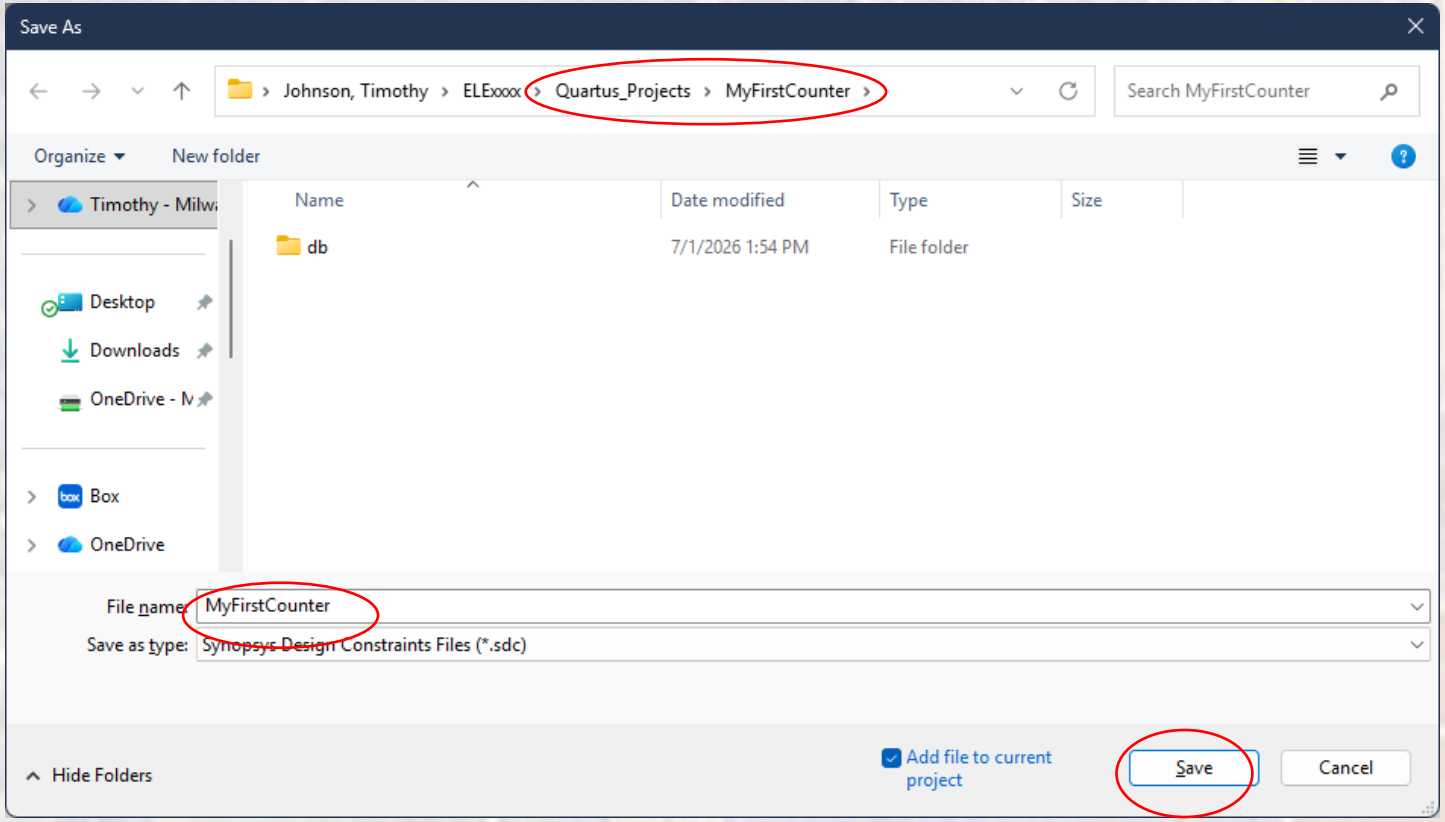
- Timing Analysis Setup
  - Select File -> New SDC File
  - Copy and paste the contents of Basic_SDC.sdc from the website into the file



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Quartus Project Setup

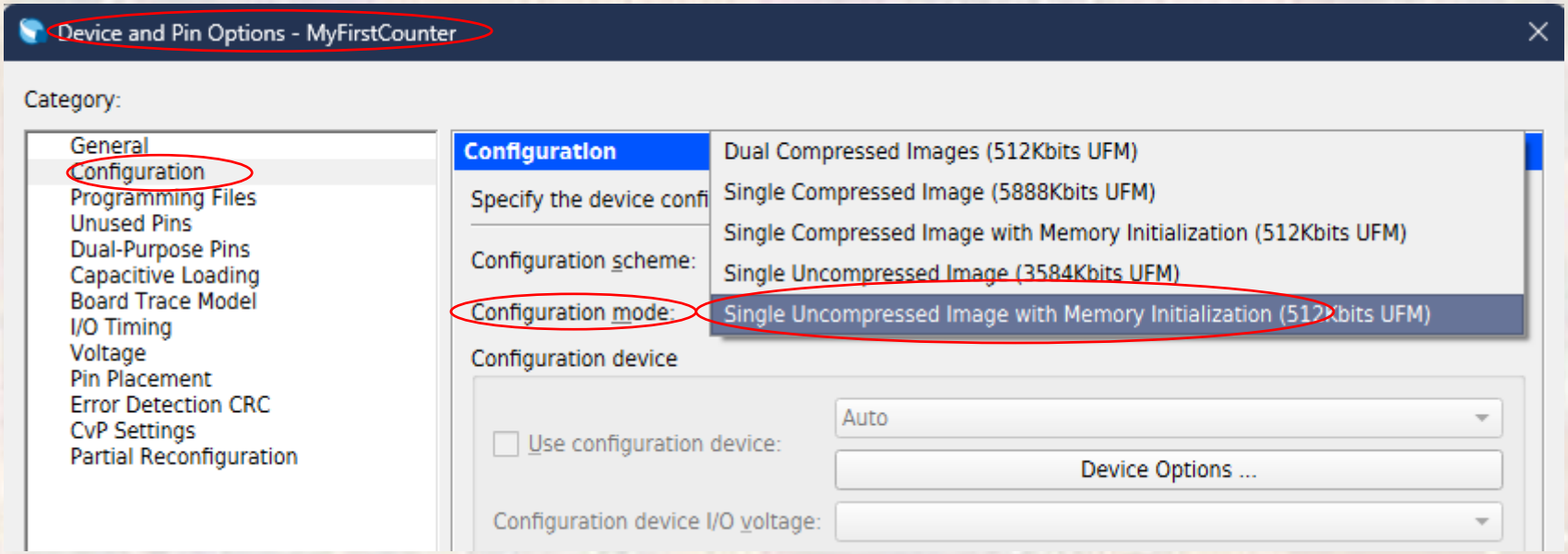
- Timing Analysis Setup
  - Select File -> Save As
  - Name the file the same as your project name
  - Save and close the TimeQuest window



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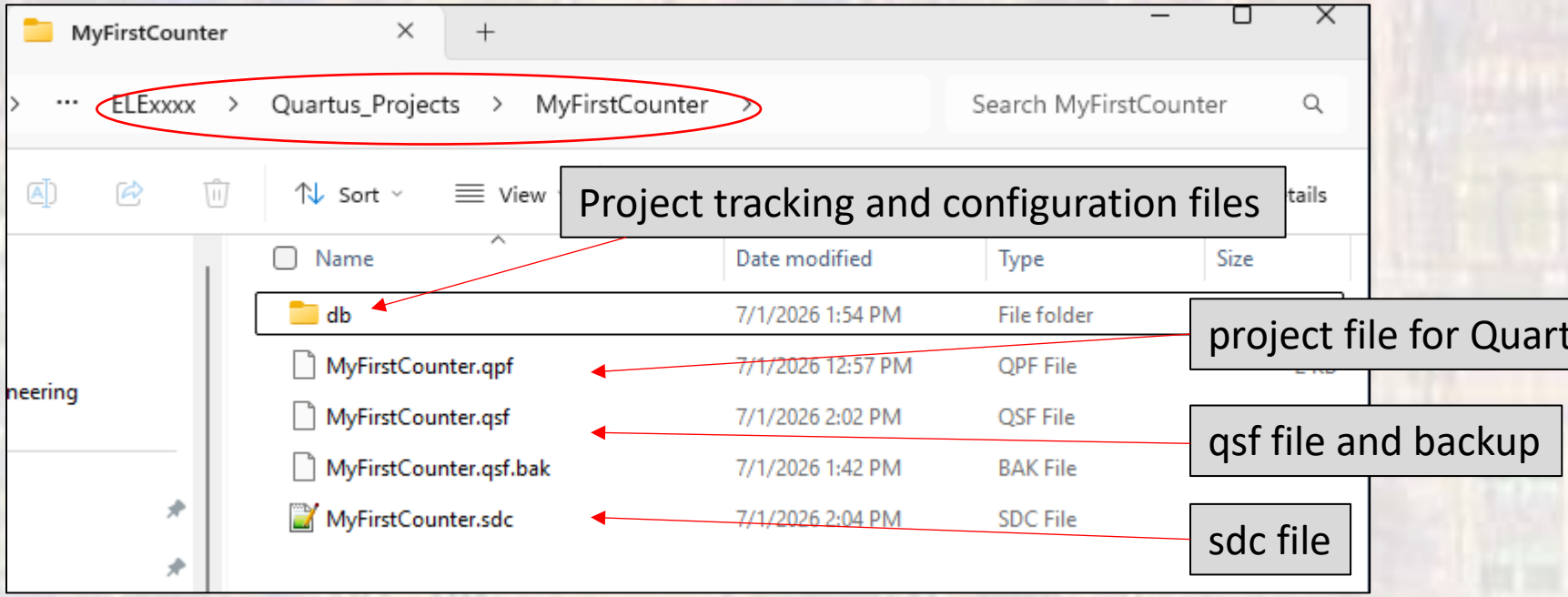
Quartus Project Setup

- Memory Configuration Setup
  - Configure the tools for the DE10_Lite board
    - This is not required until we start using the NIOS-V processor
    - Select Assignments → Device → Device and Pin Options → Configuration → Configuration Mode
    - Select single uncompressed Image with Memory Initialization



Quartus Project Setup

- Verify
  - Your project directory in Windows should look like this



  - Your project is ready to use

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