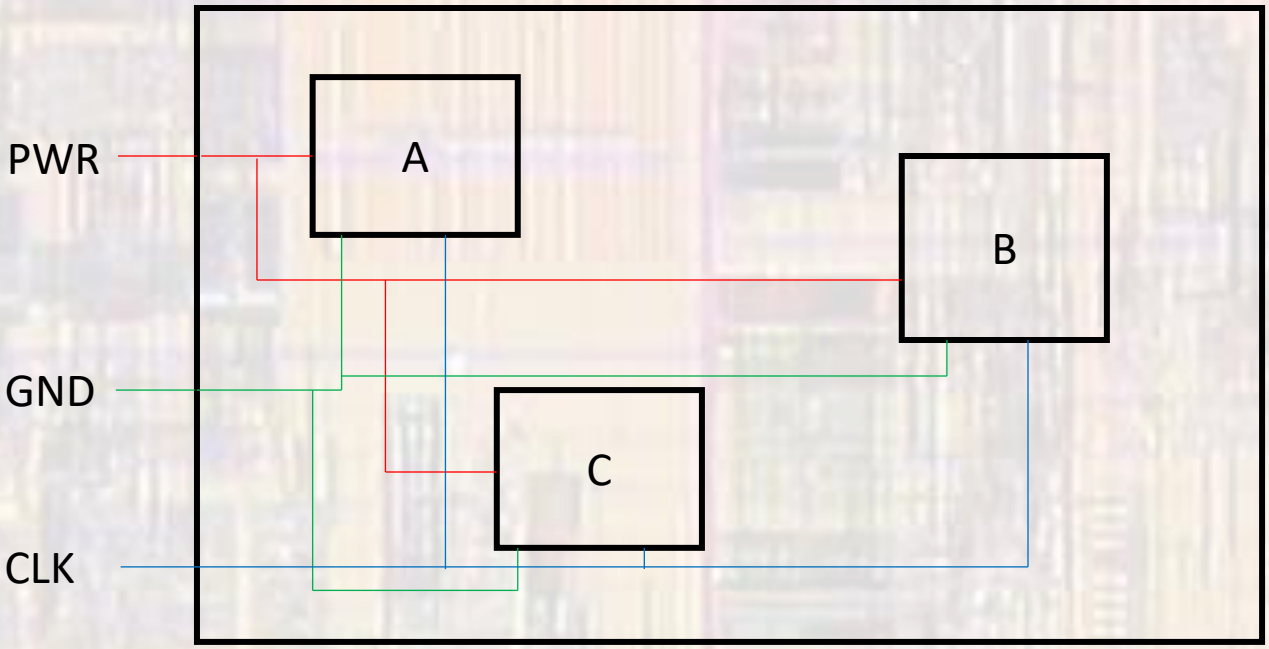
Reset_bar

Last updated 1/9/24

Reset_bar

- Why are we using resetB instead of just reset?
  - Consider a system – could be on a chip, a board, or across multiple boards



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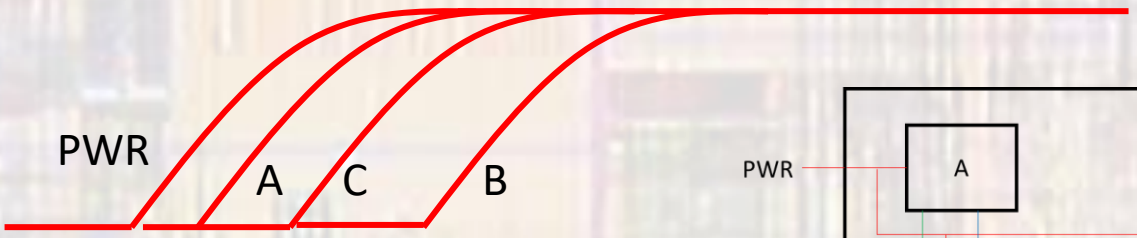
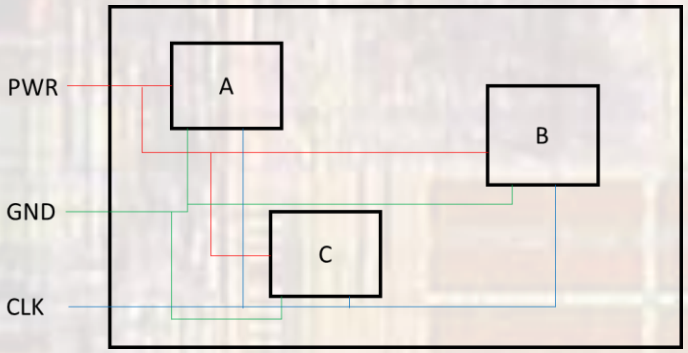
- Why are we using resetB instead of just reset?
  - When the system is powered up there is a finite time associated with the rising supply voltage
  - Due to inherent impedances (C and R), the signal is received at different blocks at different times





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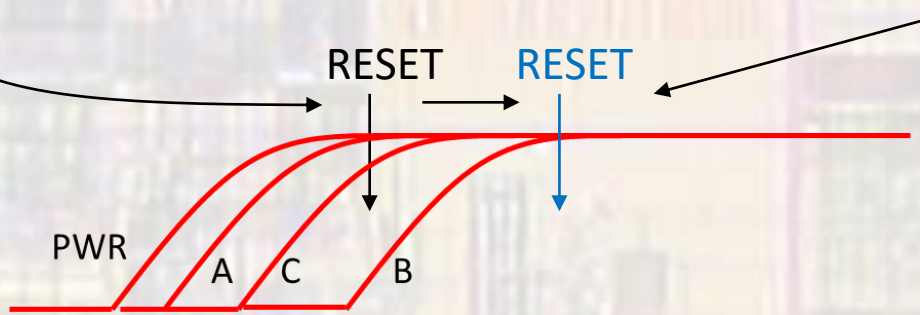
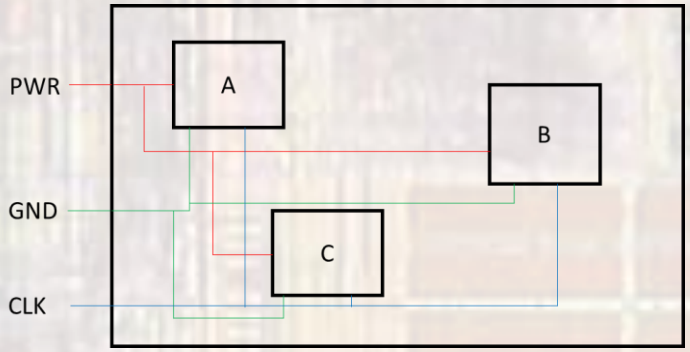
- Why are we using resetB instead of just reset?
  - Active High Reset – Case 1
  - Somewhere in the system – the reset signal must be generated
    - If it were generated by block A, it is possible the reset signal would be released before block B stabilized (or even had power)
    - If that happens, block B would not be reset, and all the registers would have random values
  - We could resolve this by slowing down the reset signal





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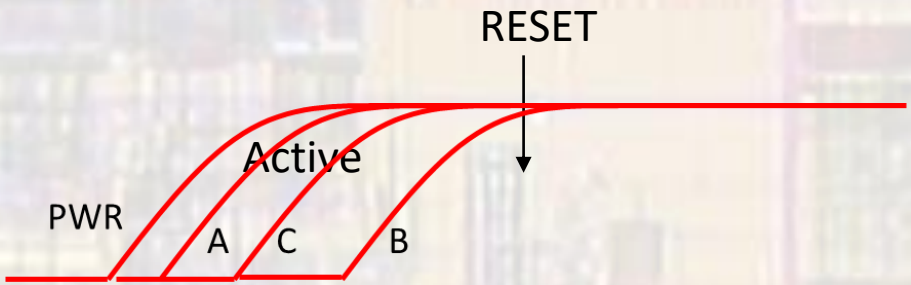
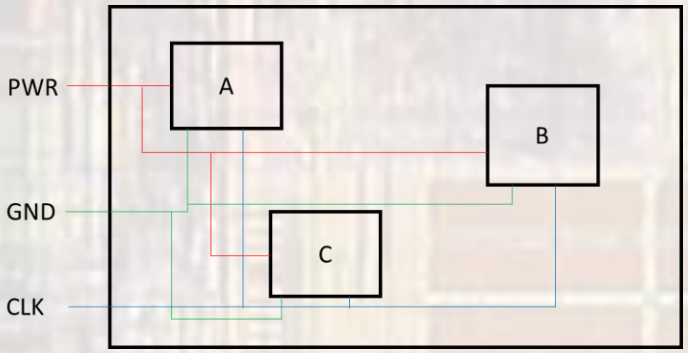
- Why are we using resetB instead of just reset?
  - Active High Reset – Case 2
  - Somewhere in the system – the reset signal must be generated
    - If it were generated by block B, blocks A and C could be powered up
    - Block B would still be unpowered → Reset = 0
    - Blocks A and C would be active – bad things could happen
  - Slowing down the Reset signal (case 1 solution) does not help this situation





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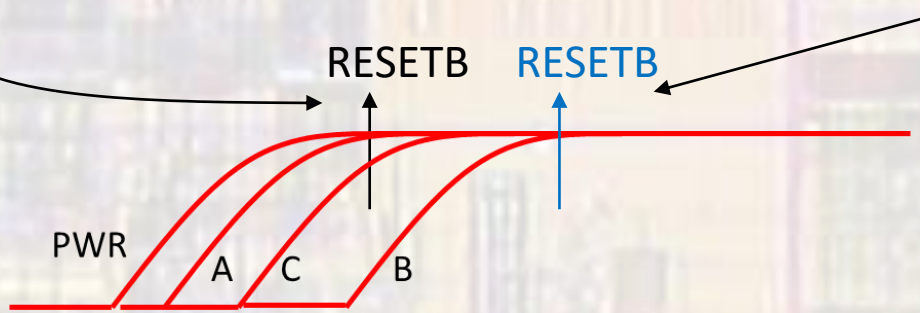

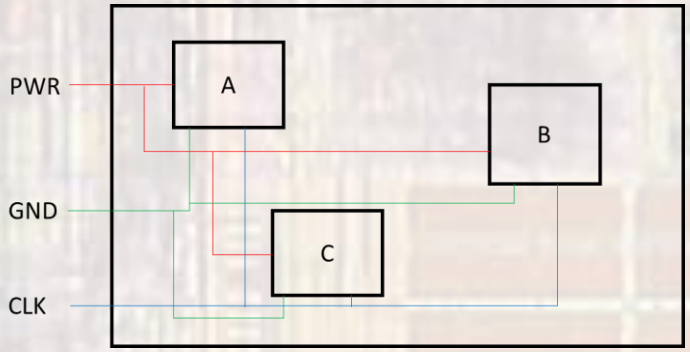

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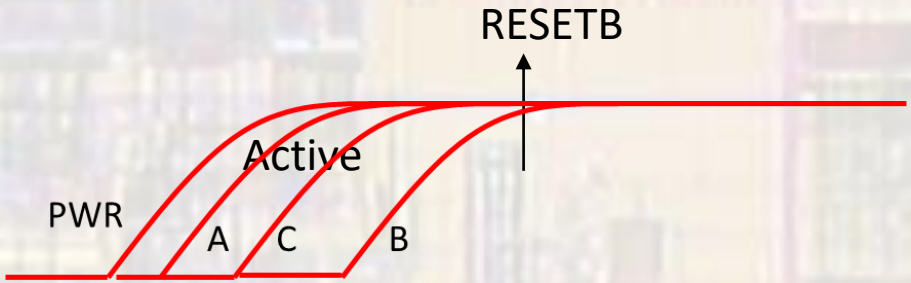
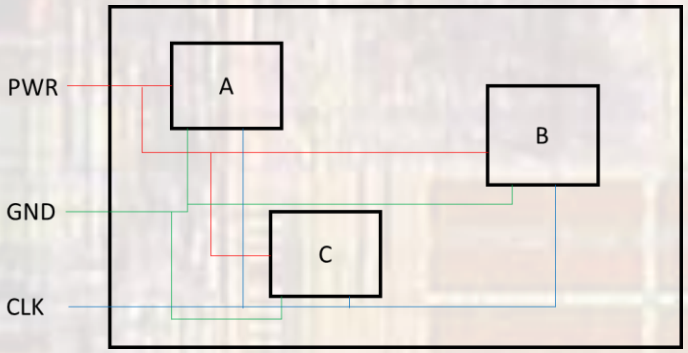
  - Active Low Reset – Case 2
  - Somewhere in the system – the resetB signal must be generated
    - If it were generated by block B, blocks A and C could be powered up
    - Block B would still be unpowered → Reset = 0
    - Blocks A and C would be in reset → No problem
  - Slowing down the Reset signal (case 1 solution) does not impact this situation





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- Why are we using resetB instead of just reset?
  - A slowed down resetB signal works in both situations
  - Solution
    - Tie a large capacitor to the resetB signal
    - Design the capacitor to ensure ALL supplies are stable before the resetB signal reaches 10% of the supply voltage