Sequential Logic Review

Last updated 7/13/23

Sequential Logic Review

- Logical world
  - Basic Signal Values
    - 1, 0
    - High Low
    - True False
    - Set Reset
  - Additional values
    - X, x = don't care
    - U, u = unknown

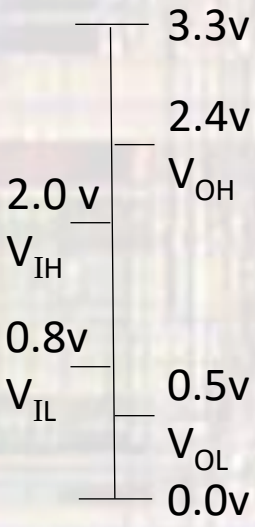
Sequential Logic Review

- Physical world
  - Voltage levels
    - System/Circuit dependent (V_{DD}, Gnd)
    - Ideal:

3.3v System	'1' = 3.3v	'0' = 0.0v
1.8v System	'1' = 1.8v	'0' = 0.0v
1.2v System	'1' = 1.2v	'0' = 0.0v

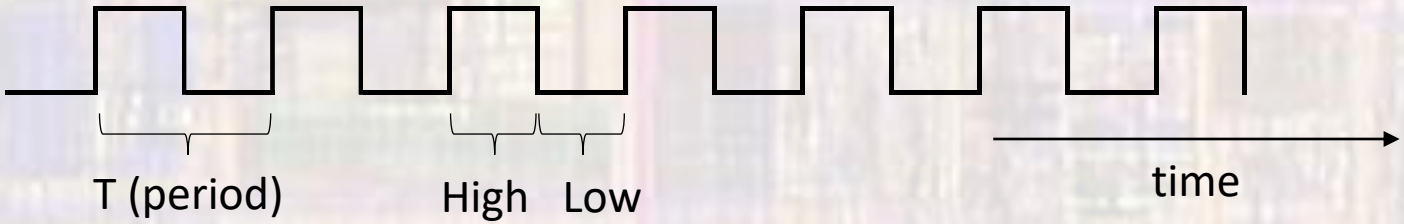
    - Real world:

3.3v System



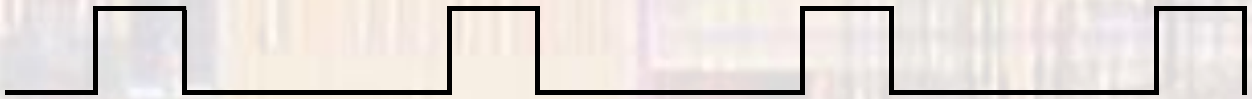
Sequential Logic Review

- Clock Systems

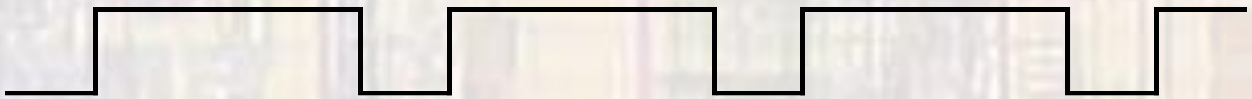


F (frequency) = 1/T Duty Cycle = High / T

50MHz <-> 20nS High = 10ns, Low = 10ns



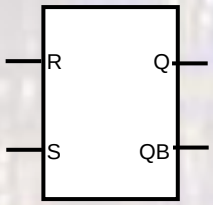
25% duty cycle, 12.5Mhz

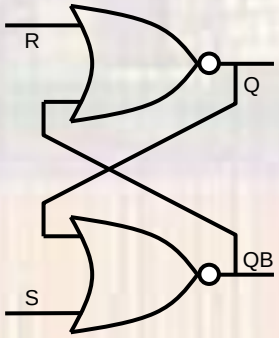


75% duty cycle, 12.5MHz

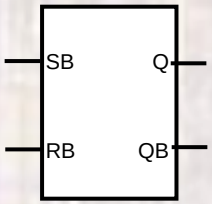
Logic Review

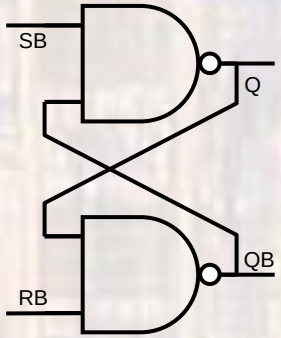
- Latches





S	R	Q	QB
0	0	No change	No change
0	1	0	1
1	0	1	0
1	1	0	0

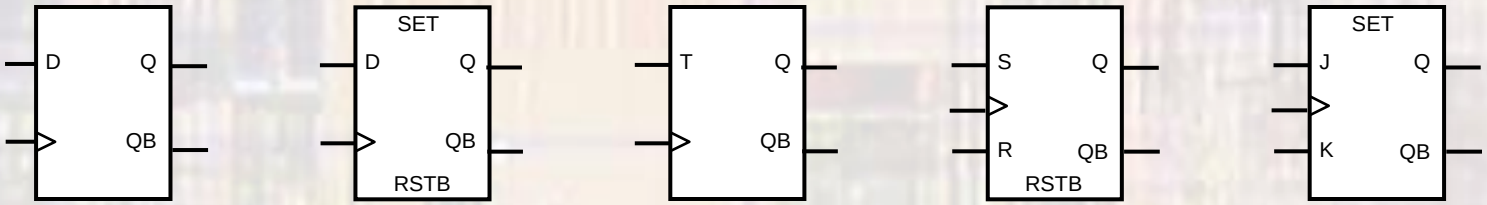




SB	RB	Q	QB
0	0	1	1
0	1	1	0
1	0	0	1
1	1	No change	No change

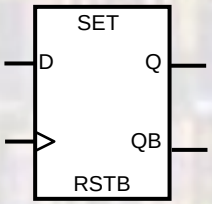
Logic Review

- Flip-Flops
  - Edge Triggered
    - Outputs only change on a rising or falling clock edge (synchronous)
    - Outputs depend on the state of the inputs at the clock edge
  - Some have asynchronous set or reset inputs



Logic Review

- Flip-Flops
  - Edge Triggered D Flip-Flop
    - Outputs depend on the state of the inputs at the rising clock edge
  - Some have asynchronous set or reset inputs

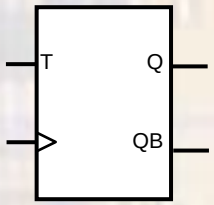


Set	Reset Bar	D		Q	QB
0	1	**0**		0	1
0	1	**1**		1	0
1	1	x		1	0
0	**0**	x		0	1

D at the rising clock edge

Logic Review

- Flip-Flops
  - Edge Triggered T Flip-Flop (Toggle)
    - Outputs depend on the state of the inputs at the rising clock edge
  - Some have asynchronous set or reset inputs



T	Q	QB
0	Q_{OLD}	QB_{OLD}
1	QB_{OLD}	Q_{OLD}

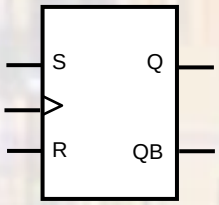
T at the rising clock edge

T	Q	QB
0	No Change	No Change
1	Toggle	Toggle

T at the rising clock edge

Logic Review

- Flip-Flops
  - Edge Triggered SR Flip-Flop (Set/Reset)
    - Outputs depend on the state of the inputs at the rising clock edge
  - Some have asynchronous set or reset inputs

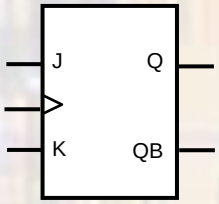


R	S		Q	QB
0	0		Q_{OLD}	QB_{OLD}
0	1		1	0
1	0		0	1
1	1		N/A	N/A

S,R at the rising clock edge

Logic Review

- Flip-Flops
  - Edge Triggered JK Flip-Flop
    - Outputs depend on the state of the inputs at the rising clock edge
  - Some have asynchronous set or reset inputs

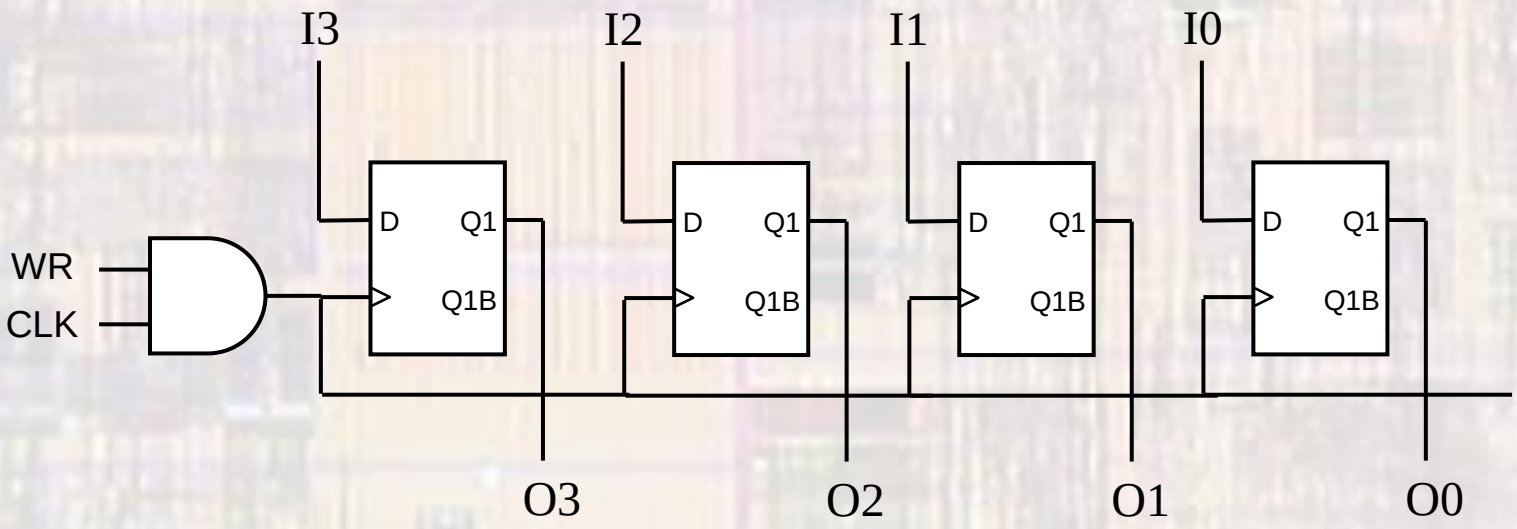


J	K		Q	QB
0	**0**		Q_{OLD}	QB_{OLD}
0	**1**		0	1
1	**0**		1	0
1	**1**		Toggle	Toggle

J,K at the rising clock edge

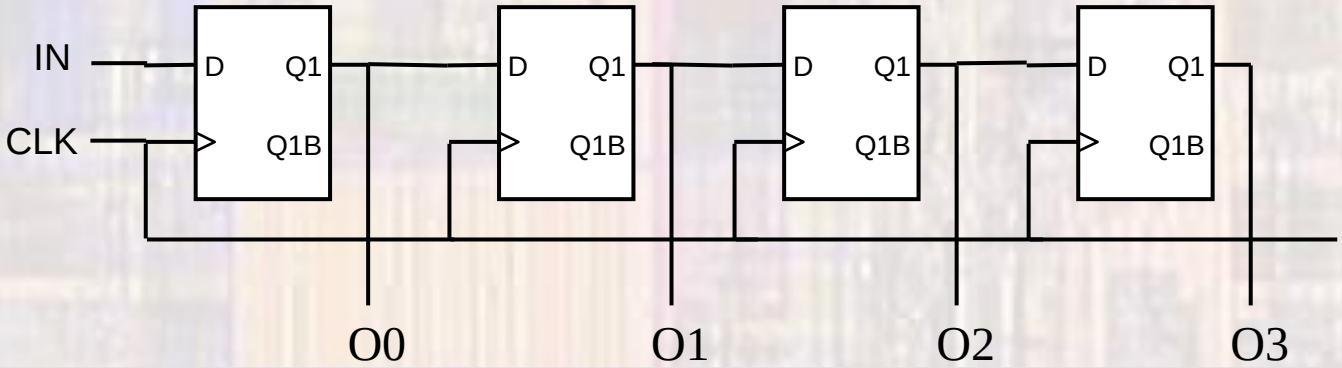
Logic Review

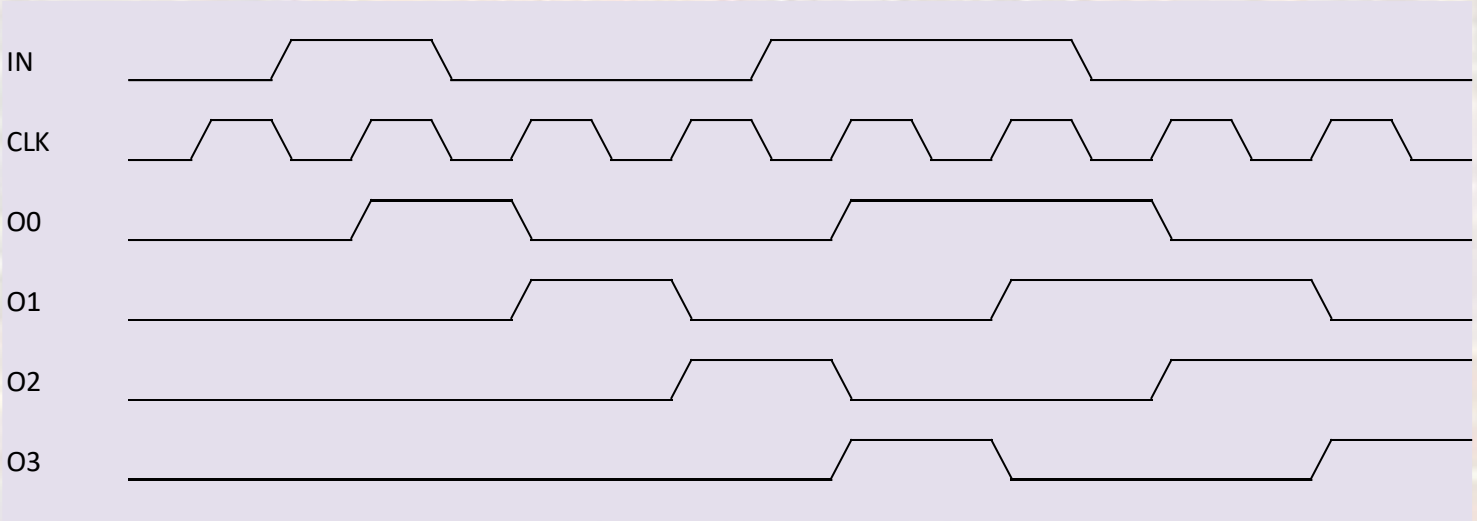
- Parallel Data Register



Logic Review

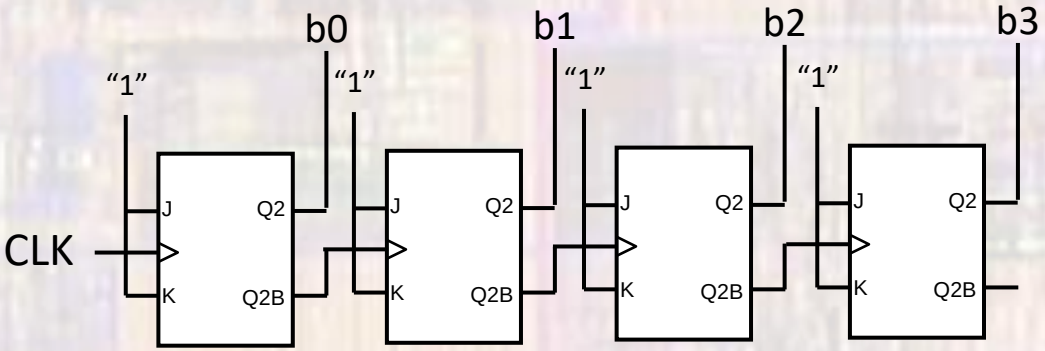
- Shift Register

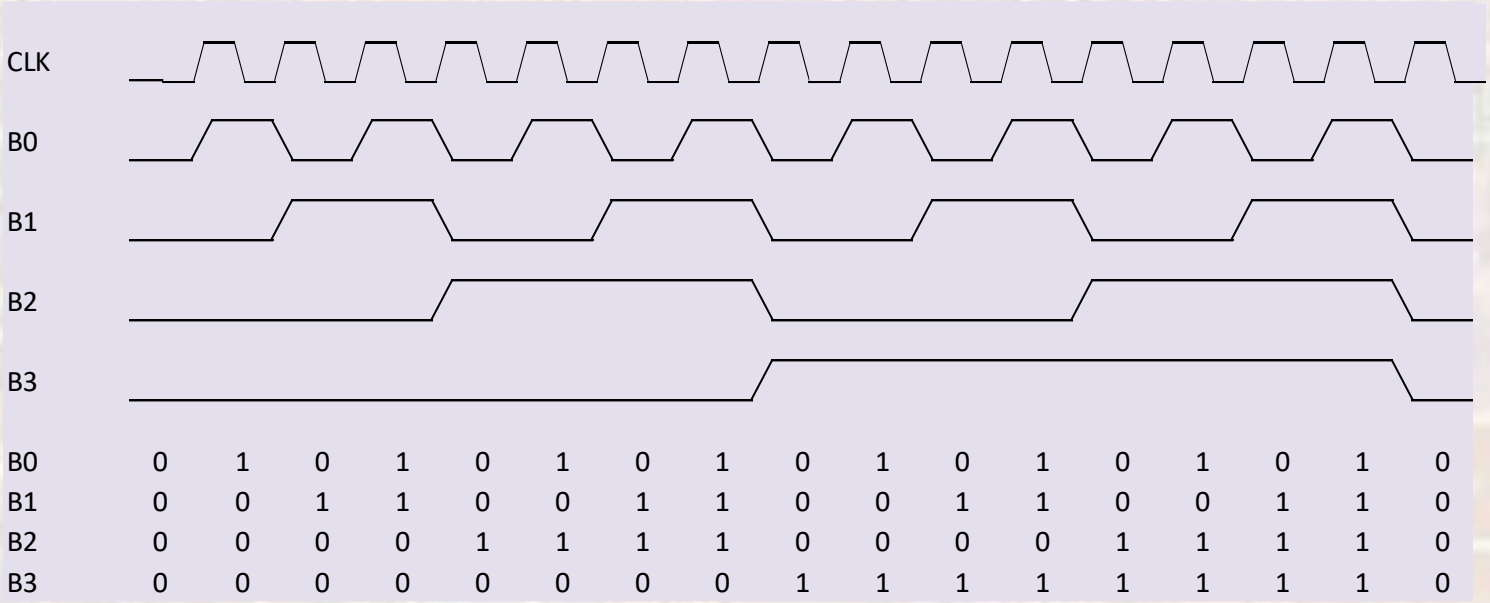




Logic Review

- Counter





B0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
B1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
B2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
B3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0