SignalTap

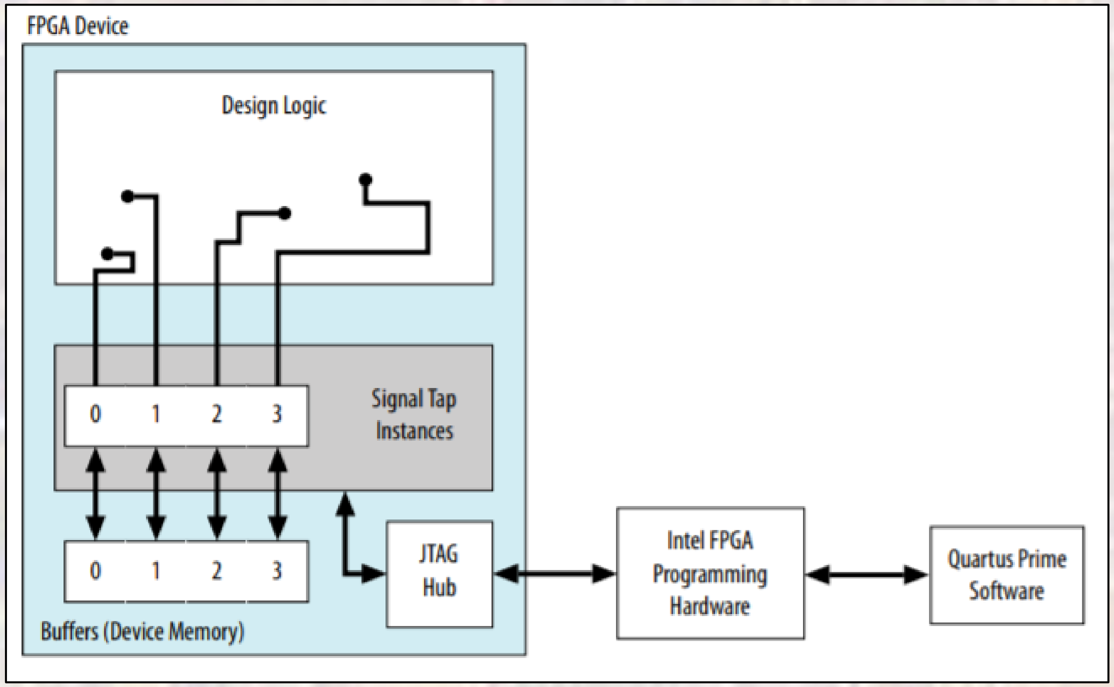
Last updated 7/20/23

SignalTap

- Your simulation showed your design works but your hardware does not work
  - Debug options
    - Review test coverage of simulations
    - Add signals to the design and bring them out to pins to see them
    - Signal Tap

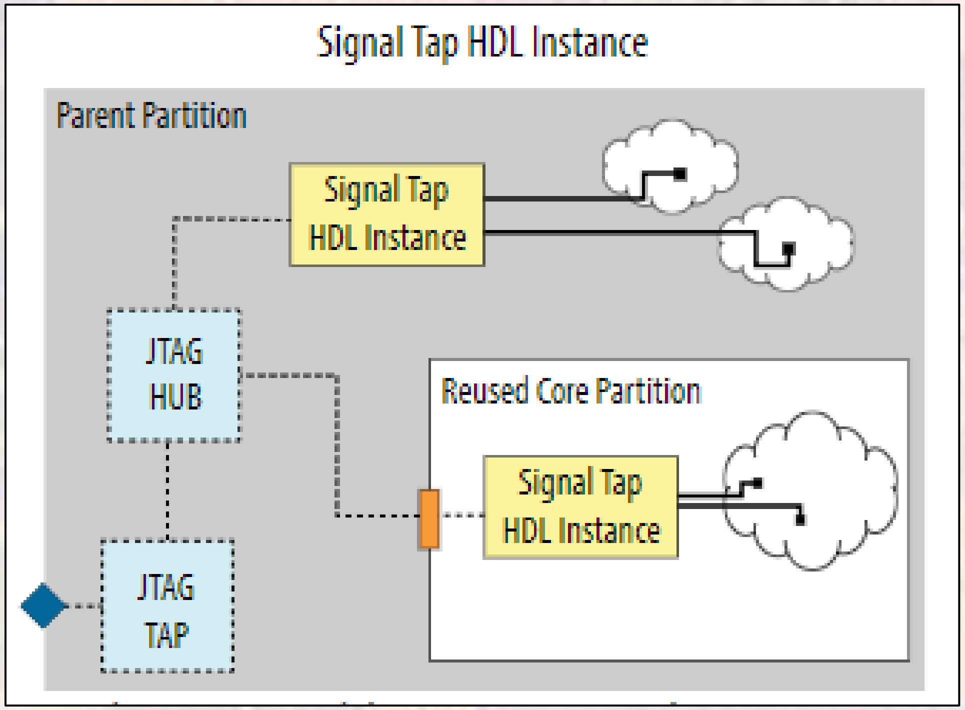
SignalTap

- SignalTap II
  - Embedded Logic Analyzer
  - System-level debugging tool that captures and displays signals



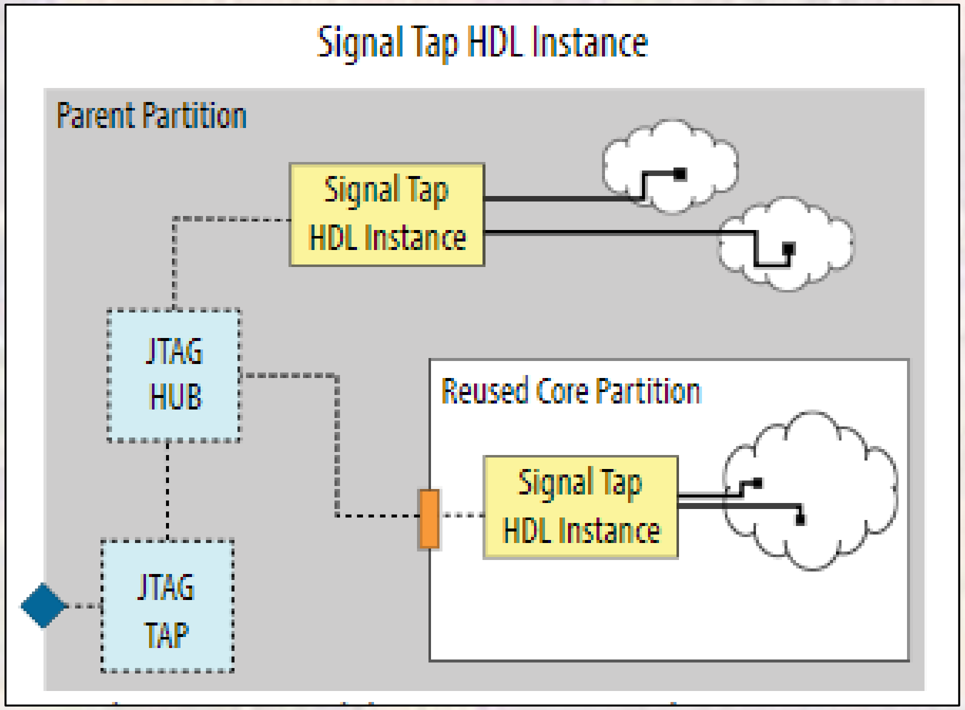
SignalTap

- SignalTap II
  - This modifies our baseline design
    - Potentially impacts timing
    - Potentially impacts implementation
  - Not an issue for our simple designs



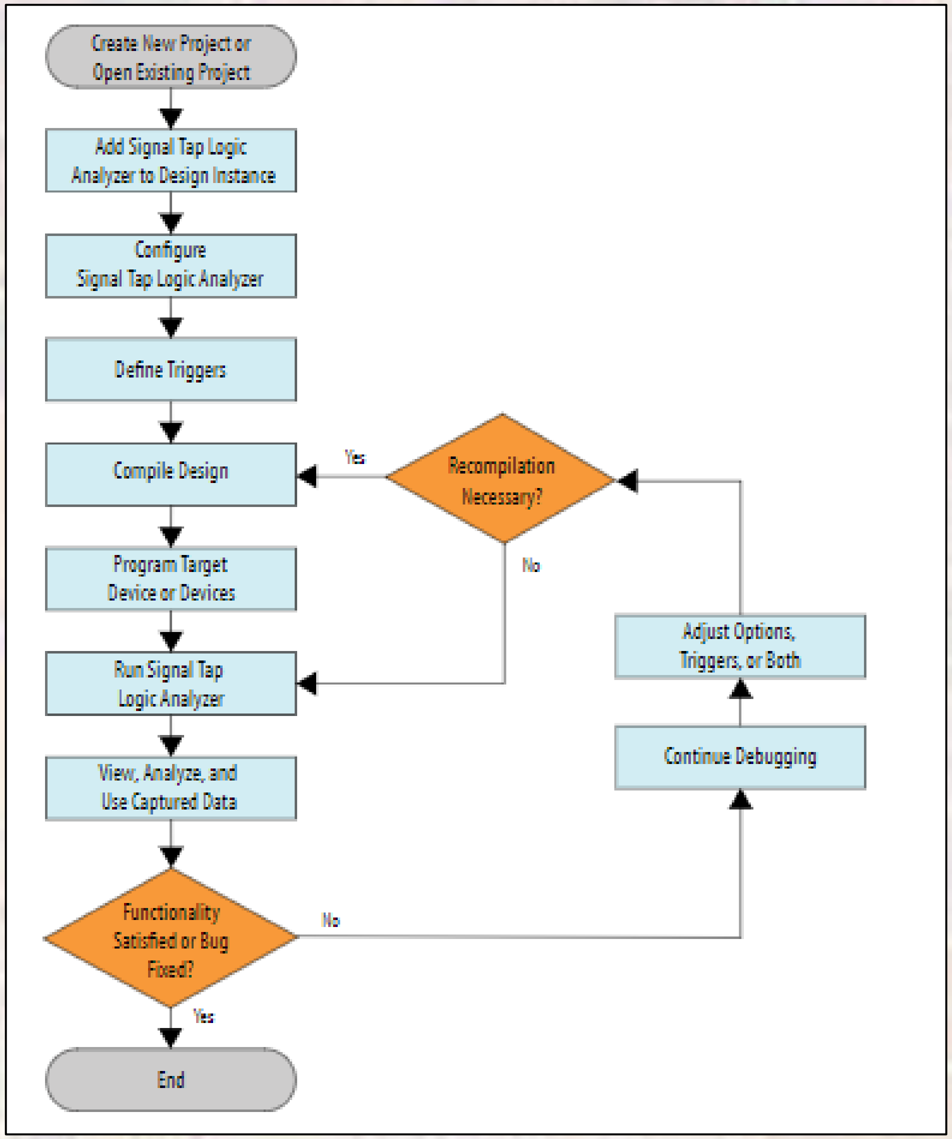
SignalTap

- SignalTap II
  - Uses on-device memory to store samples
    - Allows high speed data storage
    - Uses up some available memory



SignalTap

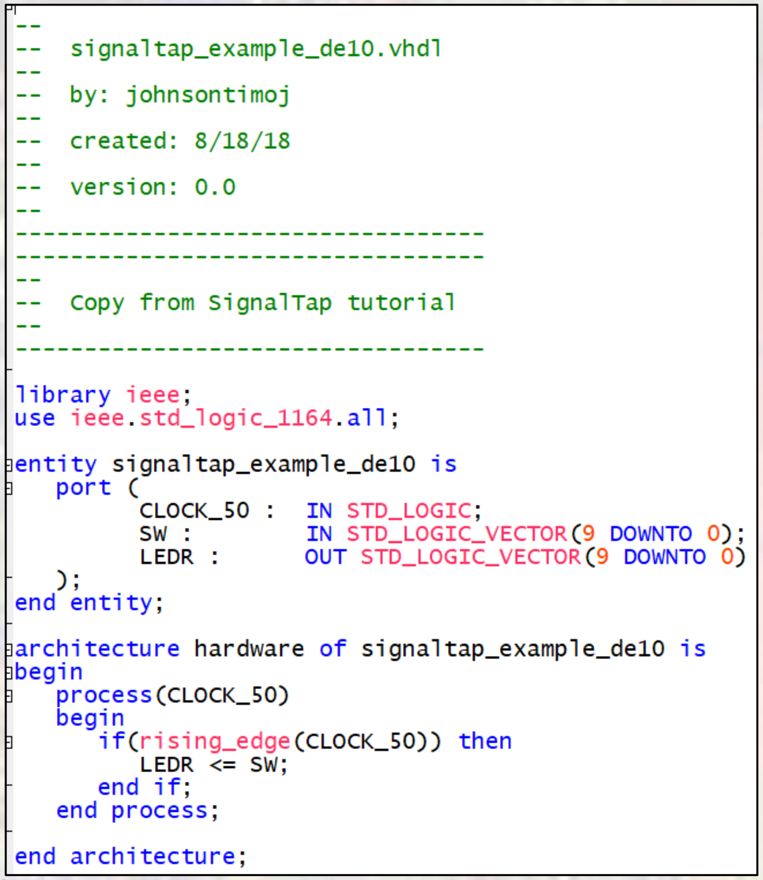
- SignalTap II
  - Incremental Flow


Create New Project or Open Existing Project
Add Signal Tap Logic Analyzer to Design Instance
Configure Signal Tap Logic Analyzer
Define Triggers
Compile Design
Program Target Device or Devices
Run Signal Tap Logic Analyzer
View, Analyze, and Use Captured Data
Functionality Satisfied or Bug Fixed?
Yes
End
No
Continue Debugging
Adjust Options, Triggers, or Both
Recompilation Necessary?
Yes
No

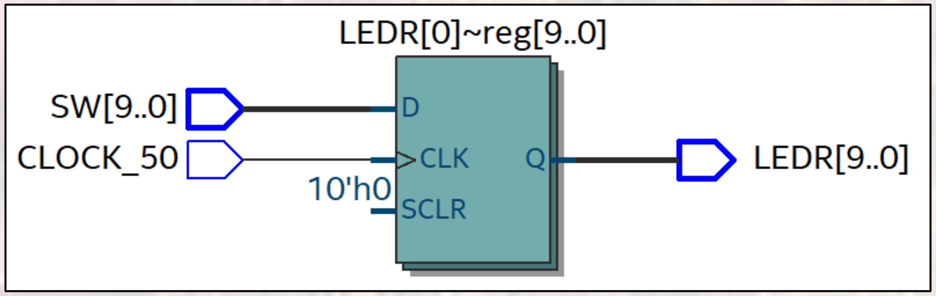
SignalTap

- The SignalTap II
  - Simple Example – Switches tied to LEDs

Monitor the internal switch signals

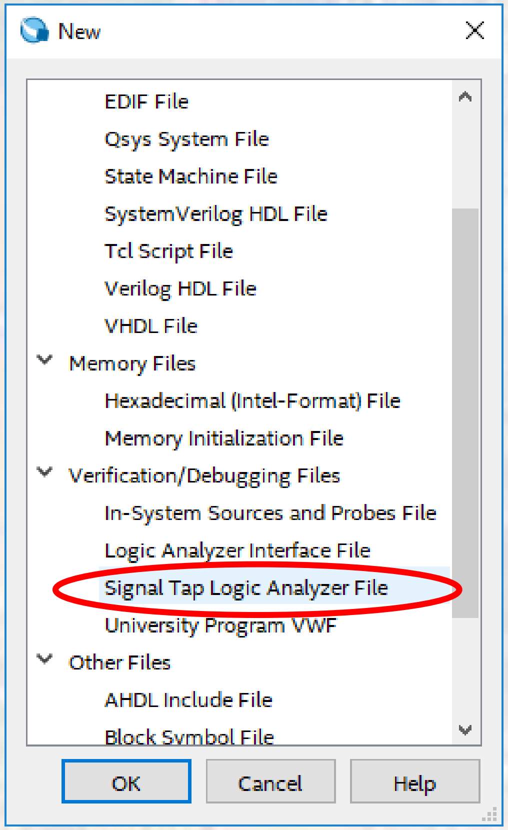


```
--
--  signaltap_example_de10.vhdl
--
--  by: johnsontimoj
--
--  created: 8/18/18
--
--  version: 0.0
--
----------------------------------
----------------------------------
--
--  Copy from SignalTap tutorial
--
----------------------------------

library ieee;
use ieee.std_logic_1164.all;

entity signaltap_example_de10 is
    port (
            CLOCK_50 :  IN STD_LOGIC;
            SW :        IN STD_LOGIC_VECTOR(9 DOWNTO 0);
            LEDR :      OUT STD_LOGIC_VECTOR(9 DOWNTO 0)
    );
end entity;

architecture hardware of signaltap_example_de10 is
begin
    process(CLOCK_50)
    begin
        if(rising_edge(CLOCK_50)) then
            LEDR <= SW;
        end if;
    end process;

end architecture;
```



SignalTap

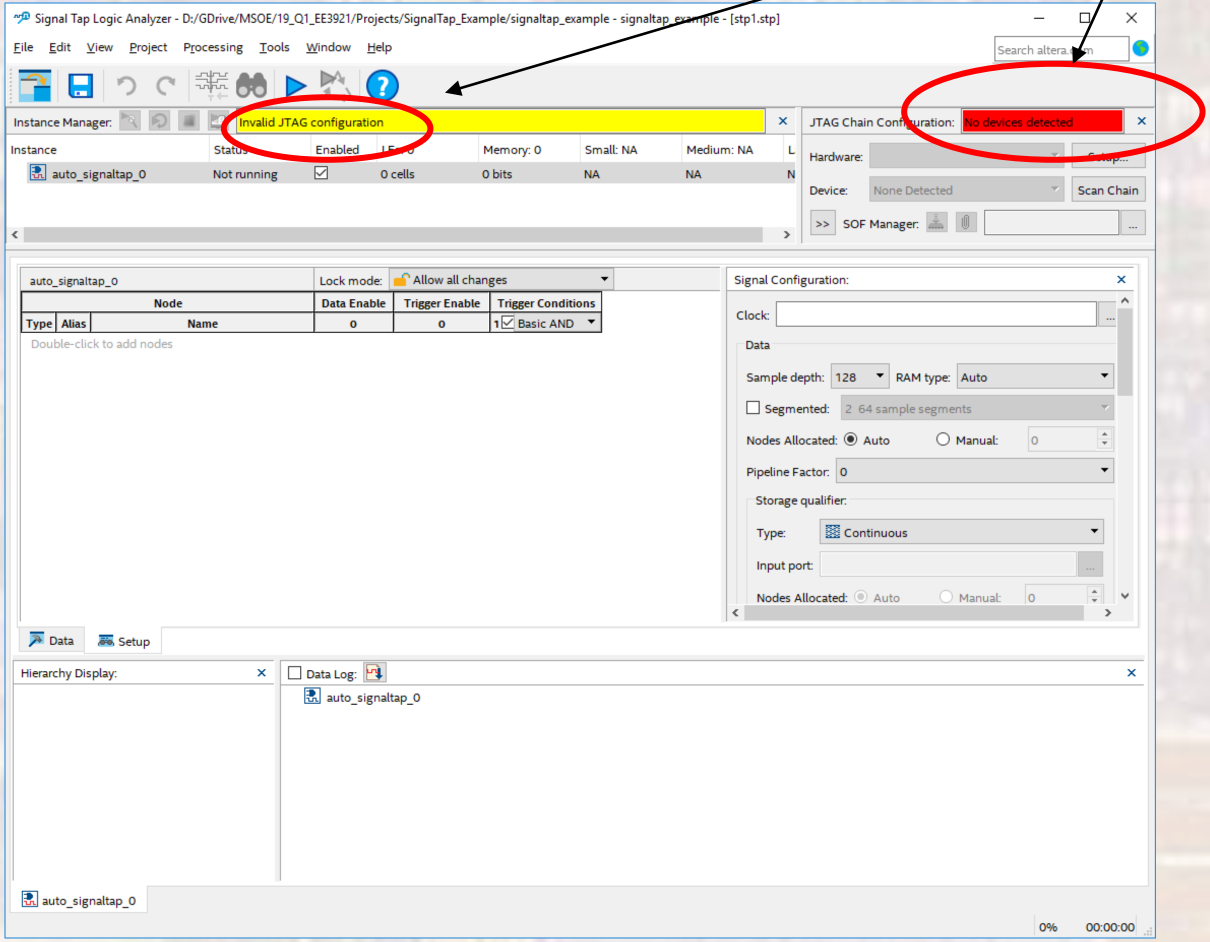
- The SignalTap II
  - Open a SignalTap Logic Analyzer file
  - File → New → SignalTap Logic Analyzer file



SignalTap

- The SignalTap II
  - Open a SignalTap Logic Analyzer file

ignore these

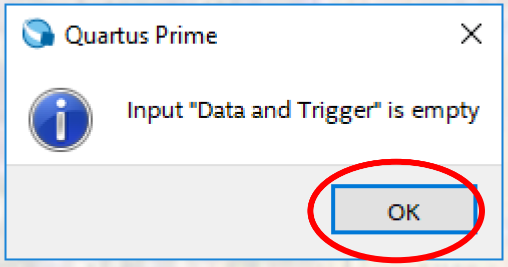

Signal Tap Logic Analyzer - D:/GDrive/MSOE/19_Q1_EE3921/Projects/SignalTap_Example/signaltap_example - signaltap_example - [stp1.stp]
File Edit View Project Processing Tools Window Help
Instance Manager:
Invalid JTAG configuration
JTAG Chain Configuration: No devices detected
Hardware:
Device: None Detected
Scan Chain
SOF Manager:
Signal Configuration:
Clock:
Data
Sample depth: 128 RAM type: Auto
Segmented: 2 64 sample segments
Nodes Allocated: Auto Manual: 0
Pipeline Factor: 0
Storage qualifier:
Type: Continuous
Input port:
Lock mode: Allow all changes
Double-click to add nodes
Data
Setup
Hierarchy Display:
Data Log:
auto_signaltap_0
0% 00:00:00

Instance	Status	Enabled	LEs: 0	Memory: 0	Small: NA	Medium: NA	L
auto_signaltap_0	Not running	✓	0 cells	0 bits	NA	NA	N

Node			Data Enable	Trigger Enable	Trigger Conditions
Type	Alias	Name	0	0	1 ✓ Basic AND

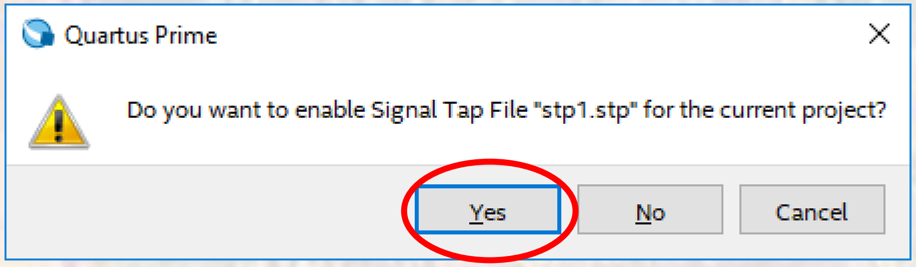
SignalTap

- The SignalTap II
  - Save the file
  - Click OK when it complains “Input Data and Trigger is empty”
  - Click yes to enable the file



Quartus Prime

Input "Data and Trigger" is empty

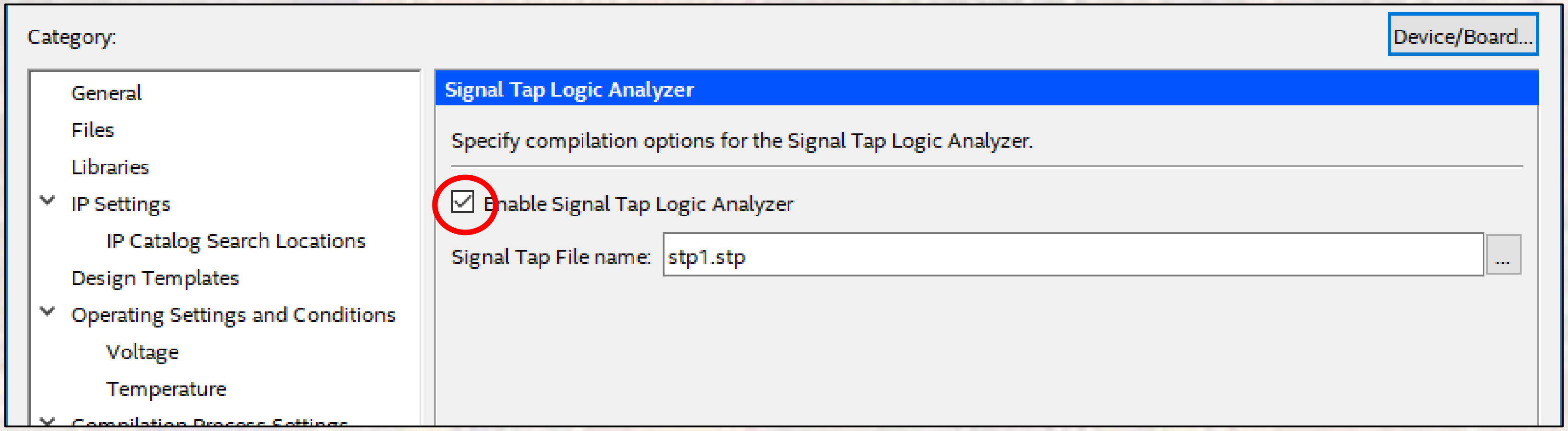


Quartus Prime

Do you want to enable Signal Tap File "stp1.stp" for the current project?

SignalTap

- Under Assignments → Settings → SignalTap Logic …
  - Check/uncheck enable to enable/disable SignalTap
  - You can change the current SignalTap file



Signal Tap Logic Analyzer

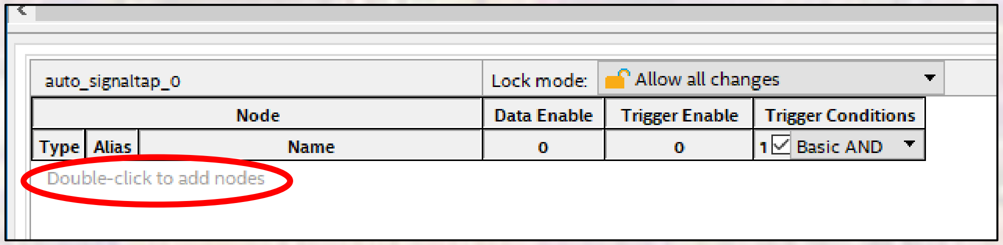
Specify compilation options for the Signal Tap Logic Analyzer.

☑ Enable Signal Tap Logic Analyzer

Signal Tap File name: stp1.stp

SignalTap

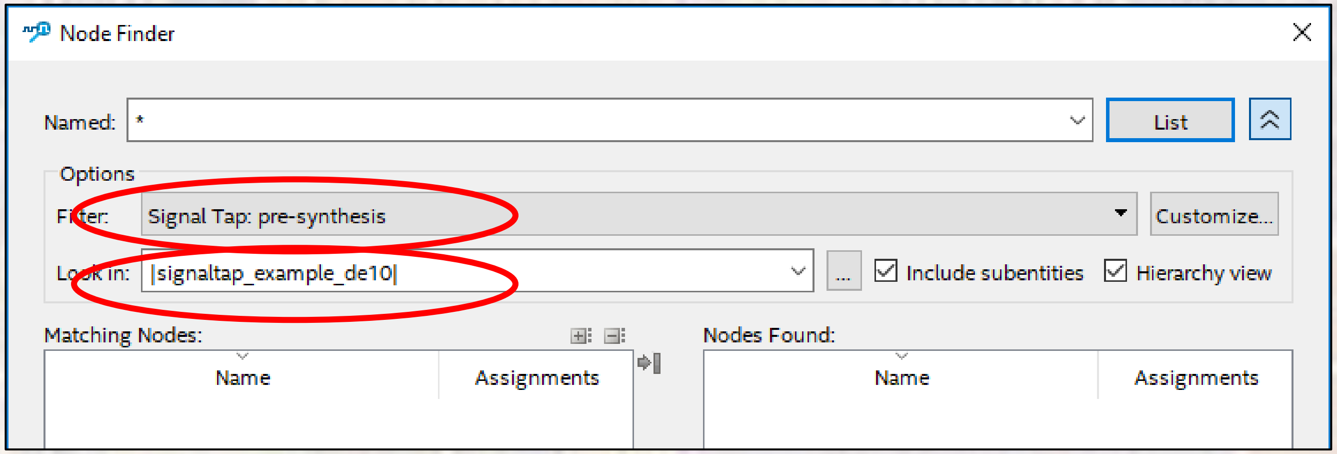
- Select nodes to monitor
  - Double click in the node window



auto_signaltap_0 | Lock mode: Allow all changes

Node			Data Enable	Trigger Enable	Trigger Conditions
Type	Alias	Name	0	0	1 ☑ Basic AND
Double-click to add nodes					

  - Expand the top section – arrows or right
  - Select pre-synthesis under filter
  - Make sure your design is listed under Look in



Node Finder

Named: *

Options

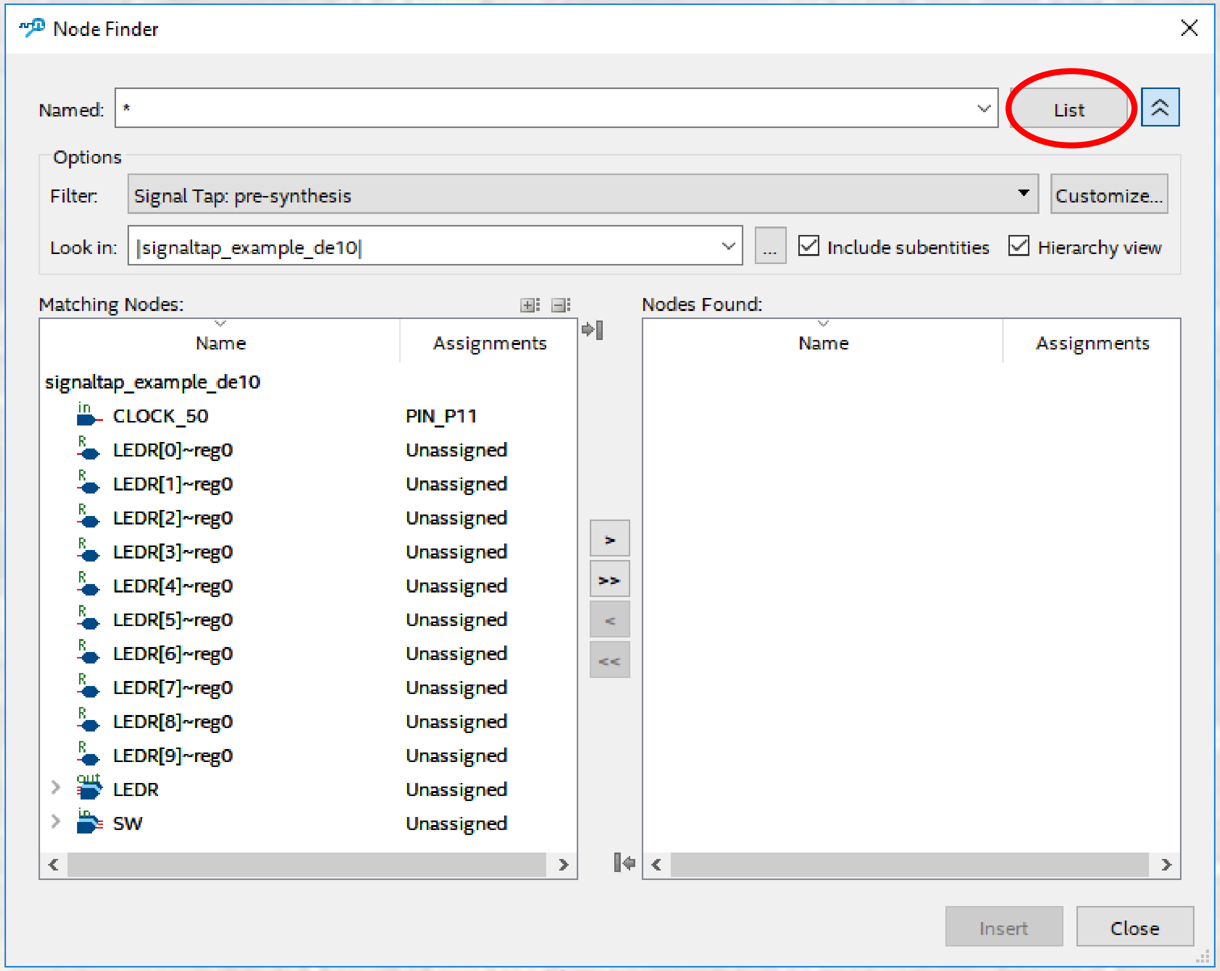
Filter: Signal Tap: pre-synthesis

Look in: |signaltap_example_de10|

☑ Include subentities ☑ Hierarchy view

SignalTap

- Click List
  - All the nodes in your design will be listed



Named: *

Options

Filter: Signal Tap: pre-synthesis

Look in: |signaltap_example_de10|

☑ Include subentities ☑ Hierarchy view

Matching Nodes:

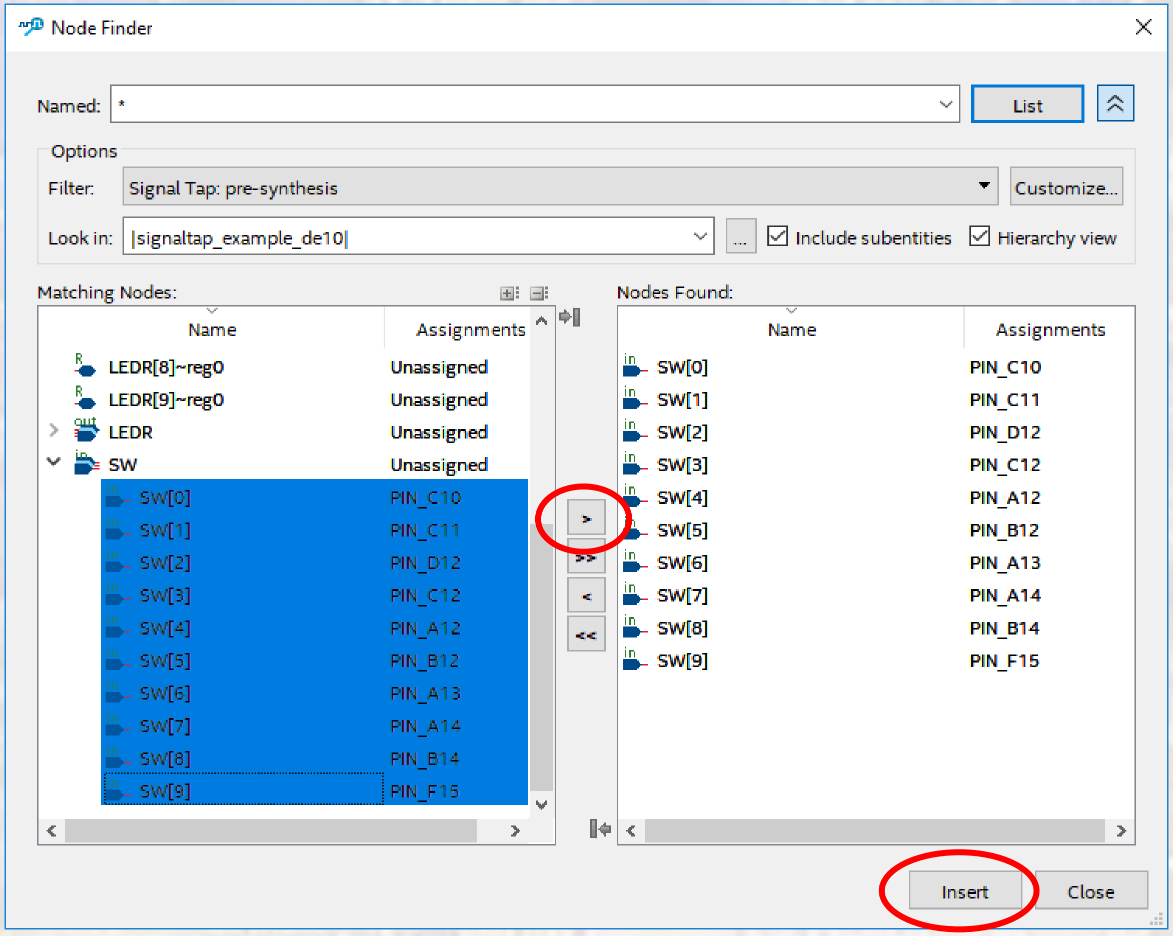
Name	Assignments
signaltap_example_de10	
CLOCK_50	PIN_P11
LEDR[0]~reg0	Unassigned
LEDR[1]~reg0	Unassigned
LEDR[2]~reg0	Unassigned
LEDR[3]~reg0	Unassigned
LEDR[4]~reg0	Unassigned
LEDR[5]~reg0	Unassigned
LEDR[6]~reg0	Unassigned
LEDR[7]~reg0	Unassigned
LEDR[8]~reg0	Unassigned
LEDR[9]~reg0	Unassigned
LEDR	Unassigned
SW	Unassigned

Nodes Found:

Name	Assignments

SignalTap

- Expand the SW node and copy them to the right window and then insert


Node Finder

Named: *

Options

Filter: Signal Tap: pre-synthesis

Look in: |signaltap_example_de10|

☑ Include subentities ☑ Hierarchy view

Matching Nodes:

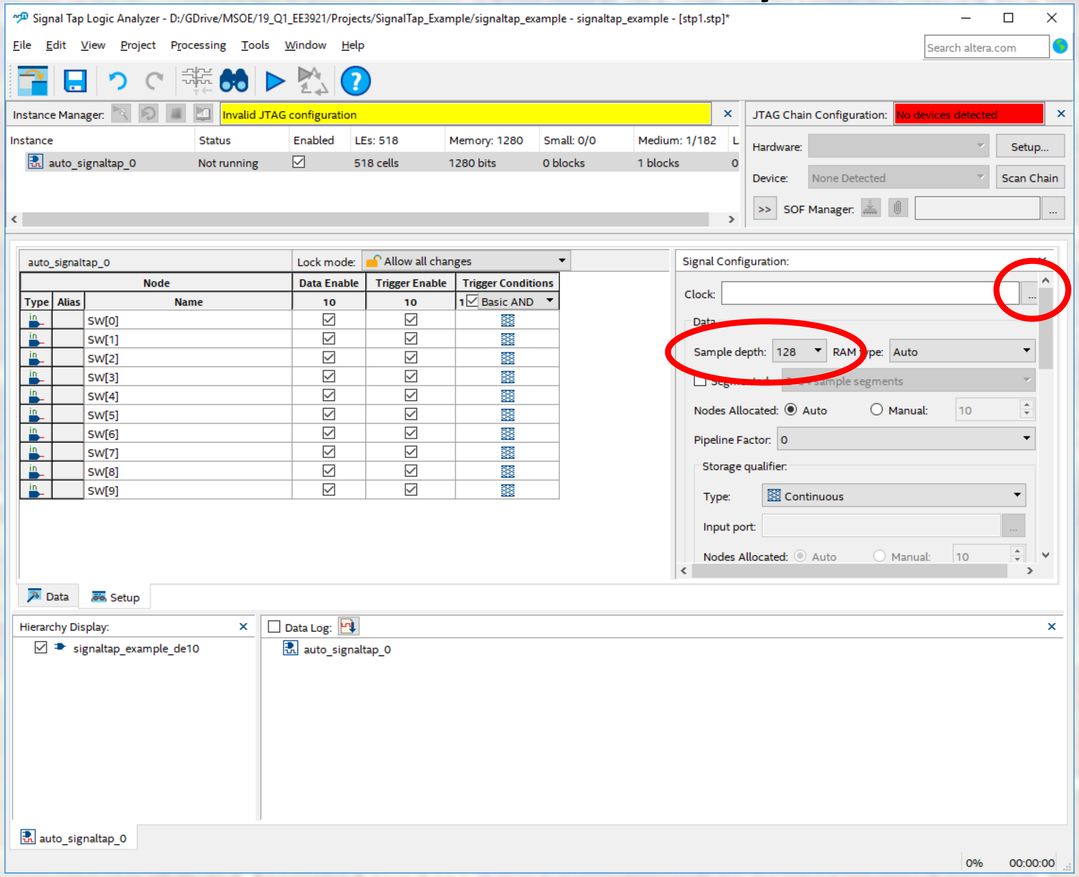
Name	Assignments
LEDR[8]~reg0	Unassigned
LEDR[9]~reg0	Unassigned
LEDR	Unassigned
SW	Unassigned
SW[0]	PIN_C10
SW[1]	PIN_C11
SW[2]	PIN_D12
SW[3]	PIN_C12
SW[4]	PIN_A12
SW[5]	PIN_B12
SW[6]	PIN_A13
SW[7]	PIN_A14
SW[8]	PIN_B14
SW[9]	PIN_F15

Nodes Found:

Name	Assignments
SW[0]	PIN_C10
SW[1]	PIN_C11
SW[2]	PIN_D12
SW[3]	PIN_C12
SW[4]	PIN_A12
SW[5]	PIN_B12
SW[6]	PIN_A13
SW[7]	PIN_A14
SW[8]	PIN_B14
SW[9]	PIN_F15

SignalTap

- Note the sample depth – this is how many data points to keep
- Select "…" beside the clock entry box



Signal Tap Logic Analyzer - D:/GDrive/MSOE/19_Q1_EE3921/Projects/SignalTap_Example/signaltap_example - signaltap_example - [stp1.stp]*

Instance Manager: Invalid JTAG configuration

Instance	Status	Enabled	LEs: 518	Memory: 1280	Small: 0/0	Medium: 1/182	L
auto_signaltap_0	Not running	✓	518 cells	1280 bits	0 blocks	1 blocks	0

JTAG Chain Configuration: No devices detected

Hardware:
Device: None Detected
SOF Manager:

auto_signaltap_0 Lock mode: Allow all changes

Node			Data Enable	Trigger Enable	Trigger Conditions
Type	Alias	Name	10	10	1 ✓ Basic AND
in		SW[0]	✓	✓	▦
in		SW[1]	✓	✓	▦
in		SW[2]	✓	✓	▦
in		SW[3]	✓	✓	▦
in		SW[4]	✓	✓	▦
in		SW[5]	✓	✓	▦
in		SW[6]	✓	✓	▦
in		SW[7]	✓	✓	▦
in		SW[8]	✓	✓	▦
in		SW[9]	✓	✓	▦

Signal Configuration:

Clock:

Data

Sample depth: 128 RAM type: Auto

Segmented: sample segments

Nodes Allocated: [● Auto] Manual: 10

Pipeline Factor: 0

Storage qualifier:

Type: Continuous

Input port:

Nodes Allocated: Auto Manual: 10

Hierarchy Display:
✓ signaltap_example_de10

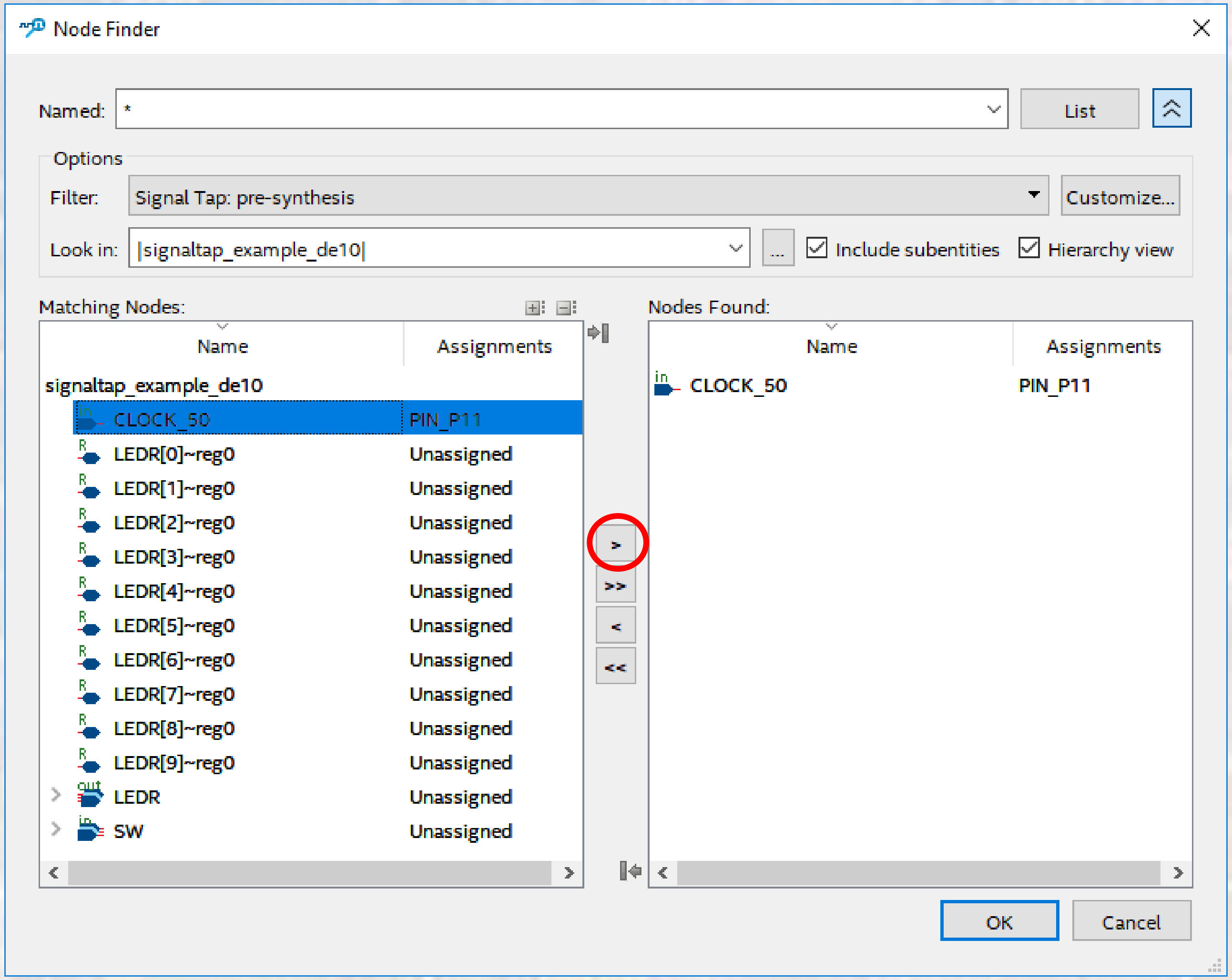
Data Log:
auto_signaltap_0

auto_signaltap_0

0% 00:00:00

SignalTap

- Copy the CLOCK_50 signal over to the right window



Node Finder

Named: *

Options

Filter: Signal Tap: pre-synthesis

Look in: |signaltap_example_de10|

☑ Include subentities ☑ Hierarchy view

Matching Nodes:

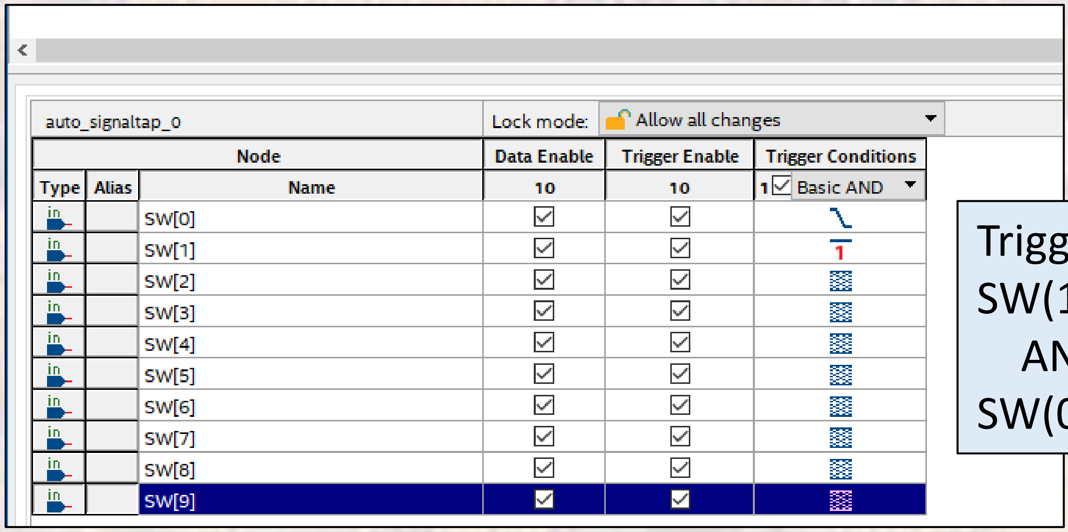
Name	Assignments
signaltap_example_de10	
CLOCK_50	PIN_P11
LEDR[0]~reg0	Unassigned
LEDR[1]~reg0	Unassigned
LEDR[2]~reg0	Unassigned
LEDR[3]~reg0	Unassigned
LEDR[4]~reg0	Unassigned
LEDR[5]~reg0	Unassigned
LEDR[6]~reg0	Unassigned
LEDR[7]~reg0	Unassigned
LEDR[8]~reg0	Unassigned
LEDR[9]~reg0	Unassigned
LEDR	Unassigned
SW	Unassigned

Nodes Found:

Name	Assignments
CLOCK_50	PIN_P11

SignalTap

- Setup the data capture trigger(s)
  - There are a number of simple and complex triggering mechanisms available
  - Select Basic AND in the pull down
  - Right click on the right column of sw0 and select falling edge
  - Right click on the right column of sw1 and select high (1)



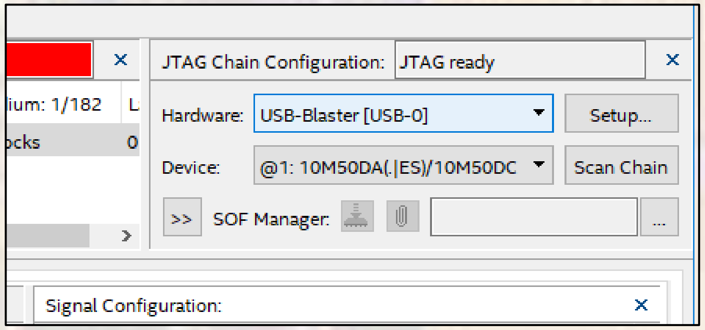
auto_signaltap_0 — Lock mode: Allow all changes

Type	Alias	Name	Data Enable 10	Trigger Enable 10	Trigger Conditions 1 ✓ Basic AND
in		SW[0]	✓	✓	⤵
in		SW[1]	✓	✓	1
in		SW[2]	✓	✓	▨
in		SW[3]	✓	✓	▨
in		SW[4]	✓	✓	▨
in		SW[5]	✓	✓	▨
in		SW[6]	✓	✓	▨
in		SW[7]	✓	✓	▨
in		SW[8]	✓	✓	▨
in		SW[9]	✓	✓	▨

Trigger on
SW(1) high
AND
SW(0) ↓

SignalTap

- Connect the DE10 Board
  - Select Setup in the upper right hand corner of the SignalTap window
  - Select the USB-Blaster
  - Save



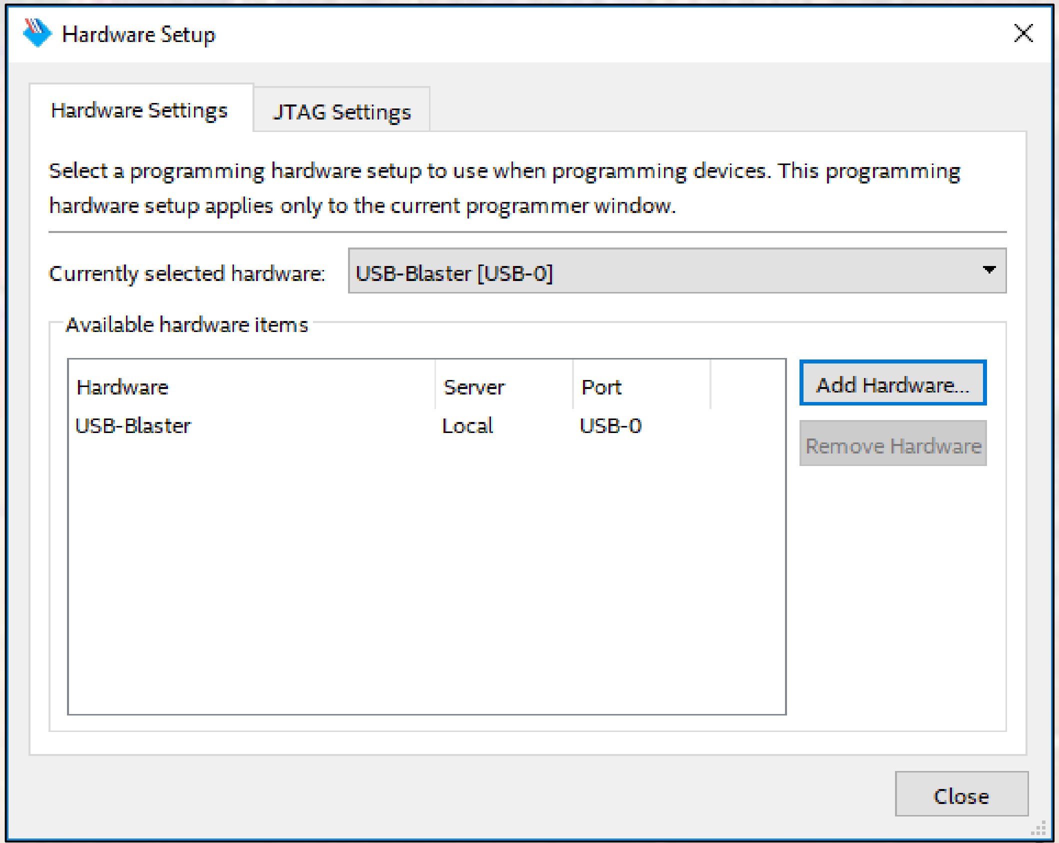
JTAG Chain Configuration: JTAG ready

Hardware: USB-Blaster [USB-0]

Device: @1: 10M50DA(.|ES)/10M50DC

SOF Manager:

Signal Configuration:



Hardware Setup

Select a programming hardware setup to use when programming devices. This programming hardware setup applies only to the current programmer window.

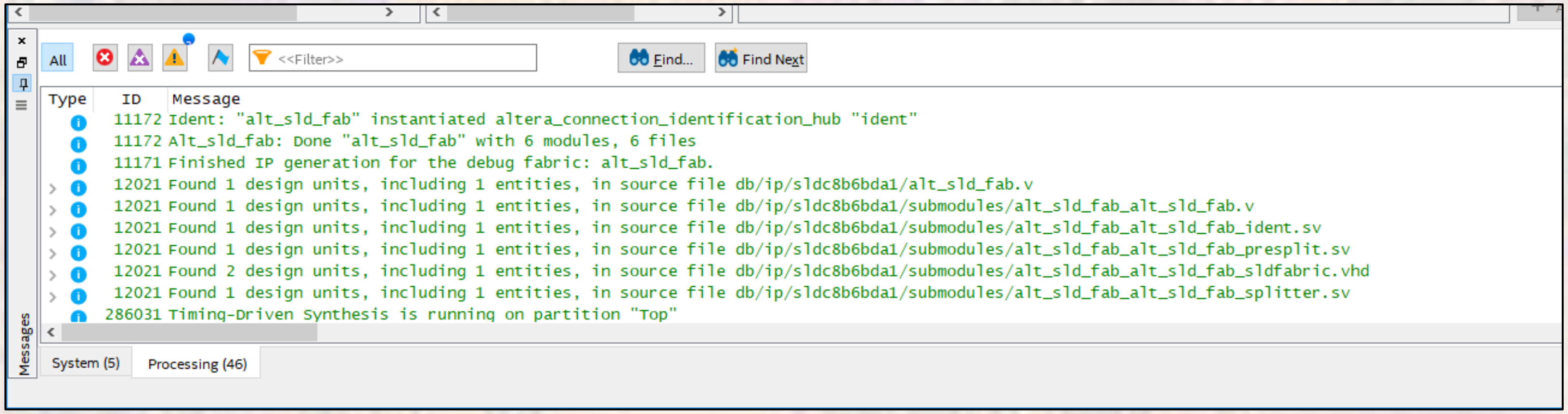
Currently selected hardware: USB-Blaster [USB-0]

Available hardware items

Hardware	Server	Port
USB-Blaster	Local	USB-0

SignalTap

- Recompile
  - In the main Quartus window – compile your design
  - You will see the SignalTap modules along with your own design

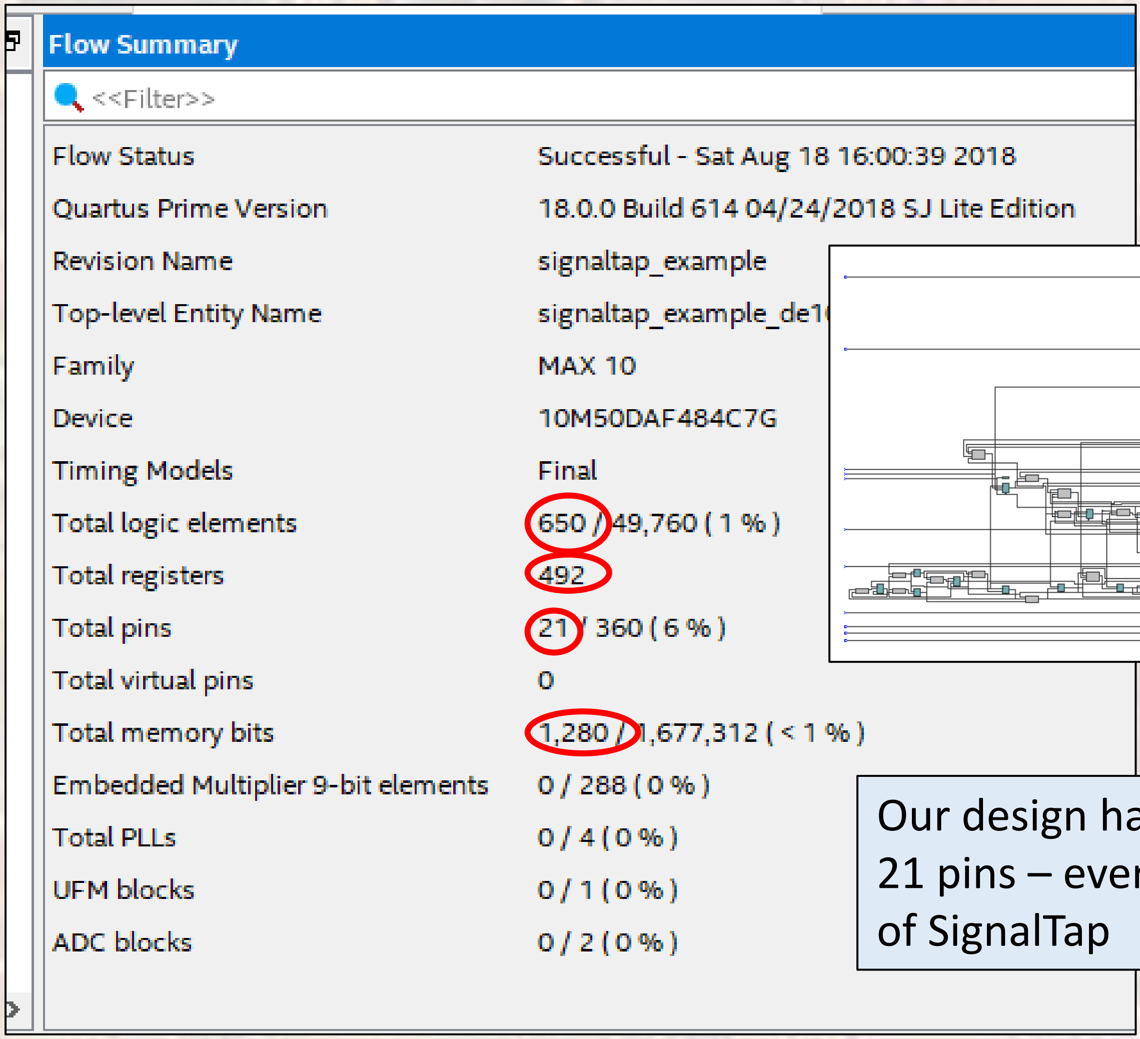


```
Type   ID    Message
     11172 Ident: "alt_sld_fab" instantiated altera_connection_identification_hub "ident"
     11172 Alt_sld_fab: Done "alt_sld_fab" with 6 modules, 6 files
     11171 Finished IP generation for the debug fabric: alt_sld_fab.
     12021 Found 1 design units, including 1 entities, in source file db/ip/sldc8b6bda1/alt_sld_fab.v
     12021 Found 1 design units, including 1 entities, in source file db/ip/sldc8b6bda1/submodules/alt_sld_fab_alt_sld_fab.v
     12021 Found 1 design units, including 1 entities, in source file db/ip/sldc8b6bda1/submodules/alt_sld_fab_alt_sld_fab_ident.sv
     12021 Found 1 design units, including 1 entities, in source file db/ip/sldc8b6bda1/submodules/alt_sld_fab_alt_sld_fab_presplit.sv
     12021 Found 2 design units, including 1 entities, in source file db/ip/sldc8b6bda1/submodules/alt_sld_fab_alt_sld_fab_sldfabric.vhd
     12021 Found 1 design units, including 1 entities, in source file db/ip/sldc8b6bda1/submodules/alt_sld_fab_alt_sld_fab_splitter.sv
    286031 Timing-Driven Synthesis is running on partition "Top"
```

  - Program the board

SignalTap

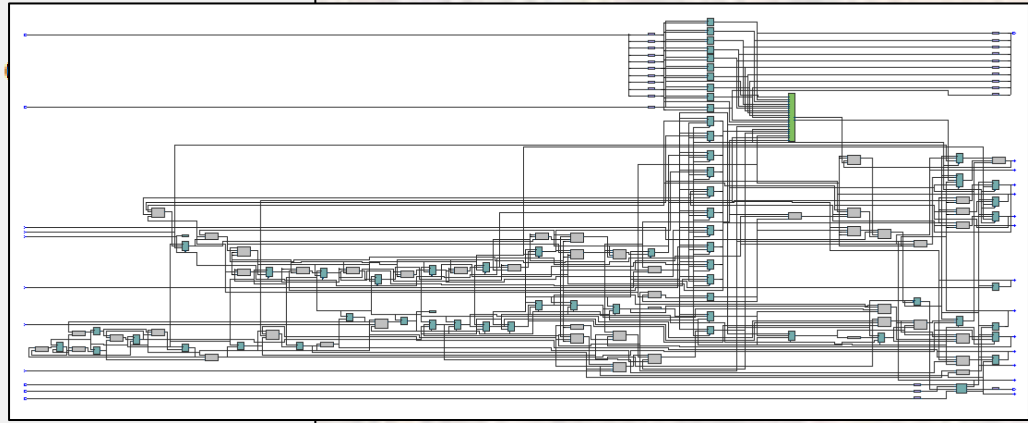
- Review resources



Flow Summary

<<Filter>>

Flow Status	Successful - Sat Aug 18 16:00:39 2018
Quartus Prime Version	18.0.0 Build 614 04/24/2018 SJ Lite Edition
Revision Name	signaltap_example
Top-level Entity Name	signaltap_example_de1
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	650 / 49,760 (1 %)
Total registers	492
Total pins	21 / 360 (6 %)
Total virtual pins	0
Total memory bits	1,280 / 1,677,312 (< 1 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)



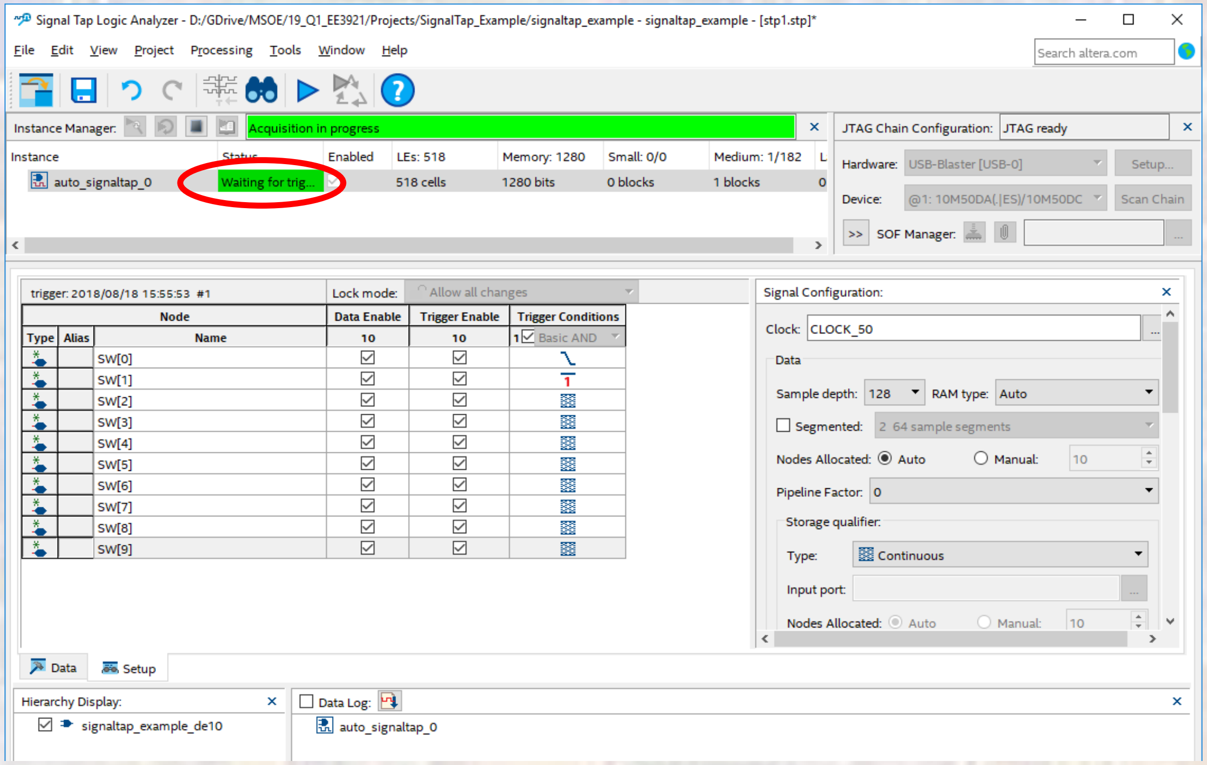
Our design has 10 registers and 21 pins – everything else is part of SignalTap

SignalTap

- Verify your design
  - Each switch is coupled to an LED via a register clocked at 50MHZ
  - Toggle the switches and see the LEDs turn on and off
    - It appears instantaneous due to the clock speed

SignalTap

- Start the analysis
  - Reset the switches to 0's
  - In the SignalTap window select Processing → Run Analysis



Signal Tap Logic Analyzer - D:/GDrive/MSOE/19_Q1_EE3921/Projects/SignalTap_Example/signaltap_example - signaltap_example - [stp1.stp]*

Instance Manager: Acquisition in progress

JTAG Chain Configuration: JTAG ready

Hardware: USB-Blaster [USB-0]

Device: @1: 10M50DA(.|ES)/10M50DC

Instance	Status	Enabled	LEs: 518	Memory: 1280	Small: 0/0	Medium: 1/182
auto_signaltap_0	Waiting for trig...		518 cells	1280 bits	0 blocks	1 blocks

trigger: 2018/08/18 15:55:53 #1

Lock mode: Allow all changes

Type	Alias	Name	Data Enable 10	Trigger Enable 10	Trigger Conditions 1 Basic AND
		SW[0]	✓	✓	↓
		SW[1]	✓	✓	↑
		SW[2]	✓	✓	▨
		SW[3]	✓	✓	▨
		SW[4]	✓	✓	▨
		SW[5]	✓	✓	▨
		SW[6]	✓	✓	▨
		SW[7]	✓	✓	▨
		SW[8]	✓	✓	▨
		SW[9]	✓	✓	▨

Signal Configuration:

Clock: CLOCK_50

Data

Sample depth: 128 RAM type: Auto

Segmented: 2 64 sample segments

Nodes Allocated: Auto Manual: 10

Pipeline Factor: 0

Storage qualifier:

Type: Continuous

Input port:

Nodes Allocated: Auto Manual: 10

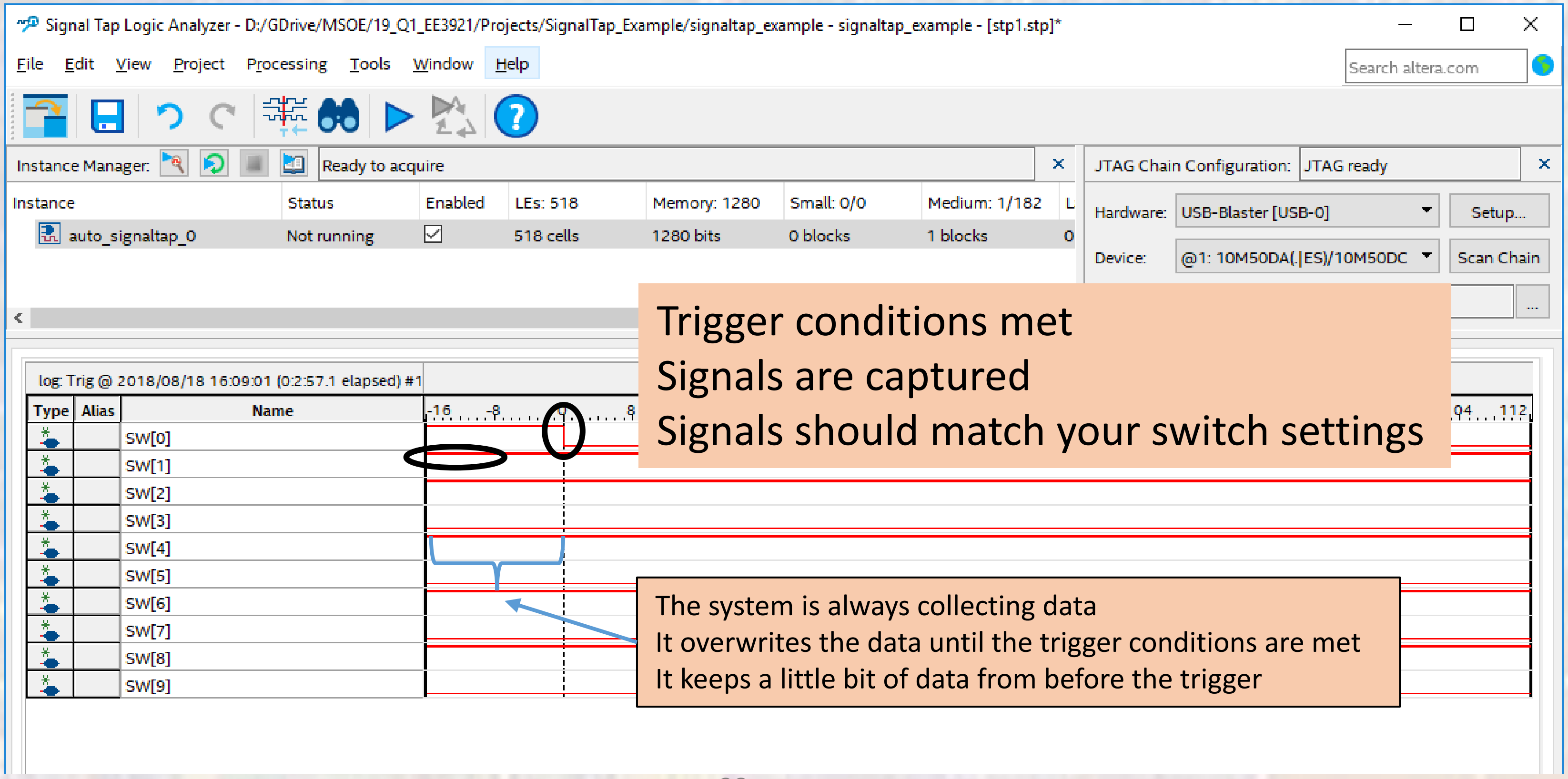
Hierarchy Display: signaltap_example_de10

Data Log: auto_signaltap_0

No trigger condition met yet

SignalTap

- Start the analysis
  - Toggle some switches – nothing should happen in SignalTap
  - Set SW(1) to ‘1’ and toggle SW(0) from ‘1’ to ‘0’


Signal Tap Logic Analyzer - D:/GDrive/MSOE/19_Q1_EE3921/Projects/SignalTap_Example/signaltap_example - signaltap_example - [stp1.stp]*

Instance Manager: Ready to acquire

JTAG Chain Configuration: JTAG ready

Hardware: USB-Blaster [USB-0]

Device: @1: 10M50DA(.|ES)/10M50DC

Instance	Status	Enabled	LEs: 518	Memory: 1280	Small: 0/0	Medium: 1/182
auto_signaltap_0	Not running	☑	518 cells	1280 bits	0 blocks	1 blocks

log: Trig @ 2018/08/18 16:09:01 (0:2:57.1 elapsed) #1

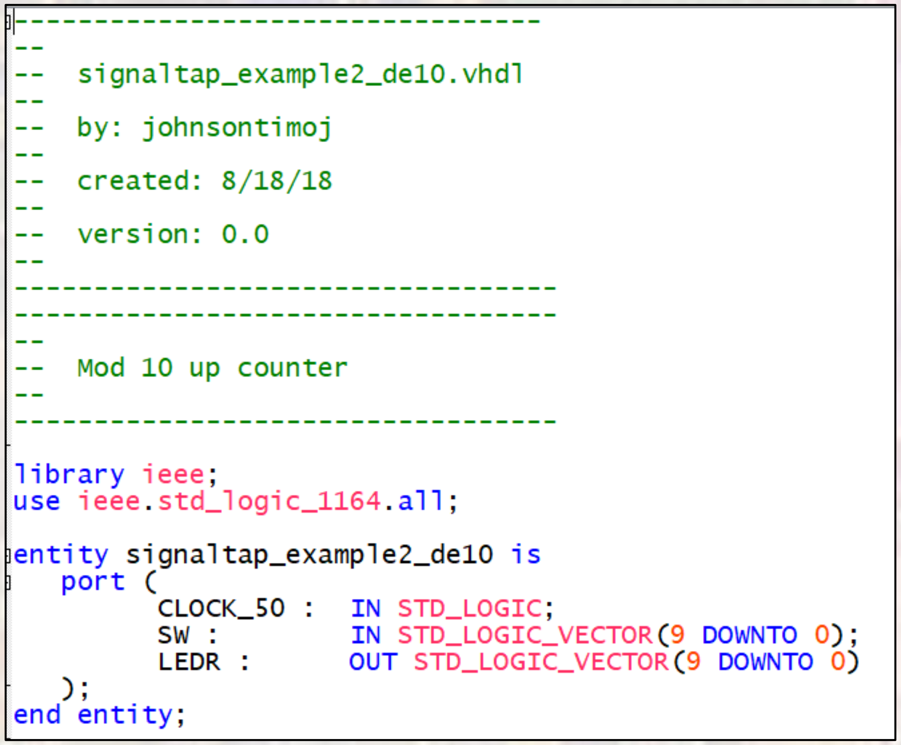
Type	Alias	Name
		SW[0]
		SW[1]
		SW[2]
		SW[3]
		SW[4]
		SW[5]
		SW[6]
		SW[7]
		SW[8]
		SW[9]

Trigger conditions met
Signals are captured
Signals should match your switch settings

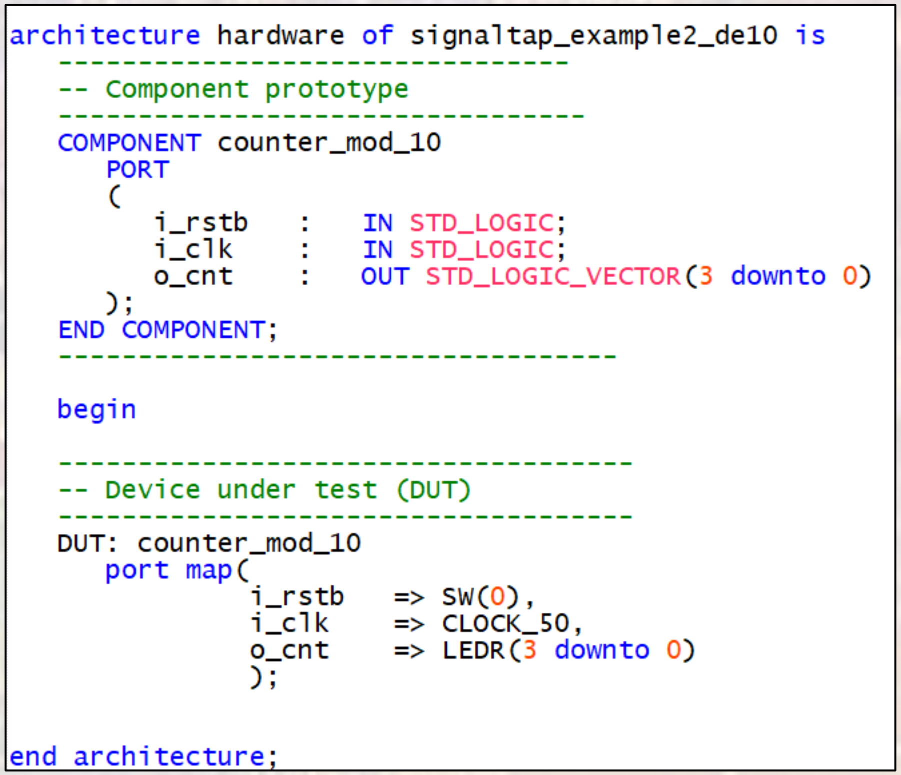
The system is always collecting data
It overwrites the data until the trigger conditions are met
It keeps a little bit of data from before the trigger

SignalTap

- Example 2
  - Mod10 Counter with LED outputs
  - Running at full speed – impossible to see on LEDs



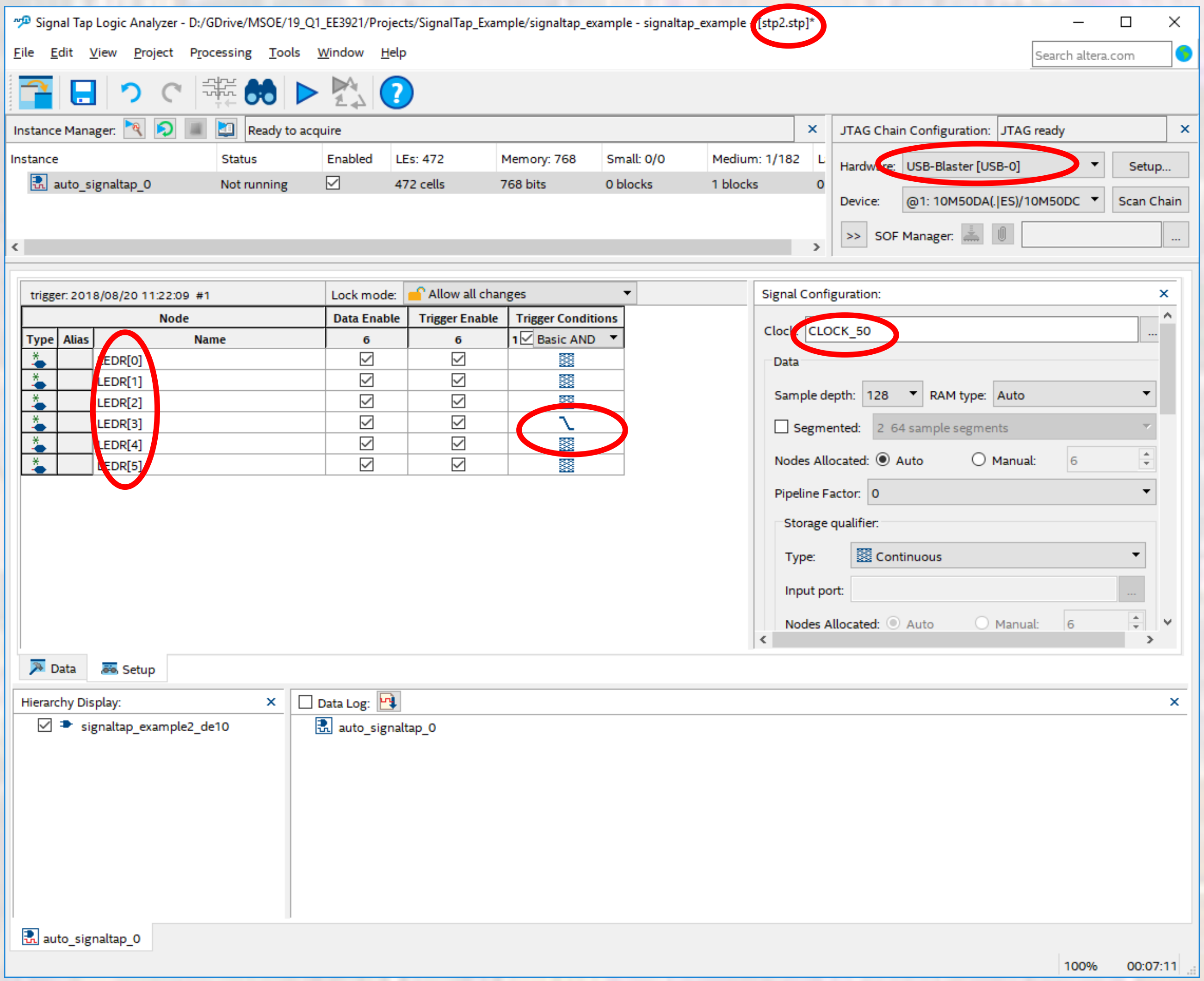
```
----------------------------------
--
--   signaltap_example2_de10.vhdl
--
--   by: johnsontimoj
--
--   created: 8/18/18
--
--   version: 0.0
--
-----------------------------------
-----------------------------------
--
--   Mod 10 up counter
--
-----------------------------------

library ieee;
use ieee.std_logic_1164.all;

entity signaltap_example2_de10 is
   port (
         CLOCK_50 :  IN STD_LOGIC;
         SW :        IN STD_LOGIC_VECTOR(9 DOWNTO 0);
         LEDR :      OUT STD_LOGIC_VECTOR(9 DOWNTO 0)
   );
end entity;
```



```
architecture hardware of signaltap_example2_de10 is
   --------------------------------
   -- Component prototype
   ---------------------------------
   COMPONENT counter_mod_10
      PORT
      (
         i_rstb    :   IN STD_LOGIC;
         i_clk     :   IN STD_LOGIC;
         o_cnt     :   OUT STD_LOGIC_VECTOR(3 downto 0)
      );
   END COMPONENT;
   -----------------------------------

   begin

   ------------------------------------
   -- Device under test (DUT)
   ------------------------------------
   DUT: counter_mod_10
      port map(
               i_rstb   => SW(0),
               i_clk    => CLOCK_50,
               o_cnt    => LEDR(3 downto 0)
               );

end architecture;
```

SignalTap

- Create a new STP file



Signal Tap Logic Analyzer - D:/GDrive/MSOE/19_Q1_EE3921/Projects/SignalTap_Example/signaltap_example - signaltap_example - [stp2.stp]*

Instance Manager: Ready to acquire

Instance	Status	Enabled	LEs: 472	Memory: 768	Small: 0/0	Medium: 1/182
auto_signaltap_0	Not running	✓	472 cells	768 bits	0 blocks	1 blocks

JTAG Chain Configuration: JTAG ready

Hardware: USB-Blaster [USB-0]

Device: @1: 10M50DA(.|ES)/10M50DC

trigger: 2018/08/20 11:22:09 #1 — Lock mode: Allow all changes

Type	Alias	Name	Data Enable	Trigger Enable	Trigger Conditions
			6	6	1 ✓ Basic AND
		LEDR[0]	✓	✓	▨
		LEDR[1]	✓	✓	▨
		LEDR[2]	✓	✓	▨
		LEDR[3]	✓	✓	╲
		LEDR[4]	✓	✓	▨
		LEDR[5]	✓	✓	▨

Signal Configuration:

Clock: CLOCK_50

Data

Sample depth: 128 RAM type: Auto

Segmented: 2 64 sample segments

Nodes Allocated: Auto Manual: 6

Pipeline Factor: 0

Storage qualifier:

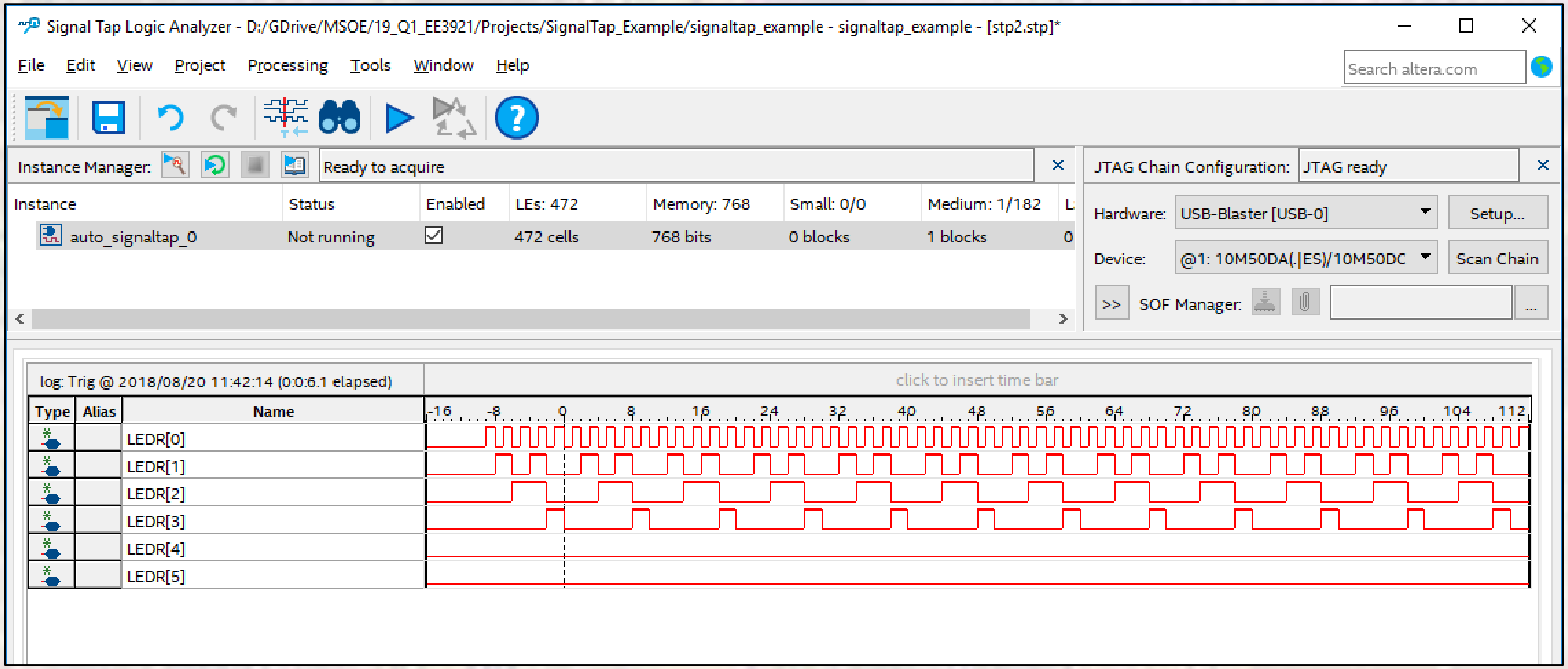
Type: Continuous

Hierarchy Display: signaltap_example2_de10

Data Log: auto_signaltap_0

SignalTap

- Compile, Program and Run Analysis



Signal Tap Logic Analyzer - D:/GDrive/MSOE/19_Q1_EE3921/Projects/SignalTap_Example/signaltap_example - signaltap_example - [stp2.stp]*

Instance Manager: Ready to acquire

Instance	Status	Enabled	LEs: 472	Memory: 768	Small: 0/0	Medium: 1/182
auto_signaltap_0	Not running	✓	472 cells	768 bits	0 blocks	1 blocks

JTAG Chain Configuration: JTAG ready

Hardware: USB-Blaster [USB-0]

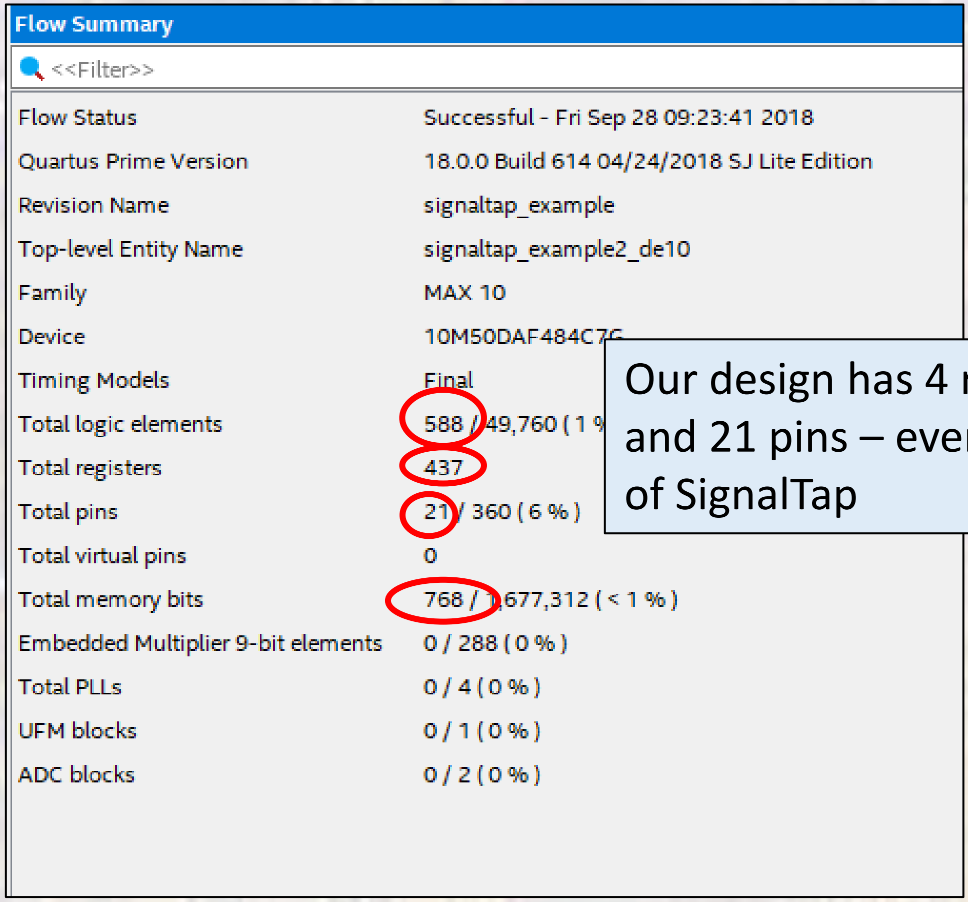
Device: @1: 10M50DA(.|ES)/10M50DC

log: Trig @ 2018/08/20 11:42:14 (0:0:6.1 elapsed)

Type	Alias	Name
		LEDR[0]
		LEDR[1]
		LEDR[2]
		LEDR[3]
		LEDR[4]
		LEDR[5]

SignalTap

- Review resources



Flow Summary

<<Filter>>

Flow Status	Successful - Fri Sep 28 09:23:41 2018
Quartus Prime Version	18.0.0 Build 614 04/24/2018 SJ Lite Edition
Revision Name	signaltap_example
Top-level Entity Name	signaltap_example2_de10
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	588 / 49,760 (1 %
Total registers	437
Total pins	21 / 360 (6 %)
Total virtual pins	0
Total memory bits	768 / 1,677,312 (< 1 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)

Our design has 4 registers, a little logic and 21 pins – everything else is part of SignalTap