

Single Cycle Processor Operation

Last updated 7/18/23

Single Cycle Processor - Operation

- Arithmetic and logical

`fn Reg1, Reg2, Wreg` $Wreg \leftarrow \text{Reg1 } \text{fn } \text{Reg2}$

- Memory

`ld Reg1, Wreg`

$Wreg \leftarrow \text{MEM}(\text{Reg1})$

`st Reg1, Reg2`

$\text{MEM}(\text{Reg1}) \leftarrow \text{Reg2}$

- Immediate

`ldi Wreg, "imm value"` $Wreg \leftarrow \text{"imm value"}$

Single Cycle Processor - Operation

- Arithmetic and logical

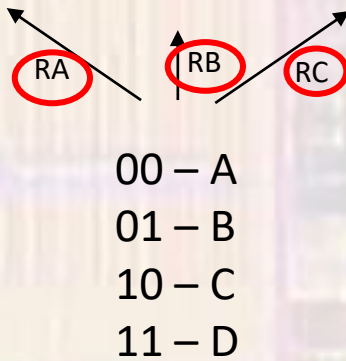
sub RA, RB, RC

$W_{reg} \leftarrow \text{Reg1 fn Reg2}$

$RC \leftarrow RA - RB$

Instruction				Reg 1		Reg 2		W Reg		Immediate Value					
0	1	0	1	0	0	0	1	1	0	0	0	0	0	0	0

or	↑	0000	
and	↑	0001	
nor		0010	
nand		0011	
add		0100	
sub		0101	
slt		0110	
ld		1000	
st		1001	
ldi		1100	



Technically these are don't care but we will always code them as 0s

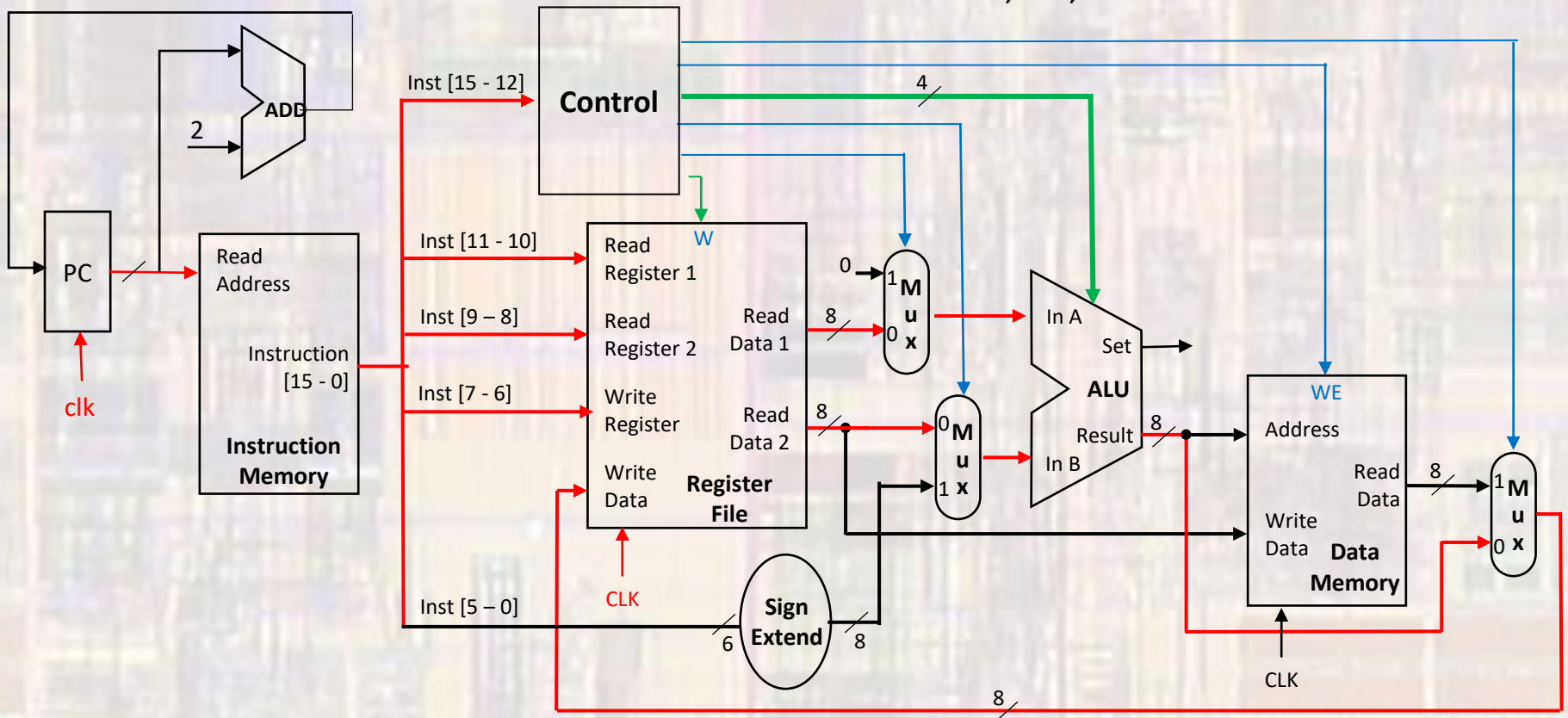
Single Cycle Processor - Operation

- Operation
 - Arithmetic and Logical

Instruction				Reg 1		Reg 2		W Reg		Immediate Value					
0	1	0	1	0	0	0	1	1	0	0	0	0	0	0	0

Wreg ← Reg1 fn Reg2

sub RA, RB, RC RC ← RA - RB



Single Cycle Processor - Operation

- Instruction Format

- Instruction Encoding

- **ld** Reg1, Wreg

Wreg \leftarrow MEM(Reg1)

- **ld** RA, RC

RC \leftarrow MEM(RA)

Instruction				Reg 1		Reg 2		W Reg		Immediate Value						
1	0	0	0	0	0	x	x	1	0	0	0	0	0	0	0	0

or ↑ 0000
 and ↑ 0001
 nor 0010
 nand 0011
 add 0100
 sub 0101
 slt 0110
 ld 1000
 st 1001
 ldi 1100



00 – A
 01 – B
 10 – C
 11 – D

added to Reg 1 to make the memory address

Single Cycle Processor - Operation

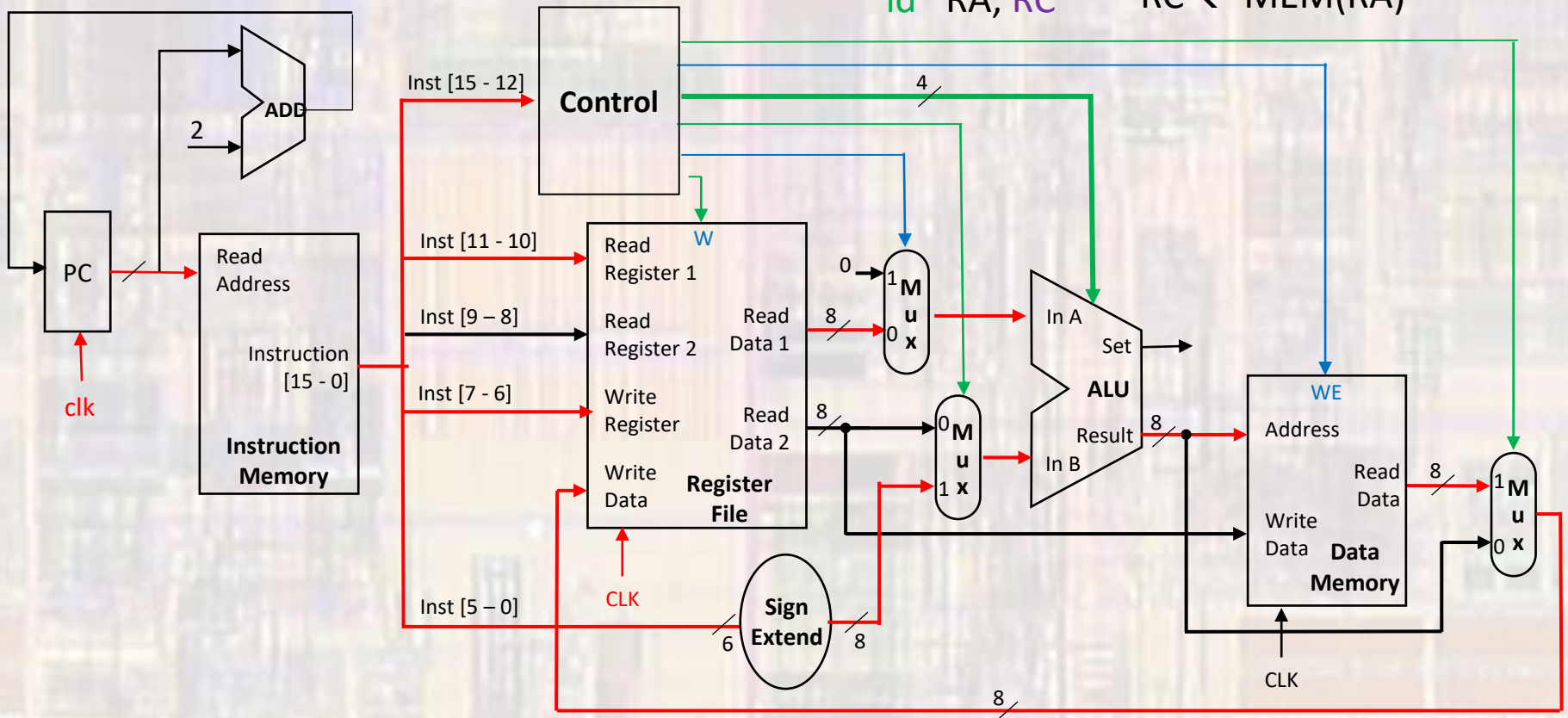
- Operation
 - LD

Instruction				Reg 1		Reg 2		W Reg		Immediate Value					
1	0	0	0	0	0	x	x	1	0	0	0	0	0	0	0

WRreg \leftarrow MEM(Reg1)

RC \leftarrow MEM(RA)

ld RA, RC



Single Cycle Processor - Operation

- Instruction Format

- Instruction Encoding

- `st Reg1, Reg2`

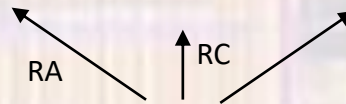
$MEM(Reg1) \leftarrow Reg2$

- `st RA, RC`

$MEM(RA) \leftarrow RC$

Instruction				Reg 1		Reg 2		W Reg		Immediate Value					
1	0	0	1	0	0	1	0	x	x	0	0	0	0	0	0

or ↑ 0000
 and ↑ 0001
 nor 0010
 nand 0011
 add 0100
 sub 0101
 slt 0110
 ld 1000
 st 1001
 ldi 1100



00 – A
 01 – B
 10 – C
 11 – D

↑
 added with Reg 1 to
 make the memory
 address

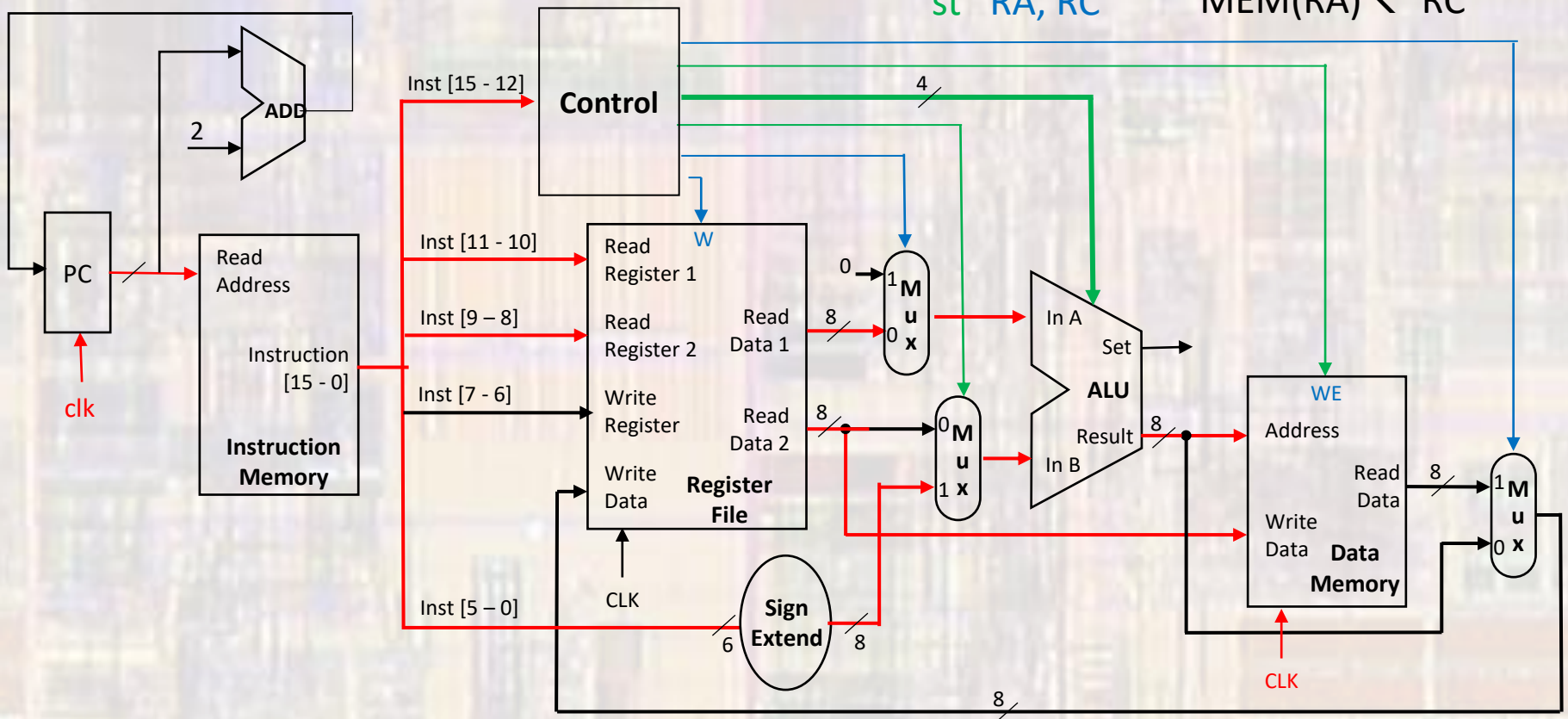
Single Cycle Processor - Operation

- Operation
- ST

Instruction				Reg 1		Reg 2		W Reg		Immediate Value					
1	0	0	1	0	0	1	0	x	x	0	0	0	0	0	0

MEM(Reg1) \leftarrow Reg2

MEM(RA) \leftarrow RC



st RA, RC

Single Cycle Processor - Operation

- Instruction Format

- Instruction Encoding

- **ldi** Wreg, imm

Wreg \leftarrow Imm extended

- **ldi** RA, 0x12

RA \leftarrow 0x12

Instruction				Reg 1		Reg 2		W Reg		Immediate Value					
1	1	0	0	x	x	x	x	0	0	0	1	0	0	1	0

or	0000
and	0001
nor	0010
nand	0011
add	0100
sub	0101
slt	0110
ld	1000
st	1001
ldi	1100



00 – A
 01 – B
 10 – C
 11 – D

signed Hex
 0x20 to 0x1F
 100000 to 011111
 -32 to 31

Single Cycle Processor - Operation

- Operation
- LDI

Instruction				Reg 1		Reg 2		W Reg		Immediate Value					
1	1	0	0	x	x	x	x	0	0	0	1	0	0	1	0

Wreg \leftarrow Imm extended

ldi RA, 0x12 RA \leftarrow 0x12

