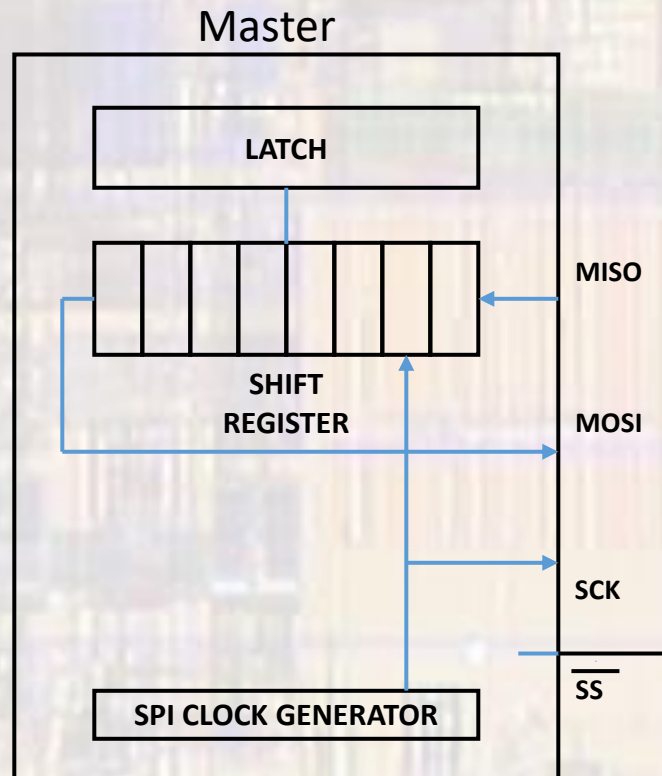# SPI Review

Last updated 7/21/23

# SPI Review

- Overview

  - 8 bit synchronous shift register used to communicate externally

  - Most often used to communicate with peripherals
    - displays, sensors, converters

  - Can be used for inter-processor communication

  - Two modes of operation
    - Master – responsible for providing the clock
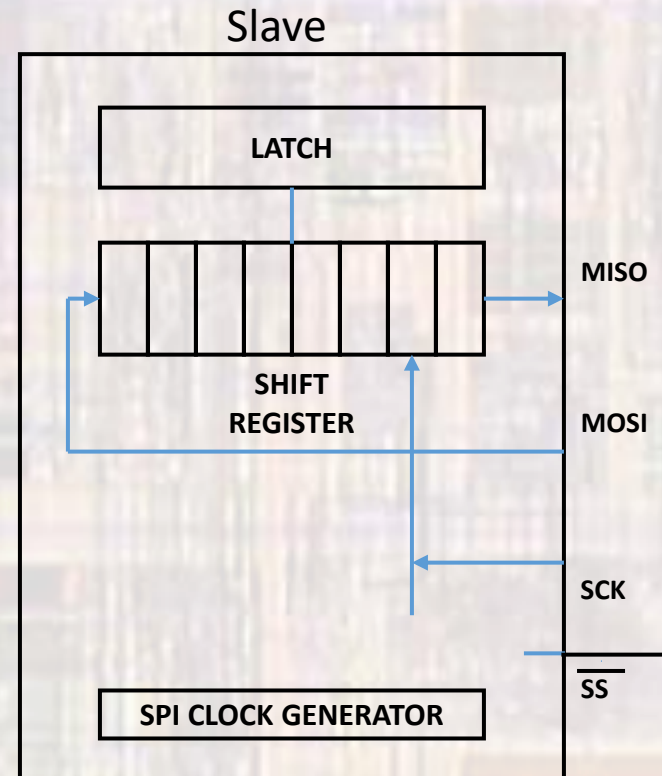    - Slave – receives clock from the master

# SPI Review

- Overview

Master

| LATCH |
| SHIFT REGISTER |

MISO

MOSI

SCK

$\overline{SS}$

SPI CLOCK GENERATOR

Slave

| LATCH |
| SHIFT REGISTER |

MISO

MOSI

SCK

$\overline{SS}$

SPI CLOCK GENERATOR

MISO – Master:IN or Slave:OUT

MOSI – Master:OUT or Slave:IN

SCK – SPI CLK

$\overline{SS}$ – Slave Select Bar

# SPI Review

- Operation

Master                                                        Slave

| LATCH | | | | | | | | | | LATCH |

SHIFT REGISTER

SHIFT REGISTER

MISO          MISO

MOSI          MOSI

SCK          SCK

$\overline{SS}$    X       0    $\overline{SS}$

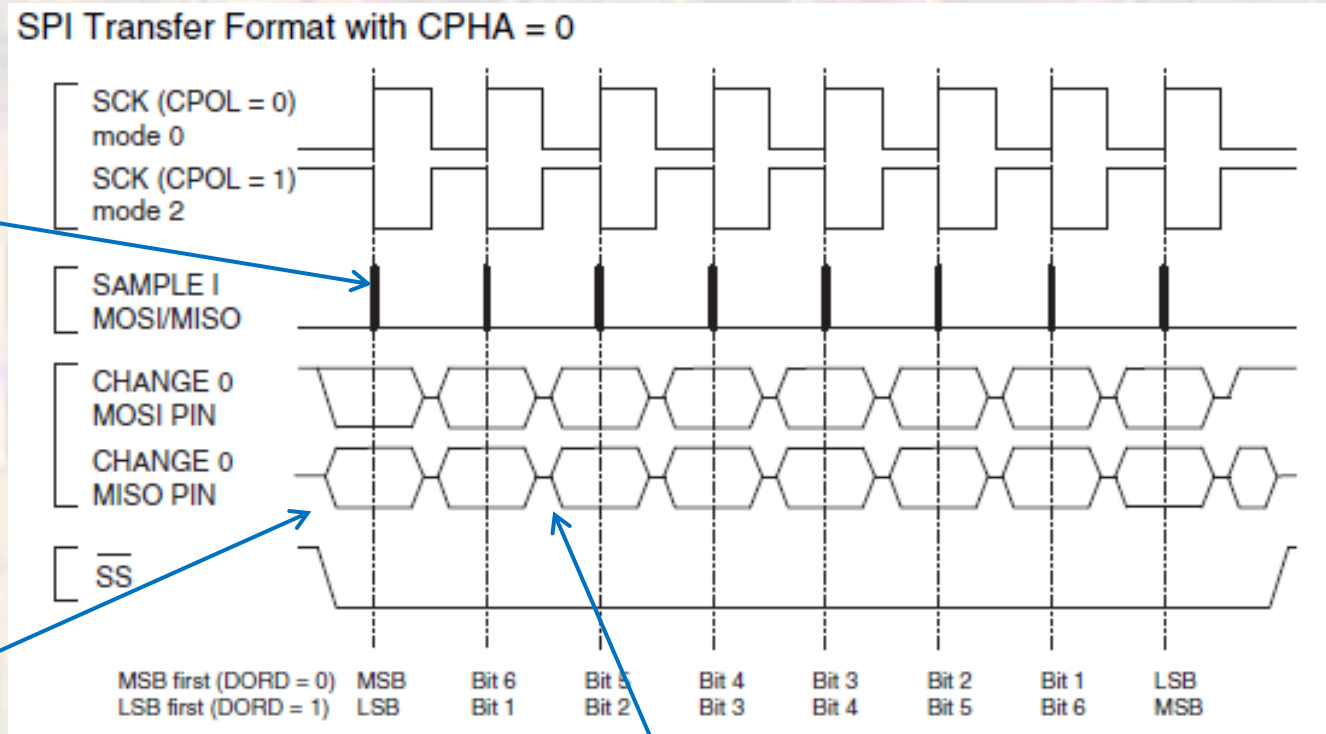SPI CLOCK GENERATOR          SPI CLOCK GENERATOR
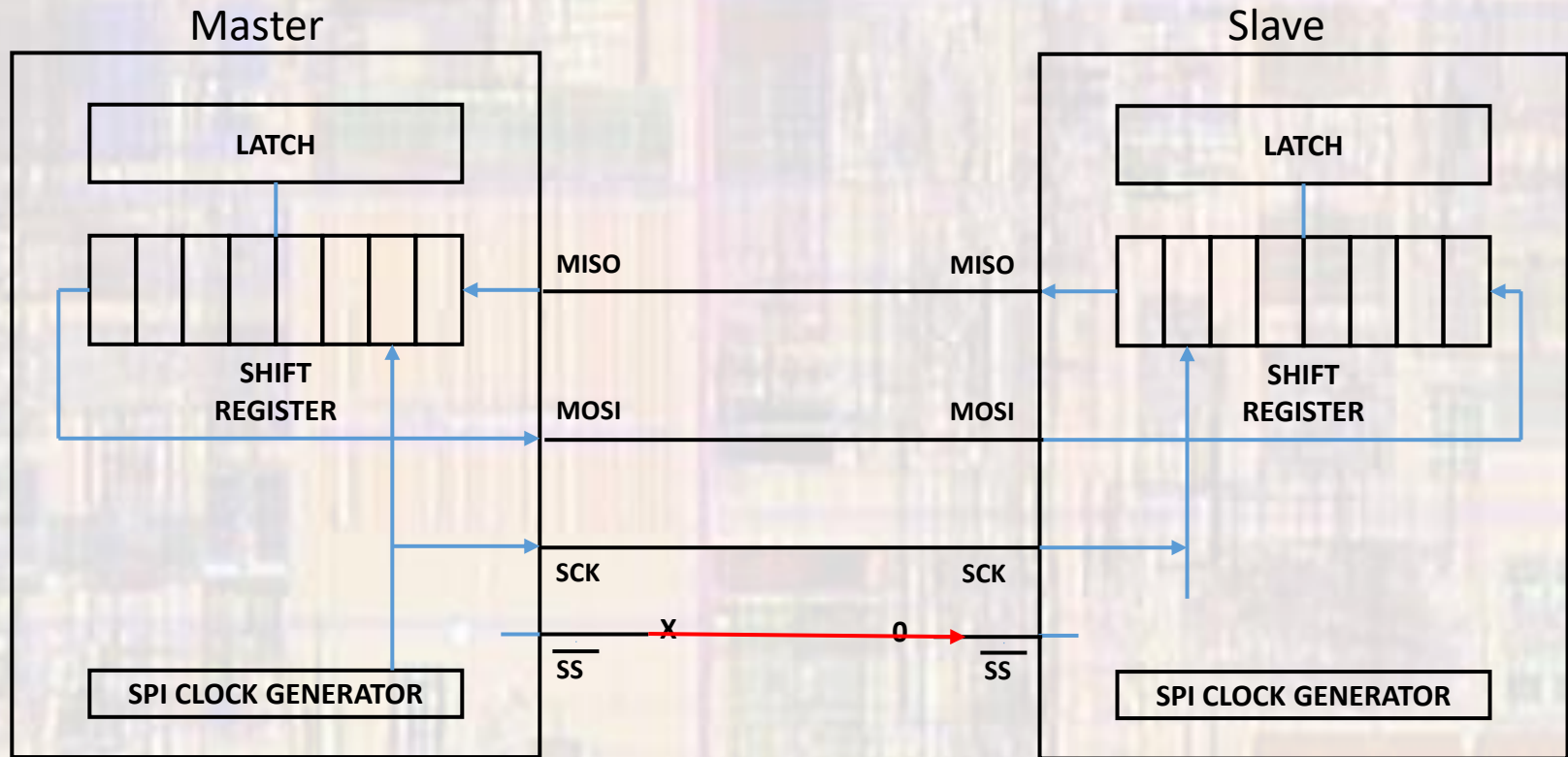
Latch → Shift Register in both master and slave
Master generates 8 clocks → shifts both registers (swaps content)
Shift Register → Latch in both master and slave

# SPI Review

- Operation

  - CPHA = 0

Captured in register on leading clock edge

Values active on pins as soon as SSbar goes low

New values placed on pins on trailing clock edge

SPI Transfer Format with CPHA = 0

SCK (CPOL = 0) mode 0
SCK (CPOL = 1) mode 2

SAMPLE I MOSI/MISO

CHANGE 0 MOSI PIN

CHANGE 0 MISO PIN

$\overline{SS}$

| | MSB first (DORD = 0) | MSB | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | LSB |
| | LSB first (DORD = 1) | LSB | Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | MSB |

# SPI Review

- Operation

  - CPHA = 1



SPI Transfer Format with CPHA = 1

Captured in register on trailing clock edge

Values active on pins on first clock edge
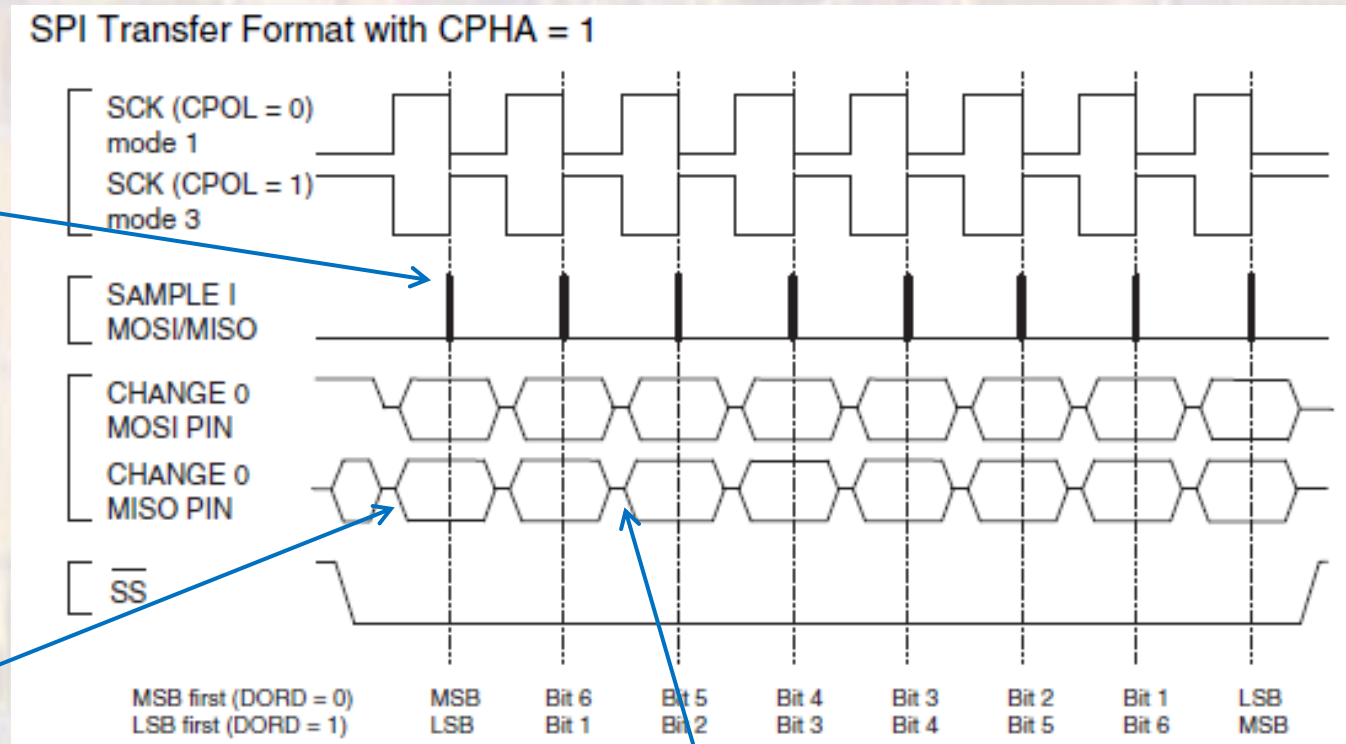
New values placed on pins on leading clock edge
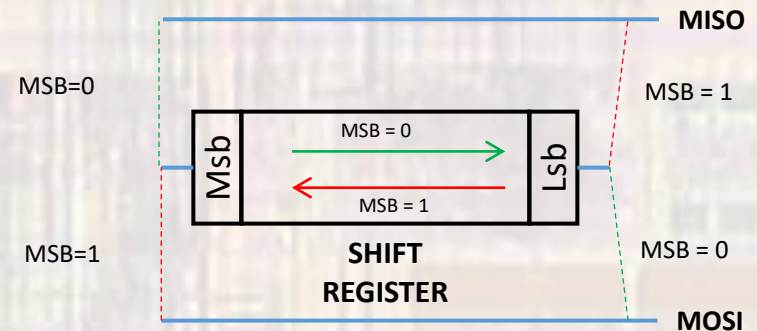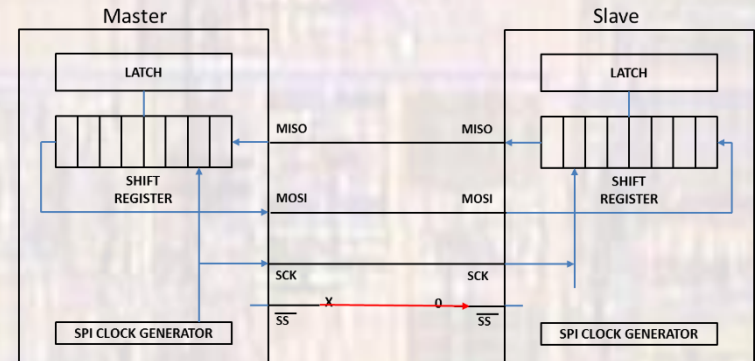
# SPI Review

- Operation

  - Configure 1 device as master
  - Configure 1 or more devices as
        slaves
  - Load values into register(s)
  - Pull SSbar low on the desired slave device
  - Initiate transfer by writing to the data register
    - The master will generate the appropriate clocks
  - If interrupts are enabled – an interrupt will be generated on completion
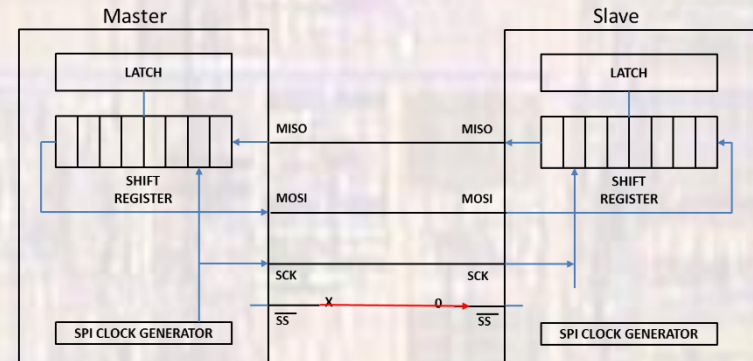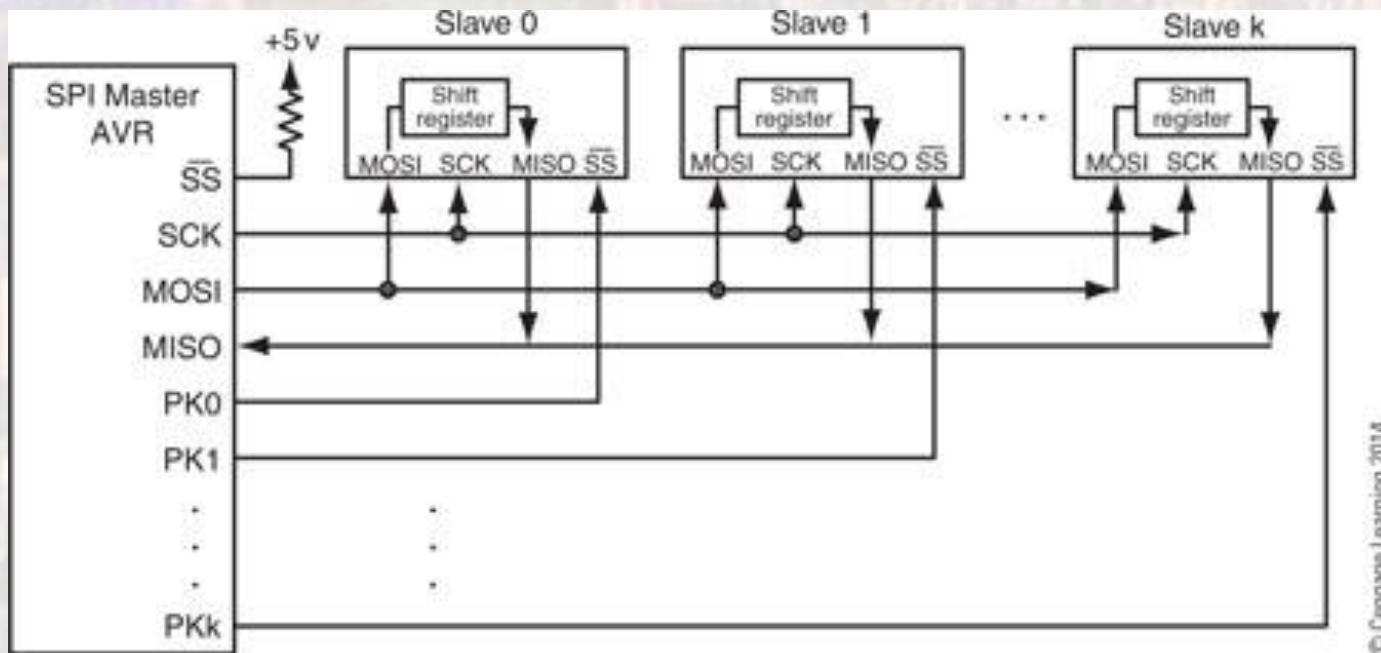
# SPI Review

- Operation

  - 2 options for clock polarity
    - CKPL = 0 → rising edge triggered
    - CKPL = 1 → falling edge triggered

  - 2 options for clock phase
    - CKPH = 0 → leading edge triggered
    - CKPH = 1 → trailing edge triggered

  - 2 options on transfer direction
    - MSB = 0 → LSB transferred first
    - MSB = 1 → MSB transferred first



Master / Slave shift register diagram with LATCH, SHIFT REGISTER, SPI CLOCK GENERATOR, MISO, MOSI, SCK, SS



Shift register diagram showing MISO, MOSI, Msb, Lsb, MSB = 0, MSB = 1

# SPI Review

- Operation

  - Multiple Slave Configuration



**Figure 14.7** ■ Single-master and multiple-slave device connection (method 1)

# SPI Review

- Operation

- Multiple Slave – Extended Shift Configuration



**Figure 14.8** ■ Single-master and multiple-slave device connection (method 2)