State Machines

Last updated 7/18/23

State Machines

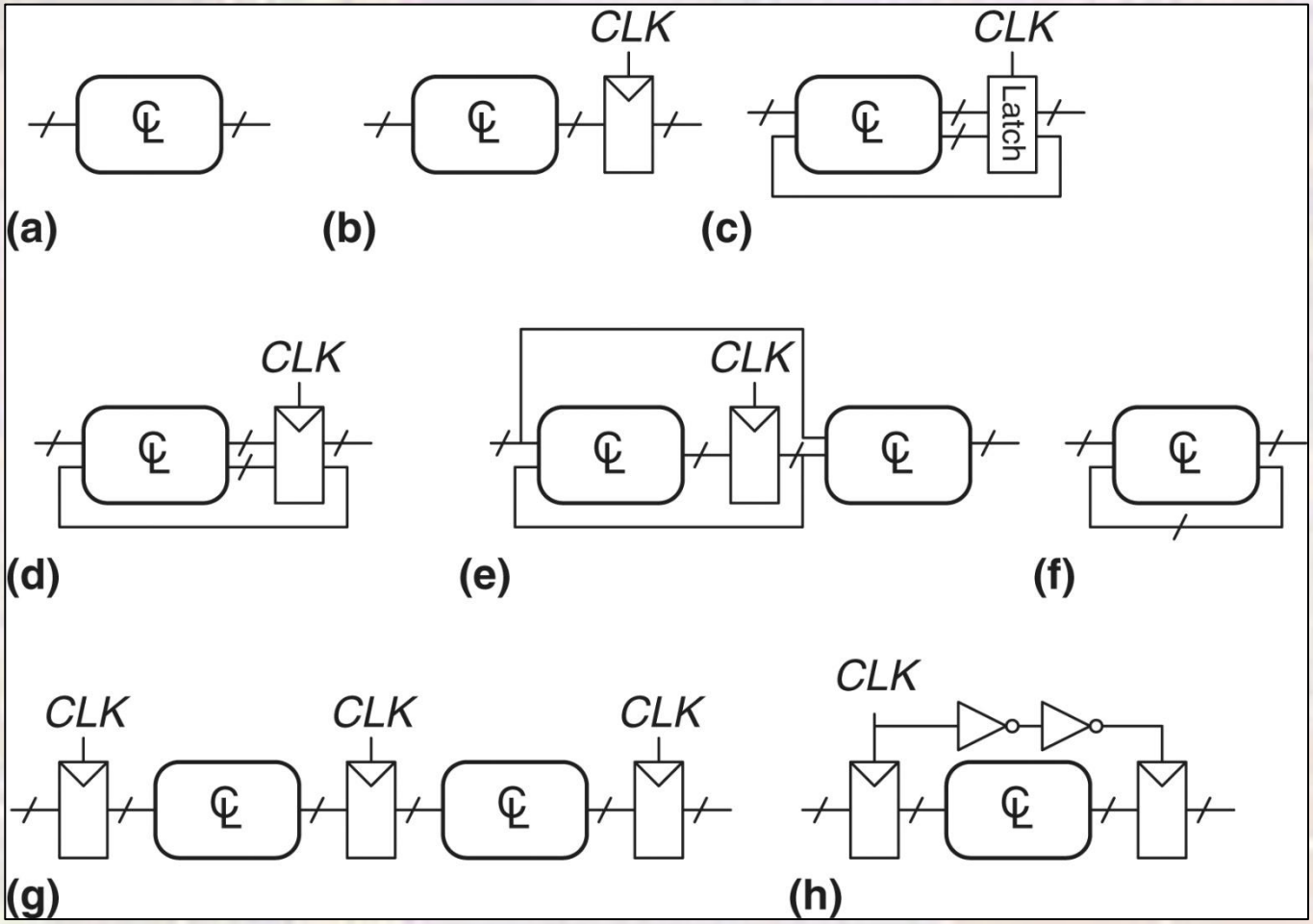
- Synchronous Sequential Circuit
  - Synchronous
    - Outputs change on a clock edge
    - One common clock
  - Sequential
    - Involves memory
    - Register(s)
  - 2 generalized types
    - Finite State Machines
    - Pipelined Machines

State Machines

- Synchronous Sequential Circuit
  - Rules
    - Every element is either a
      - Register
      - Combinational Logic
    - At least one element is a register
    - All registers are driven by the same clock
    - Every cyclic path contains at least one register

State Machines

- Synchronous Sequential Circuit
  - Rules



src: Harris & Harris

State Machines

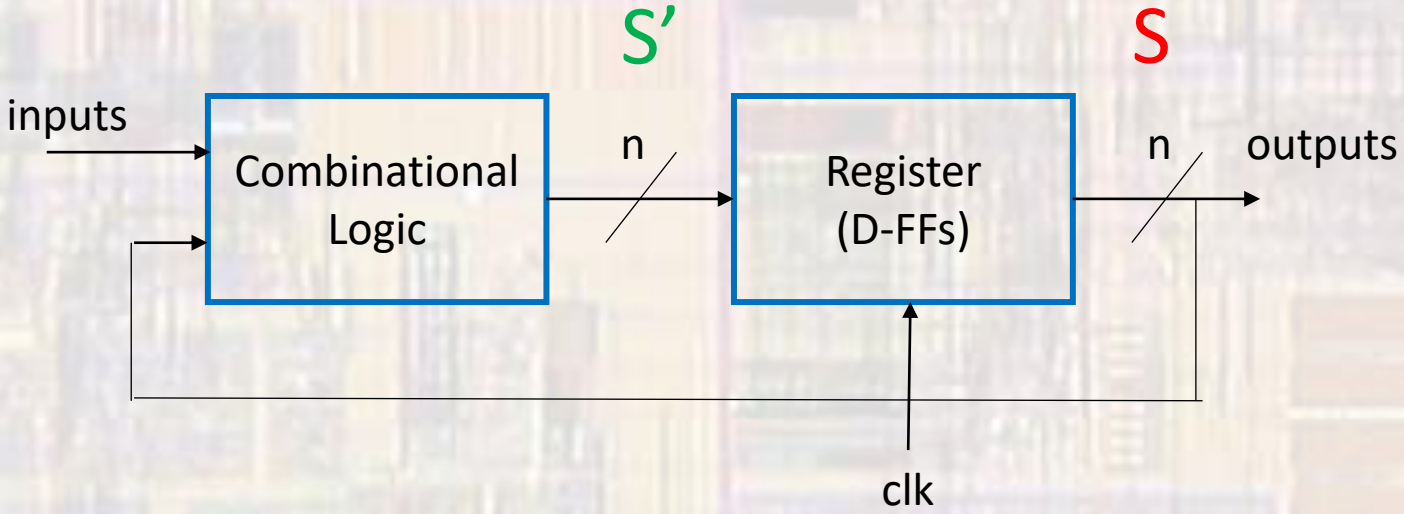
- Synchronous Sequential Circuit
  - State
    - Collection of all unique values held in memory elements
    - 1 D-FF can hold 2 states (0 or 1)
    - 4 D-FFs can hold 16 states (0000, 0001, 0010, … 1111)
  - State Variable
    - Ordered collection of memory elements
    - Can hold any of 2^n states
    - 1 D-FF can have 1 state variable (Q)
    - 4 D-FFs can have 1 state variable (S) with 16 possible values

Actually, there are many more possible values – what are they?

State Machines

- Finite State Machine
  - Finite – fixed size of register → finite number of states
  - State / Next State
    - State (S) - current value of a State Variable
    - Next State (S') - future value of a State Variable (next clock cycle)

    - If we know what S is, we can figure out what S' is
    - If we know what S' is, we know what S WILL BE after the next clock

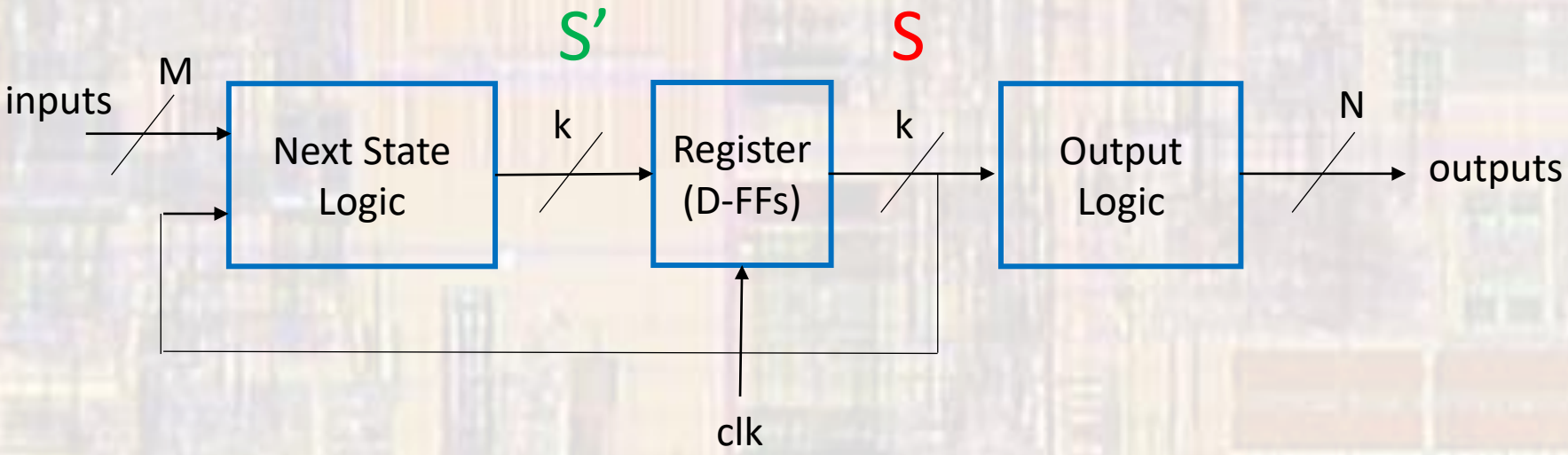


State Machines

- Finite State Machine
  - Finite
    - n storage elements (D-FFs) → 2^n states – not infinite
  - State
    - Meets the requirements for a synchronous sequential circuit
  - 2 common types
    - Mealy Machine
    - Moore Machine

State Machines

- Finite State Machine
  - Moore Machine
    - Outputs depend only on the current state(S)



State Machines

- Finite State Machine
  - Mealy Machine
    - Outputs depend on the current state(S) and the inputs