VHDL Assert

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VHDL Assert

- Assert
  - Test and debug instruction
  - Format [ ] indicates optional

```
[label:] assert condition
[report "message_string"]
[severity severity_level];
```

  - Action
    - If assert condition is TRUE – nothing happens
    - If assert condition is FALSE – report and severity lines are executed

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VHDL Assert

- Assert example - 1
  - Assume a std_logic signal named EMPTY
  - Setup a test to force the signal to go high
  - Add the assert command

```
assert EMPTY = '1'
   report "ERROR: FIFO should be EMPTY after RSTB: "
   severity error;
```

  - If the EMPTY signal is 1 – nothing happens
  - If the EMPTY signal is 0:

    The report is printed in the simulation log

    An error is reported in the simulation log

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VHDL Assert

- Assert example - 2
  - Assume an 8 bit std_logic_vector signal named DATA_OUT
  - Setup a test to force the DATA_OUT to 5
  - Add the assert command

```
assert DATA_OUT = std_logic_vector(to_unsigned(5, 8))
   report "ERROR: First FULL data read is incorrect."
   severity error;
```

  - If the DATA_OUT signal matches the bits for unsigned 5

    Nothing happens
  - Otherwise:

    The report is printed in the simulation log

    An error is reported in the simulation log

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VHDL Assert

- Assert – Conditions
  - The condition can be any valid VHDL expression
    - Includes all of the VHDL type matching requirements

std_logic	assert std_logic_sig = ‘0’	single quotes required
std_logic_vector	assert my_slv_sig = “0110”	double quotes required
unsigned/signed	assert my_sig >= 5	
enumerated state	assert state = IDLE	

    - Type conversions are allowed

SLV to integer	assert to_integer(unsigned(my_slv_sig)) = 5
integer to SLV	assert std_logic_vector(to_unsigned(5, 8)) = my_slv_sig

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VHDL Assert

- Assert – Data values
  - The report can only include strings
  - Multiple strings can be included by concatenating '&' them
  - Data values can be included in the report by turning them into strings – but this is not supported by our tools
  - Integers can be included in the report by using the 'image attribute
    - This turns an integer into the appropriate text string

  - Assume an 8 bit std_logic_vector signal named DATA_OUT
  - Setup a test to force the DATA_OUT to 5
  - Add the assert command

```
assert DATA_OUT = std_logic_vector(to_unsigned(5, 8))
   report "ERROR: First FULL data read is incorrect." &
          " measured " & integer'image(to_integer(unsigned(DATA_OUT))) &
          " expected " & integer'image(5)
   severity error;
```


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VHDL Assert

- Assert – Severity levels
  - NOTE
    - Informational messages
    - Simulation continues
  - WARNING
    - Highlights unusual or potentially problematic conditions
    - Simulation continues
  - ERROR
    - Indicates a design or testbench bug
    - Simulator setting determine whether the simulation continues
      - Default for our tools is - continue
  - FAILURE
    - Indicates a fatal violation
    - This forces the simulator to stop immediately

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VHDL Assert

- Report
  - A report can be made with or without an assert

```
report “Memory load test complete”
```


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