Behavioral VHDL

Last updated 8/10/24

Behavioral VHDL

- Behavioral VHDL describes the behavior of the circuit
  - Concurrent logic
  - Sequential Logic
  - Memories
  - Finite State Machines
  - …

Behavioral VHDL

- Behavioral VHDL file components
  - Header
    - Description of who created the file
    - Description of the purpose of the block
    - Description of inputs and outputs
  - Inclusions
    - Any libraries that will be referenced in the design
  - Entity
    - Formal definition of the inputs and outputs
    - Any generic parameters are defined here also
  - Architecture
    - Internal signal declarations
    - HDL description of the desired functionality
      - Concurrent, sequential logic

Behavioral VHDL

- Behavioral VHDL file components - example

```
----------------------------
--
-- basic_vhdl.vhdl
-- Created: 7/16/18
-- By: johnsontimoj
-- For: EE3921
--

-- File Overview ---
--
-- This file demonstrates basic VHDL file structure

-- File Details ---
-----------------------------
```

Header Information

Document
who, when, what and how

Should be sufficient to allow a co-worker to use/modify the design

Behavioral VHDL

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Header Information

```
-- Library inclusions
library IEEE;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
```

Library Inclusions

Companies may have their own libraries
- we will use the IEEE standard library

Only include the portions of the library you need
- ieee.std_logic_1164.all provides:
  - std_logic
  - std_logic_vector
  - 9 logic levels
- ieee.numeric_std.all provides
  - Signed vectors – signed, unsigned

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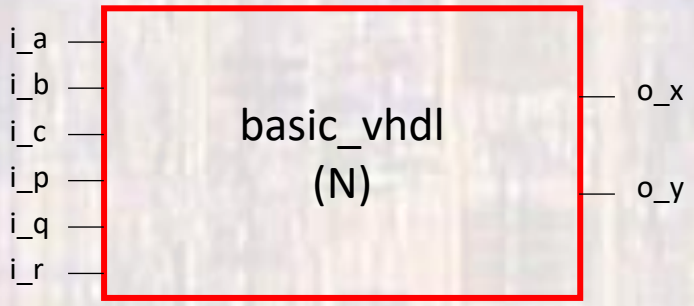
Library Inclusions



Generic

Ports

```
-- Entity definition
entity basic_vhdl is
    generic( N:     positive := 8);
    port(    i_a:   in       std_logic;
             i_b:   in       std_logic;
             i_c :  in       std_logic;
             i_p:   in       std_logic_vector(N-1 downto 0);
             i_q:   in       std_logic_vector(N-1 downto 0);
             i_r :  in       std_logic_vector(N-1 downto 0);
             o_x:   out      std_logic;
             o_y:   out      std_logic_vector(N-1 downto 0)
    );
end entity;
```

Entity

The Entity is the external view of the block

Generics indicate 'adjustable' aspects of the block

Ports are the i/o connections of the block

Ports have a direction but no interpretation

Wires

Limited to std_logic or std_logic_vector for us

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Header Information

The Architecture is the operational description of the block
- Behavioral
- Structural
- Testbench
- …

Before the begin
- Internal signals
- Constants used for readability

After the begin
- HDL for the specific application

```
        i_q:    in      std_logic_vector(N-1 downto 0);
        i_r :   in      std_logic_vector(N-1 downto 0);
        o_x:    out     std_logic;
        o_y:    out     std_logic_vector(N-1 downto 0)
    );
end entity;
```

```
-- Behavioral Architecture Definition
architecture behavioral of basic_vhdl is
    signal e:   std_logic;
    signal f:   std_logic;
    signal g:   std_logic;
    signal t:   unsigned(N-1 downto 0);
    signal u:   signed(N-1 downto 0);

    Begin

        e <= i_a and i_b;
        f <= i_c nor i_a;
        g <= e xor f;
        o_x <= g and not i_p(3);

        t <= unsigned(i_p xor i_q);
        u <= signed("11" & i_a & t(4) & i_r(3 downto 2) & i_a & g);
        o_y <= (7 => '1' , 4 => u(5), 1 => i_a , 5 => t(4) , others => '1' );    -- array assignment

end architecture;
```

Architecture

Internal signals

Architectural Definition

Behavioral VHDL

- Behavioral VHDL file components - example

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Library Inclusions

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              i_p:    in      std_logic_vector(N-1 downto 0);
              i_q:    in      std_logic_vector(N-1 downto 0);
              i_r :   in      std_logic_vector(N-1 downto 0);
              o_x:    out     std_logic;
              o_y:    out     std_logic_vector(N-1 downto 0)
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end entity;
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Entity

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Architecture