Concurrent VHDL

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- Concurrent Logic in HDL
  - Concurrent activities are happening all the time (in parallel)
    - Assignment: <=
    - with-select
    - when-else
    - AND, OR, NOT, …

    x <= a AND (NOT b);

    y <= a when (b = '1') else c;

    z <= (b OR c) when (d = '0') else (e AND f);

      x, y, z can change if any value changes, immediately