VHDL Constants

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VHDL Constants

- Constants in VHDL are values that cannot change
  - Can be std_logic, std_logic_vectors, signed, or unsigned for signals (synthesizable)
  - Can be any other valid VHDL type for calculation purposes
    - Must be compile time calculations
  - Can be used like a generic for the purpose a setting a value once and using it multiple places
    - Cannot be changed during instantiation

    - Format: constant name : type := value;

      the value may be a calculation based on other constants or generics but cannot be based on a signal (must be known at compile time)

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- Examples

```
constant num_bits : natural := 8;        - - natural because must be > 0

constant combination : std_logic_vector(5 downto 0) := “10010”      - - combination code value

constant max_allowed : unsigned(7 downto 0) := to_unsigned( 145, 8);    -- set to 145

constant max_sig_size : unsigned((num_bits – 1) downto 0) := to_unsigned(((2 ** num_bits) – 1), num_bits);
                                                                  - - sets value to all 1s
                                                                  - - num_bits must be previously defined


-- determine the number of bits required to hold a number
constant num_elements : natural := 4321;
constant num_bits : natural := integer(ceil(log2(real(num_elements))));
```


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