VHDL Entity

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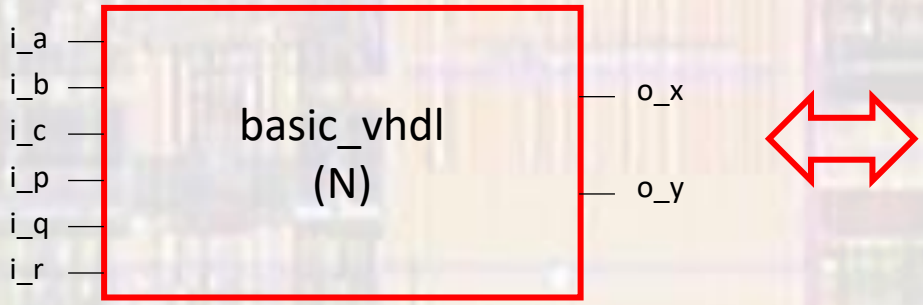
VHDL Entity

- The Entity is the external view of the block
  - Inputs
  - Outputs
  - Parameters - generics

Just wires (ports) no interpretation
ALWAYS std_logic or std_logic_vector() for us



Generic

```
-- Entity definition
entity basic_vhdl is
    generic( N:     positive := 8);
    port(   i_a:    in      std_logic;
            i_b:    in      std_logic;
            i_c :   in      std_logic;
            i_p:    in      std_logic_vector(N-1 downto 0);
            i_q:    in      std_logic_vector(N-1 downto 0);
            i_r :   in      std_logic_vector(N-1 downto 0);
            o_x:    out     std_logic;
            o_y:    out     std_logic_vector(N-1 downto 0)
    );
end entity;
```

Ports