

Sequential VHDL

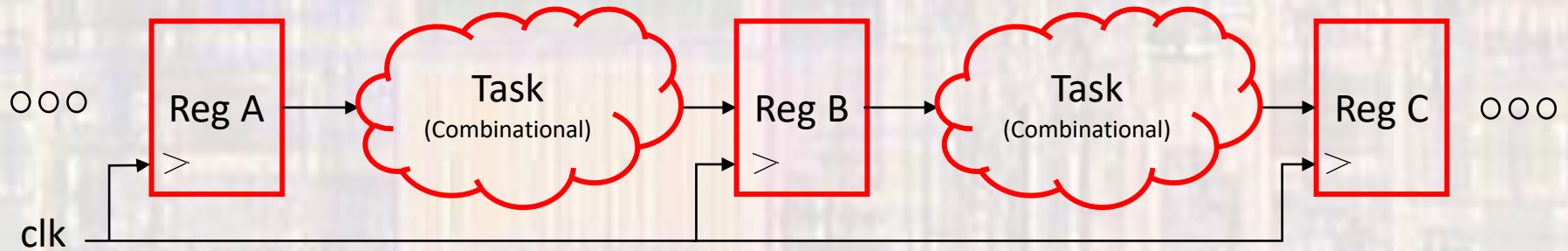
Last updated 8/19/24

Sequential VHDL

- Sequential Logic in HDL
 - Sequential activities only happen in certain situations
 - E.g. Rising edge of clock
 - Sequential activities are identified by placing them in a “process” block
 - Process blocks are only executed when a signal in the blocks “sensitivity list” changes
 - Sequential Signals are ONLY updated at the end of the process block
 - Process blocks themselves are concurrent activities

Sequential VHDL

- RTL – Register Transfer Level (logic)
 - Sequential VHDL structure



Sequential VHDL

- Code constructs
 - Inside processes
 - if – else
 - case
 - with-select (2008)
 - when-else (2008)
 - Assignment `<=`
 - OR, AND, NOT, ...
 - See the VHDL Processes slides for details