DDR5 SDRAM

Product Core Data Sheet

Features

- V_{DD} = V_{DDQ} = 1.1V (nom)
- V_{PP}= 1.8V (nom)
- On-die, internal, adjustable V_{REF} generation for DQ, CA, CS
- 1.1V pseudo open-drain I/O
- TC maximum up to 95°C
  - 32ms, 8192-cycle refresh up to 85°C
  - 16ms, 8192-cycle refresh at >85°C to 95°C
- 32 internal banks (x4, x8): 8 groups of 4 banks each
- 16 internal banks (x16): 4 groups of 4 banks each
- 16n-bit prefetch architecture
- 1 cycle/2 cycle command structure
- 2N mode
- All bank and same bank refresh
- Multi-purpose command (MPC)
- CS/CA training mode
- On-die ECC
- ECC transparency and error scrub
- Decision feedback equalization (DFE)
- Loopback mode
- Command-based non-target (NT) nominal, DQ/DQS park, and dynamic WR on-die termination (ODT)
- sPPR and hPPR capability
- JEDEC JESD-79.5 compliant

Options[1]

- Configuration
  - Refer to the DDR5 Die Revision-specific data sheet
- FBGA package (Pb-free) — x4, x8
  - Refer to the DDR5 Die Revision-specific data sheet
- FBGA package (Pb-free) — x16
  - Refer to the DDR5 Die Revision-specific data sheet
- Timing – cycle time
  - Refer to the DDR5 Die Revision-specific data sheet
- Operating temperature
  - Refer to the DDR5 Die Revision-specific data sheet

Notes: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on micron.com for available offerings.

General Specification Details

This document serves as the core data sheet specification for the DDR5 family of Micron DRAM products. Along with this core document, each DDR5 die revision has a specific data sheet specification (for example, 16Gb DDR5 SDRAM Die Revision A Data Sheet Addendum).

Content in the die revision specific DDR5 data sheet addendum supersedes content defined in this core DDR5 specification.

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Basic Functionality

DDR5 is a high-speed dynamic random-access memory. The 8Gb density is internally configured as:

- x4/x8 devices: 16 banks (8 bank group with 2 banks for each bank group)
- x16 devices: 8 banks (4 bank group with 2 banks for each bank group)

With higher densities (greater than or equal to 16Gb), the bank resources double, enabling the device to be internally configured as:

- x4/x8 devices: 32 banks (8 bank group with 4 banks for each bank group)
- x16 devices: 16 banks (4 bank group with 4 banks for each bank group)

DDR5 uses a 16n pre-fetch architecture to achieve high-speed operation. The 16n pre-fetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation consists of a single 16n-bit wide, eight clock data transfer at the internal core and 16 corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

READ and WRITE operations are burst-oriented, start at a selected location, and continue for a burst length of 16 (BL16) or a chopped burst of eight (BC8) in a programmed sequence. Operation begins with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered with the ACTIVATE command are used to select the bank and row to be activated (see DDR5 Addressing for specific requirements). The address bits registered with the READ or WRITE command select the starting column location for the burst operation, determine if the AUTO PRECHARGE command is to be issued, and select BC8 on-the-fly (OTF), fixed BL16, fixed BL32 (optional), or BL32 OTF (optional) mode if enabled in the mode register.

Prior to normal operation, the device must be powered up and initialized in a predefined manner.

The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

Functional Description

This simplified state diagram is intended to provide an overview of the possible state transitions and the commands to control them. Some events are not captured in full detail; in particular, situations involving more than one bank and the enabling or disabling of on-die termination.

Figure 1: Simplified State Diagram

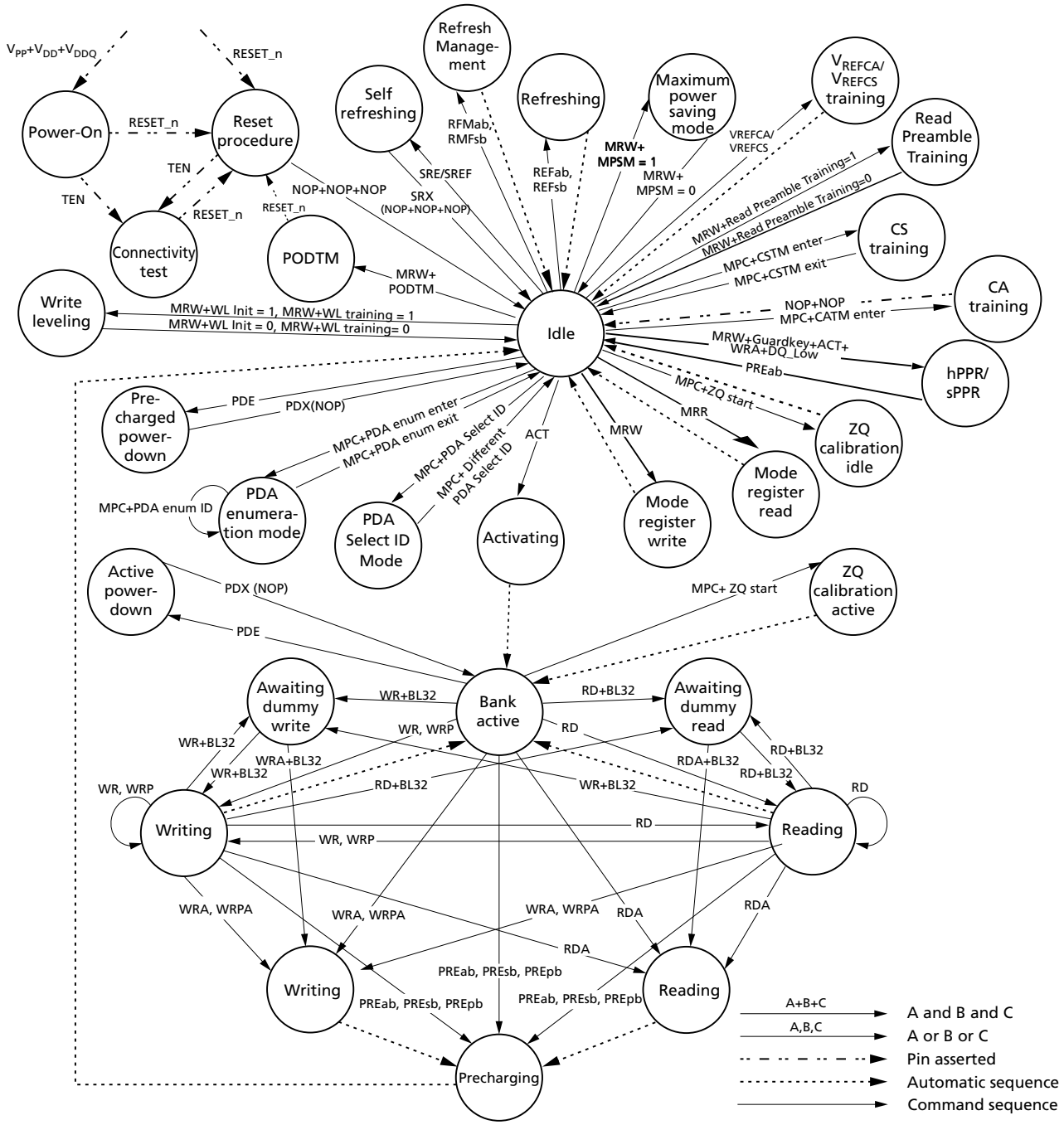


Table 1: State Diagram Command Definitions

Abbreviation	Function
ACT	Activate
MPC	Multi-purpose command
MRR	Mode register read
MRW	Mode register write
NOP	No operation
PDE	Power-down entry mode
PDX	Power-down exit mode
PREab	Precharge all banks
PREpb	Precharge per bank
PREsb	Precharge same bank
RD	Read
RDA	Read auto precharge
REFab	Refresh all banks
REFsb	Refresh same bank
RFMab	Refresh management all banks
RFMsb	Refresh management same bank
RFU	Reserved for future use
RESET_n	Start reset procedure
SRE	Self-refresh entry mode
SRX	Self-refresh exit mode
SREF	Self refresh entry with frequency change
VREFCA	VREFCA command
VREFCS	VREFCS command
WR	Write
WRA	Write auto precharge
WRP	Write pattern
WRPA	Write pattern auto precharge

DDR5 Addressing

Table 2: 8Gb Addressing

Configuration		2Gb x4	1Gb x8	512Mb x16
Bank address	Number of bank groups/number of banks per bank group/number of banks	8 / 2 / 16	8 / 2 / 16	4 / 2 / 8
	Bank group address	BG0-BG2	BG0-BG2	BG0-BG1
	Bank address in a bank group	BA0	BA0	BA0
Row address		R0-R15	R0-R15	R0-R15
Column address		C0-C10	C0-C9	C0-C9
Page size		1KB	1KB	2KB
Chip IDs/maximum stack height		CID0-3 / 16H	CID0-3 / 16H	CID0-3 / 16H

Table 3: 16Gb Addressing

Configuration		4Gb x4	2Gb x8	1Gb x16
Bank address	Number of bank groups/number of banks per bank group/number of banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
	Bank group address	BG0-BG2	BG0-BG2	BG0-BG1
	Bank address in a bank group	BA0-BA1	BA0-BA1	BA0-BA1
Row address		R0-R15	R0-R15	R0-R15
Column address		C0-C10	C0-C9	C0-C9
Page size		1KB	1KB	2KB
Chip IDs/maximum stack height		CID0-3 / 16H	CID0-3 / 16H	CID0-3 / 16H

Table 4: 24Gb Addressing

Configuration		6Gb x4	3Gb x8	1.5Gb x16
Bank address	Number of bank groups/number of banks per bank group/number of banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
	Bank group address	BG0-BG2	BG0-BG2	BG0-BG1
	Bank address in a bank group	BA0-BA1	BA0-BA1	BA0-BA1
Row address[1]		R0-R16	R0-R16	R0-R16
Column address		C0-C10	C0-C9	C0-C9
Page size		1KB	1KB	2KB
Chip IDs/maximum stack height		CID0-3 / 16H	CID0-3 / 16H	CID0-3 / 16H

Notes: 1. For non-binary memory densities, a quarter of the row address space is invalid. When the MSB address bit is HIGH, the MSB-1 address bit is LOW. An ACT command with row address inputs that violate this restriction follows all timing and protocol rules as though the ACT command was valid. Any RD or RDA command to a bank following an invalid ACT command to that same bank drives the DQS strobes with normal timing, but does not expose information that can be used to learn about data stored in cells with valid addresses. Data being sent that coincidentally matches cell array data is permissible (for example, always sending the all 1s and cell data sometimes being all 1s).

Consistently exposing data from a previous READ or previous ACTIVATE is not permissible. Any WR, WRA, WRP or WRPA command to a bank following an invalid ACT command to that same bank does not result in new data being written anywhere within the device. The device operates normally for READ and WRITE commands to banks that have pages open to valid rows.

Table 5: 32Gb Addressing

Configuration		8Gb x4	4Gb x8	2Gb x16
Bank address	Number of bank groups/number of banks per bank group/number of banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
	Bank group address	BG0-BG2	BG0-BG2	BG0-BG1
	Bank address in a bank group	BA0-BA1	BA0-BA1	BA0-BA1
Row address		R0-R16	R0-R16	R0-R16
Column address		C0-C10	C0-C9	C0-C9
Page size		1KB	1KB	2KB
Chip IDs/maximum stack height		CID0-3 / 16H	CID0-3 / 16H	CID0-3 / 16H

Table 6: 64Gb Addressing

Configuration		16Gb x4	8Gb x8	4Gb x16
Bank address	Number of bank groups/number of banks per bank group/number of banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
	Bank group address	BG0-BG2	BG0-BG2	BG0-BG1
	Bank address in a bank group	BA0-BA1	BA0-BA1	BA0-BA1
Row address		R0-R17	R0-R17	R0-R17
Column address[1]		C0-C10	C0-C9	C0-C9
Page size		1KB	1KB	2KB
Chip IDs/maximum stack height		CID0-2 / 8H	CID0-2 / 8H	CID0-2 / 8H

Notes: 1. While the column addressing rows indicate the LSB is C0, in fact, C0 and C1 are controlled internally by the burst logic. As shown in the Command Truth Table, C0 and C1 states are not selectable by any column access burst command such that the burst would be reordered.

Reset and Initialization Procedure

The table below defines the default values of the mode registers. Mode registers not shown in this table have a default value of zero (0).

Table 7: Mode Registers with Default States

Item	MR	Op-code(s)	Default Setting	Description
Burst Length	0	[1:0]	00b	BL16
Read Latency (RL) = CAS Latency (CL)	0	[6:2]	00010b	CL = 26 @3200
Write Latency (WL) = CAS Write Latency (CWL)	N/A	N/A	CWL = CL-2	Fixed; based on CL setting
PDA Enumerate ID	1	[3:0]	1111b	PDA enumerate ID
PDA Select ID	1	[7:4]	1111b	PDA select ID
Write Recovery	6	[3:0]	0000b	^{t}WR = 48CK @3200[1]
Read to Precharge Delay	6	[7:4]	0000b	^{t}RTP = 12CK @3200[1]
Write Preamble	8	[4:3]	01b	2 ^{t}CK
V_{refDQ} Value	10	[7:0]	00101101b	V_{refDQ} Range: 75% of V_{DDQ}
V_{refCA} Value	11	[6:0]	0101101b	V_{refCA} Range: 75% of V_{DDQ}
V_{refCS} Value	12	[6:0]	0101101b	V_{refCS} Range: 75% of V_{DDQ}
ECS Error Threshold Count (ETC)	15	[2:0]	011b	256
Read Training Data0	26	[7:0]	Register value = 0x5A	
Read Training Data1	27	[7:0]	Register value = 0x3C	
Read LFSR	30	[7:0]	Register value = 0xFE	
CK ODT	32	[2:0]	Based on strap value	Group A = RTT_OFF = 000b Group B = 40 ohms = 111b
CS ODT	32	[5:3]	Based on strap value	Group A = RTT_OFF = 000b Group B = 40 ohms = 111b
CA ODT	33	[2:0]	Based on strap value	Group A = RTT_OFF = 000b Group B = 80 ohms = 100b
RTT_WR	34	[5:3]	001b	240 ohms
RTT_NOM_WR	35	[2:0]	011b	80 ohms
RTT_NOM_RD	35	[5:3]	011b	80 ohms
ODTLon_WR_Offset	37	[2:0]	100b	–1 clocks
ODTLoff_WR_Offset	37	[5:3]	101b	0 clocks
ODTLon_WR_NT_Offset	38	[2:0]	100b	–1 clocks
ODTLoff_WR_NT_Offset	38	[5:3]	101b	0 clocks
ODTLon_RD_NT_Offset	39	[2:0]	100b	–1 clocks
ODTLong_RD_NT_Offset	39	[5:3]	101b	0 clocks
RFM	58	[0]	See DDR5 Die Revision specific Datasheet	Refresh management required/not required

Table 7: Mode Registers with Default States (Continued)

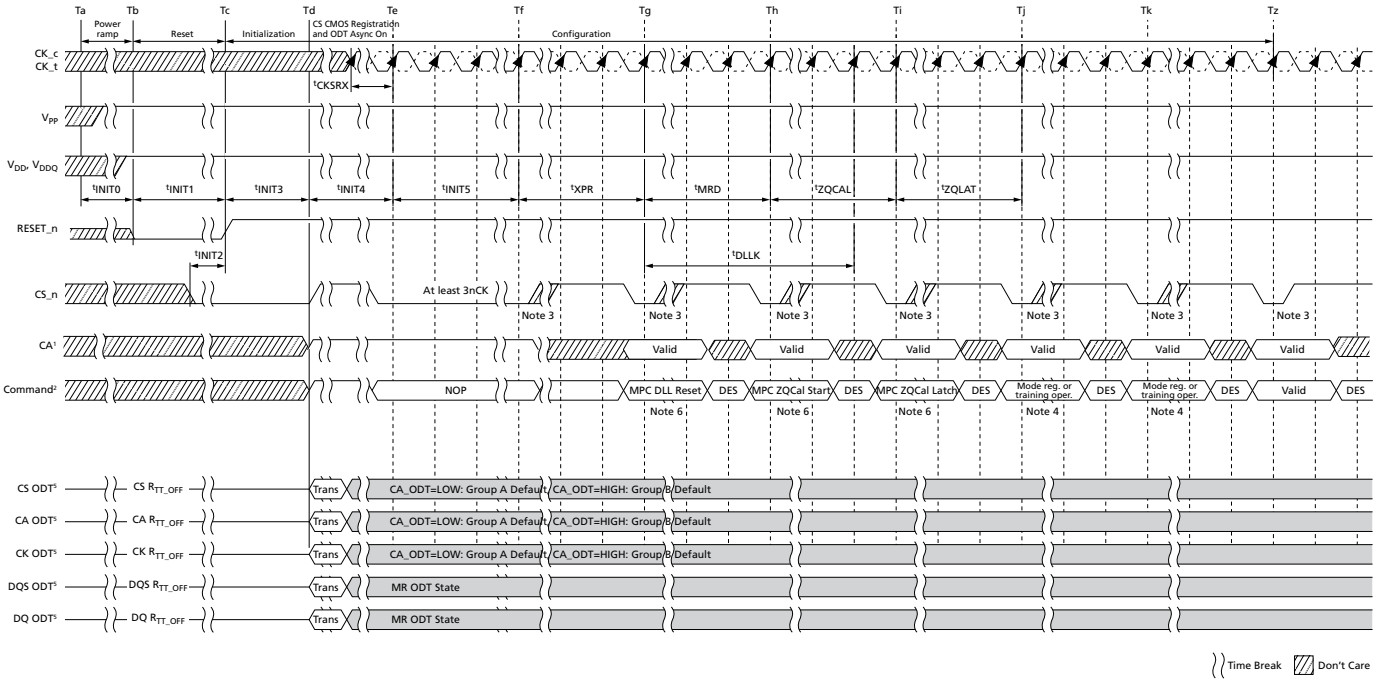
Item	MR	Op-code(s)	Default Setting	Description
RFM RAAIMT	58	[4:1]	See DDR5 Die Revision specific Datasheet	Rolling accumulated ACT initial management threshold
RFM RAAMMT	58	[7:5]	See DDR5 Die Revision specific Datasheet	Rolling accumulated ACT maximum management threshold
RFM RAA Counter	59	[7:6]	See DDR5 Die Revision specific Datasheet	Rolling accumulated ACT counter decrement per REF command

Notes: 1. See the Timing by Speed Grade Table for the timing parameter.

Power-up and Initialization

The following sequence and conditions are required for power-up and initialization, as shown in the figure below.

Figure 2: Reset and Initialization Sequence at Power-on Ramping



Notes: 1. From (Td) until (Te), the CA bus must be held HIGH.
2. From (Te) until (Tf), NOP commands must be applied on the command bus.
3. From (Tf) until (Tz), DES commands must be applied between legal commands (MRR/MRW/MPC, VREFCS, and VREFCA).
4. MRW commands must be issued to all mode registers that require non-default settings.
5. Default ODT tolerances are wider prior to ZQ calibration.
6. Prior to ZQcal completion (Tj), MPC commands will be multicycle as described in the MPC Command Timing section.

Table 8: Voltage Ramp Conditions

After	Application Conditions
Ta is reached	V_{PP} must be greater than V_{DD}

Notes: 1. Ta is the point when any power supply first reaches 300mV.
2. Voltage ramp conditions apply between Ta and power-off (controlled or uncontrolled).
3. Tb is the point at which all supply and reference voltages are within their defined ranges.
4. Power ramp duration (Tb-Ta) must not exceed ^{t}INIT0.

Power-up Initialization Sequence

1. While applying power (after Ta), it is recommended that RESET_n be LOW (≤0.2 x V_{DDQ}) while all other inputs may be undefined. The device outputs remain disabled while RESET_n is held LOW. Power supply voltage ramp requirements are provided in the Input Voltage Power-up and Power-down Sequence section that follows. During power up and power down, |VDDQ-VDD| must be equal to or less than 200mV, and V_{PP} must always be equal to or greater than V_{DDQ}.
2. Following the completion of the voltage ramp (Tb), RESET_n must be maintained LOW. DQ, DQS_t, DQS_c, CS_n, CK_t, CK_c and CA input levels must be between V_{SS} and V_{DDQ} to avoid latch-up.
3. Beginning at Tb, RESET_n must be maintained LOW for a minimum of ^{t}INIT1 (Tb to Tc), after which RESET_n may be de-asserted to HIGH (Tc). At least ^{t}INIT2 (10ns) before RESET_n deassertion, CS_n must be set LOW. All other input signals are don't care. The device supports the ability for RESET_n to be held LOW indefinitely.
4. After RESET_n is de-asserted (Tc), wait at least ^{t}INIT3 before driving CS_n HIGH.
5. After CS_n deasserts HIGH (Td), wait a minimum of ^{t}INIT4 to allow the CS_n, CK and CA, DQ, and DQS ODT to go to the defined strap initial state (Te). Clock (CK_t, CK_c) is required to be started and stabilized for ^{t}CKSRX before exit of ^{t}INIT4 (Te). Upon the completion of (Te), all ODT states (CA, CS_n, CK, DQ and DQS ODT) should be valid. The CS receiver should no longer be in its CMOS-based mode. ODT termination states remain uncalibrated until completion of ZQcal at (Tj).
6. Upon (Te), NOP commands must be issued for a minimum of ^{t}INIT5 to conclude exit of initialization process and start ^{t}XPR timer at (Tf). The system must wait at least ^{t}XPR before issuing any legal configuration commands (Tg). During configuration, only MRR, MRW, MPC, VREFCS, and VREFCA commands are legal.
7. Between (Tg) and (Tj), the following initial configuration modes must be completed prior to other training modes:
   a) MPC for setting MR13 (^{t}CCD/^{t}DLLK/^{t}CCD_L_WR/^{t}CCD_L_WR2) must be issued before the MPC command to reset the DLL.
   b) MPC to execute DLL RESET must be issued before ZQCal Start.
   c) MPC to execute ZQCal Start and ZQCal Latch must be issued before any other training modes such as CS Training.
8. Between (Tj) and (Tz), any number of legal configuration commands are allowed. Training-based commands are optional and may be done at the system architect's discretion and may vary depending on the system, though proper setting of certain registers, such as those related to write leveling training, is required.
9. After (Tz), and the completion of any training or calibration timing parameters (^{t}ZQLAT) is satisfied, the device is ready for normal operation and is able to accept any valid command. Any additional mode registers that have not previously been set up for normal operation should be written at this time. If the host uses writeback suppression mode, it should be set after the initial write process to prevent aliasing to a 2-bit error.
10. After all mode registers have been programmed for normal operation, optional MBIST mode can be entered by writing MR23:OP[4] to HIGH, followed by subsequent MR24 PPR guard keys. The device then drives ALERT_N to LOW for a maximum of ^{t}SELFTEST time. The device drives ALERT_N to HIGH to indicate the operation is complete. After ALERT_N is driven HIGH, the device is immediately ready to receive valid commands. The MBIST/mPPR transparency status must subsequently

be checked in MR22:OP[2:0] to determine whether mPPR should be performed. See the MBIST/mPPR section for more detailed operation procedures.

Table 9: Initialization Timing Parameters

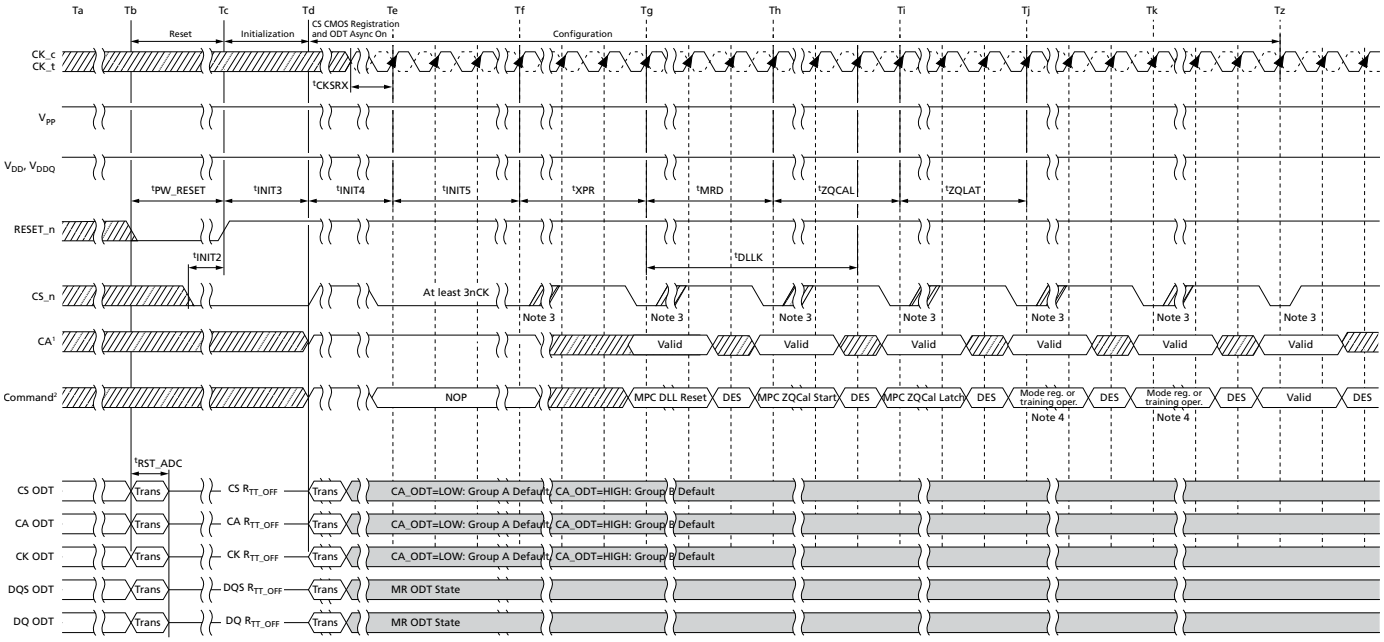
Parameter	Value		Unit	Comment
	MIN	MAX		
^{t}INIT0	–	20	ms	Maximum voltage ramp time
^{t}INIT1	200	–	µs	Minimum RESET_n LOW time after completion of voltage ramp
^{t}INIT2	10	–	ns	Minimum CS_n LOW time before RESET_n HIGH
^{t}INIT3	4	–	ms	Minimum CS_n LOW time after RESET_n HIGH
^{t}INIT4	2	–	µs	Minimum time for the device to register EXIT on CS with CMOS and assert the device default ODT values
^{t}INIT5	3	–	*n*CK	Minimum NOP cycles required after CS_n HIGH to exit RESET
^{t}XPR	^{t}XS	–	ns	Minimum time from exit RESET to first valid configuration command
^{t}CKSRX	See Self-Refresh Timing Table		–	Minimum stable clock time

Reset Initialization with Stable Power

The following sequence is required for RESET with no power interruption in order to provide proper initialization of the device as shown in the figure below.

1. Assert RESET_n below 0.2 x V_{DDQ} any time when reset is required. RESET_n must be maintained for a minimum time of ^{t}PW_RESET. CS_n must be held LOW at least ^{t}INIT2 before deasserting RESET_n.
2. Repeat steps 4 through 10 in the Power-up Initialization Sequence section.

Figure 3: Reset Procedure with Stable Power



Notes: 1. From time point (Td) until (Te), the command bus must be held HIGH.
2. From time point (Te) until (Tf), NOP commands must be applied on the command bus.
3. From time point (Tf) until (Tz), DES commands must be applied between legal commands (MRR, MRW, MPC, VREFCS, and VREFCA).
4. MRW commands must be issued to all mode registers that require defined settings.

Input Voltage Power-up and Power-down Sequence

Once V_{DD} and V_{DDQ} reach nominal operating conditions, $|V_{DDQ}-V_{DD}| < 66mV$.

Figure 4: Requirement for Voltage Ramp Control

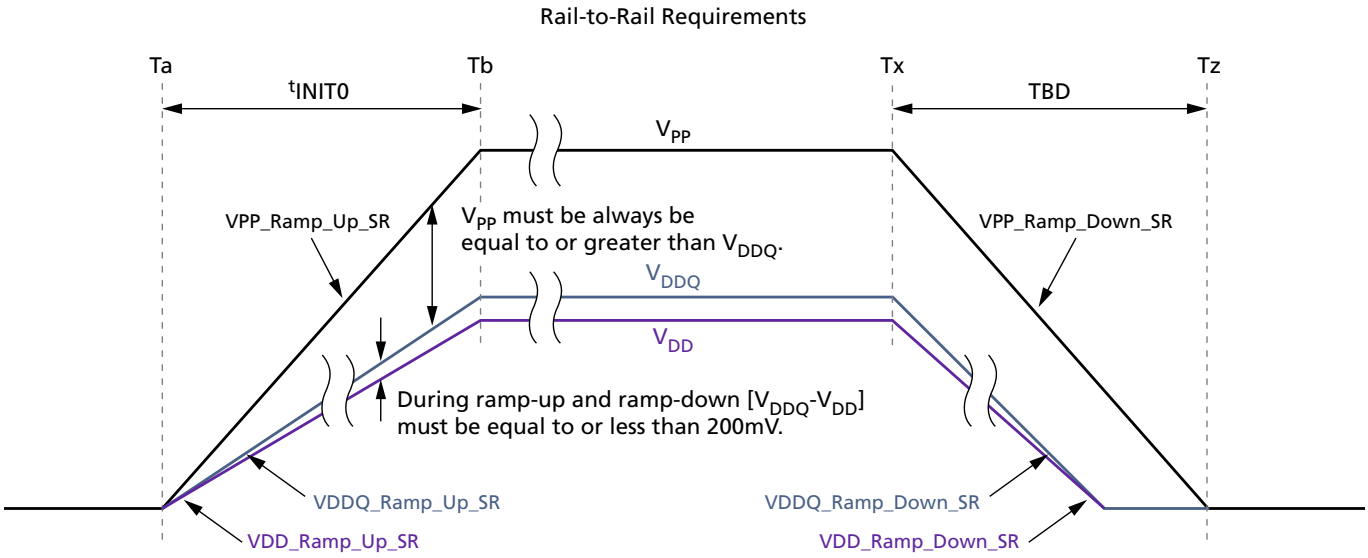


Table 10: Input Voltage Slew Rates

Description	Symbol	MIN	MAX	Units	Notes
V_{PP} Rail	VPP_Ramp_Up_SR	0.2	5	V/ms	1, 2, 3
	VPP_Ramp_Down_SR	0.1	4.5	V/ms	1, 2, 3
V_{DD} Rail	VDD_Ramp_Up_SR	0.1	4.5	V/ms	1, 2, 3
	VDD_Ramp_Down_SR	0.1	4.5	V/ms	1, 2, 3
V_{DDQ} Rail	VDDQ_Ramp_Up_SR	0.1	4.5	V/ms	1, 2, 3
	VDDQ_Ramp_Down_SR	0.1	4.5	V/ms	1, 2, 3

Notes: 1. All supply measurements made between 10% and 90% nominal voltage.
2. TBD bandwidth limited measurement.
3. After tINIT0, all supplies must be within their specified tolerance, as defined in the DC Operating tables.

Mode Registers

Note: Mode Register assignments (MRs and OP codes) for DDR5 are defined in this section and supersede any assignments found elsewhere in this document.

For application flexibility, various functions, features, and modes are programmable in up to 256 byte-wide mode registers. The mode registers are selectable by eight address bits (MRAs) provided as part of the MODE REGISTER WRITE (MRW) and MODE REGISTER READ (MRR) access commands.

The mode registers are divided into various fields depending on functionality and/or modes. As not all mode registers (MR#) have default values defined, contents of mode registers must be initialized and/or re-initialized (i. e., written) after power up and/or reset for proper operation. Additionally, the contents of the mode registers can be altered using the MRW command during normal operation.

When programming the mode registers, all address fields within the accessed mode register must be redefined when the MRW command is issued—even if only a subset of the MRW Op Code fields is modified. The MRW command does not directly affect array contents, which means this command can be executed any time after power-up without affecting the array contents.

MODE REGISTER READ

The MODE REGISTER READ (MRR) command reads configuration and status data from the device mode registers. The MRR command is initiated with CS_n and CA[13:0] in the proper state as defined by the Command Truth Table. The mode register address operands (MA[7:0]) enable selection of one of 256 registers. The mode register contents are available on the second 8 UIs of the burst and are repeated across all DQs after the CL following the MRR command. To avoid a potentially worst-case pattern, every odd DQ bit has its contents inverted (represented with an !). Data in the burst (UI 0-7) is either 0 or 1, with 1 indicating the content of the later UI's (UI 8-15) is inverted.

DQS is toggled for the duration of the MRR burst. The MRR has a command burst length of 16, regardless of the MR0 setting, the training mode, or the mode register address. MRR termination control and ODT timings are the same as for the READ command. The MRR operation must not be interrupted.

Non-target ODT encoding is available for MRR, similar to a normal READ operation. NT ODT MRR termination control and ODT timings are the same as for the READ NT command.

When Read CRC is enabled, the MRR output will come with BL18 (BL16 plus 2 CRC-bit), but the host has the option to consider the 17th and 18th bits don't care for MRR handling. Regardless if the host uses the 17th and 18th bits while Read CRC is enabled, the strobe toggles for BL18.

Figure 5: Mode Register Read Timing

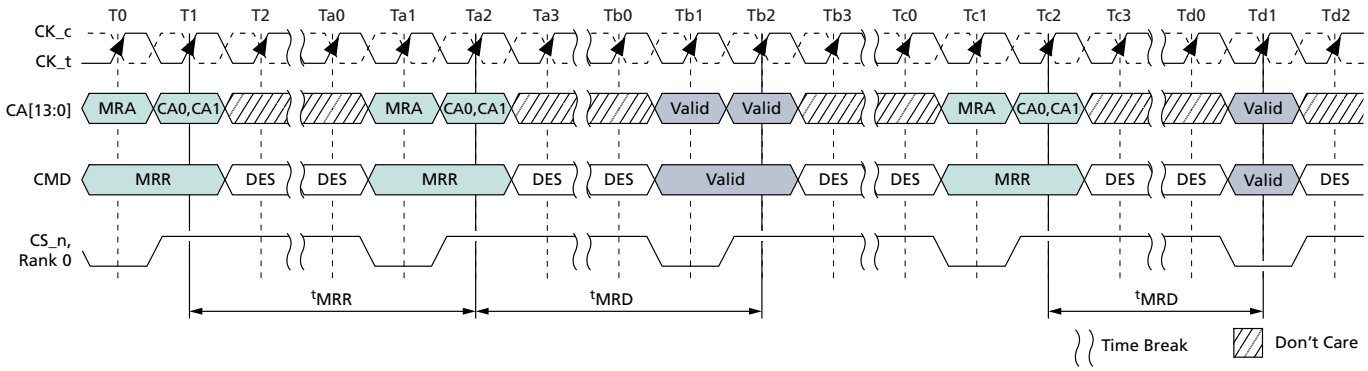


Table 11: DQ Output Mapping for x4 Devices

	UI								
	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

Notes: 1. The MRR's read preamble and postamble are the same as a normal READ command.

Table 12: DQ Output Mapping for x8 Devices

	UI								
	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

Notes: 1. The MRR's read preamble and postamble are the same as a normal READ command.

Table 13: DQ Output Mapping for x16 Devices (per-bit DFE, DCA and VREFDQ Registers Excluded)

	UI								
	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7

Table 13: DQ Output Mapping for x16 Devices (per-bit DFE, DCA and VREFDQ Registers Excluded)

	UI								
	0-7	8	9	10	11	12	13	14	15
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ8	Don't Care								
DQ9									
DQ10									
DQ11									
DQ12									
DQ13									
DQ14									
DQ15									

Notes: 1. The MRR's read preamble and postamble are the same as a normal READ command.
2. Mode register data output is only duplicated and inverted across the lower byte DQs of a x16 device. The host should treat the upper byte DQs as don't care values.
3. Output map excludes per-bit DFE, DCA, and VREFDQ mode registers (MR103–MR255).

Table 14: DQ Output Mapping for x16 Devices (MR46-47)

	UI								
	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ8	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ9	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ10	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ11	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ12	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ13	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ14	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ15	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

Notes: 1. The read preamble and postamble are the same as a normal READ command.

2. Output map excludes per-bit DFE, DCA, and VREFDQ mode registers (MR103–MR255).

Table 15: DQ Output Mapping for x16 Devices (per-bit DFE, DCA and VREFDQ Lower Byte – DQ[7:0], DML)

	UI								
	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ8	Don't Care								
DQ9									
DQ10									
DQ11									
DQ12									
DQ13									
DQ14									
DQ15									

Notes: 1. The MRR's read preamble and postamble are the same as a normal READ command.
2. Mode register data output is only duplicated and inverted across the lower byte DQs of a x16 device when reading from a per-bit DFE register associated with a lower byte DQ or DML. The host should treat the upper byte DQs as don't care values.
3. Output map is for per-bit DFE, DCA, and VREFDQ mode registers (MR103-MR255) only.

Table 16: DQ Output Mapping for x16 Devices (per-bit DFE, DCA and VREFDQ Upper Byte – DQ[15:8], DMU)

	UI								
	0-7	8	9	10	11	12	13	14	15
DQ0	Don't Care								
DQ1									
DQ2									
DQ3									
DQ4									
DQ5									
DQ6									
DQ7									
DQ8	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ9	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

Table 16: DQ Output Mapping for x16 Devices (per-bit DFE, DCA and VREFDQ Upper Byte – DQ[15:8], DMU)

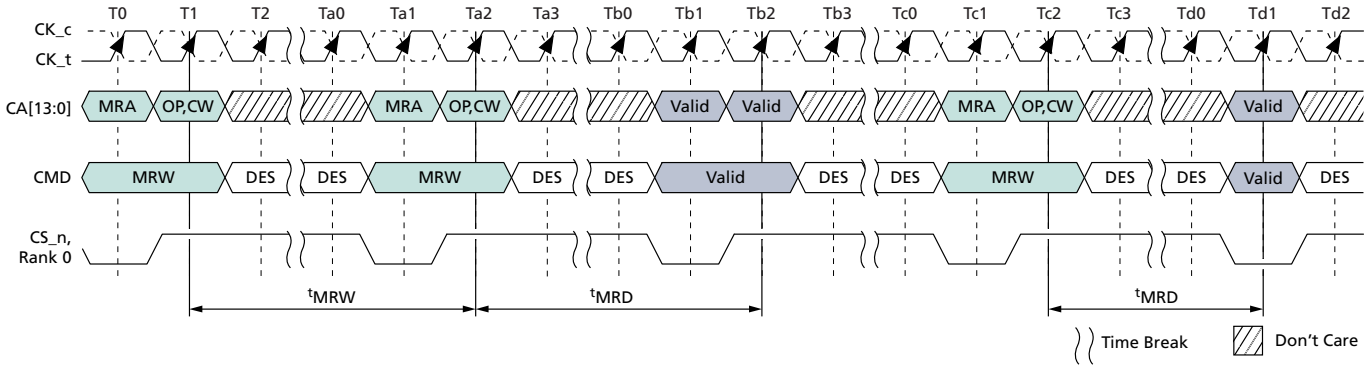
	UI								
	0-7	8	9	10	11	12	13	14	15
DQ10	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ11	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ12	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ13	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ14	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ15	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

Notes: 1. The MRR's read preamble and postamble are the same as a normal READ command.
2. Mode register data output is only duplicated and inverted across the upper byte DQs of a x16 device when reading from a per-bit DFE register associated with a upper byte DQ or DMU. The host should treat the lower byte DQs as don't care values.
3. Output map is for per-bit DFE, DCA, and VREFDQ mode registers (MR103-MR255) only.

MODE REGISTER WRITE

The MODE REGISTER WRITE (MRW) command writes configuration data to the device mode registers. The MRW command is initiated with CS and CA[13:0] in the proper state as defined by the Command Truth Table. The mode register address and the data written to the mode registers is contained in CA[13:0] according to the Command Truth Table. The MRW command period is defined by ^{t}MRW. Mode register writes to read-only registers have no impact on device functionality.

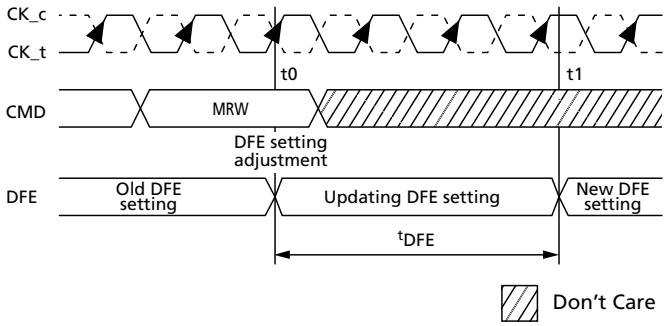
Figure 6: Mode Register Write Timing



DFE Mode Register Write Update Timing

This MR update timing parameter applies to all DFE mode registers. Mode registers for DFE include DFE Gain Bias, DFE Tap-1, DFE Tap-2, DFE Tap-3, DFE Tap-4.

Figure 7: DFE Update Setting



Mode Register Truth Tables and Timing Constraints

Table 17: MRR and MRW Truth Table

Current State	Command	Intermediate State	Next State
All banks idle	MRR	Mode Register Reading (all banks idle)	All banks idle
All banks idle	MRW	Mode Register Writing (all banks idle)	All banks idle

Table 18: MRR/MRW Timing Constraints: DQ ODT Enabled/Disabled

From Command	To Command	Minimum Delay Between From Command and To Command	Unit	Notes
MRR	MRR	^{t}MRR	–	2
	MRW	CL + BL/2 + 1	^{t}CK	2
	MPC	CL + BL/2 + 1	^{t}CK	2
	VREFCA	CL + BL/2 + 1	^{t}CK	2
	VREFCS	CL + BL/2 +1	^{t}CK	2
	Any other valid command	^{t}MRD	–	1,2
MRW	MRW	^{t}MRW	–	
	Any other valid command	^{t}MRD	–	
PRE	MRR	^{t}RP	–	
	MRW	^{t}RP	–	
REF	MRR	^{t}RFC	–	
	MRW	^{t}RFC	–	

Notes: 1. All data bursts in progress must be completed before entry into self refresh or power-down mode.
2. MRR can refer to both TARGET ODT MRR and NON-TARGET ODT MRR.

Mode Register Definitions

DDR5 devices support up to 8 mode register address (MRA) bits, each with a byte-wide payload, enabling up to 256 byte-wide registers.

The MRA and payload placed in op-codes (OP[7:0]) are all packeted in the command/address (CA[13:0]) bus encoding method. For more information, refer to the Command Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW) command protocols.

The DDR5 Mode Register Assignments table summarizes the mode registers for DDR5.

- The default state (at power-up or after reset) of each mode register (MR) bit is zero (0), except as listed in the Mode Registers with Non-Zero Default States Table in the RESET and Initialization Procedure section.
- A MODE REGISTER READ (MRR) command reads a mode register. A MODE REGISTER WRITE (MRW) command writes a mode register.
- Each bit in a register byte (MR#) is denoted as R if it can be read but not written, W if it can be written only, and R/W if it can be read and written. MR reads to write-only (W) registers always produce a zero (0) for those specific bits. Additionally, a DRAM read-only bit combined with a host write-only bit is denoted as a SR/W bit. This bit allows the DRAM to return a defined status during a read of that bit (SR = status read), independent of what the host may have written to the bit.
- Register locations shown as RFU (reserved for future use) have a value of zero (0) when read by MRR.
- A defined register byte (MR#) is any MR# that has at least one defined bit.
- If an entire MR# is marked RFU, it is considered undefined and all bits from the device are don't care for reads or writes. These undefined mode registers may not be supported in the device.
- When an MR# contains an RFU bit, the host must write a zero for those specific bits; programming any RFU bits may result in undefined operation.
- When the host issues an MRR to an MR# that contains RFU bits, those specific bits always produce a zero (0).
- In cases where a mode register is specific to a particular device configuration (x4 ,x8, x16) and/or density (8Gb, 16Gb, 32Gb), the following rules apply:
  - With a DRAM configured as a x4/x8 device, an entire MR# used only for a x16 device is considered RFU. These bits are don't care for reads and writes, and they may be unsupported.
  - When a bit field within a register is used by a different configuration or density than a given device, the host may write/read programmed values to these fields, but device operation will not be affected.

Table 19: DDR5 Mode Register Assignments

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
0	RFU	CAS Latency					Burst Length	
1	PDA Select ID				PDA Enumerate ID			
2	Internal Write Timing	Reserved	Device 15 MPSM	CS Assertion Duration (MPC)	Max Power Saving Mode (MPSM)	2N Mode	WL Training	Read Preamble Training
3	Write Leveling Internal Cycle Alignment – Upper Byte				Write Leveling Internal Cycle Alignment – Lower Byte			
4	TUF	RFU	Wide Range	Refresh ^{t}RFC Mode	Refresh Interval Rate Indicator	Refresh Rate		

Table 19: DDR5 Mode Register Assignments (Continued)

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
5	Pull-down Output Driver Impedance		DM Enable	TDQS Enable	PODTM Support	Pull-up Output Driver Impedance		Data Output Disable
6	^{t}RTP				Write Recovery Time			
7	RFU						(Optional) Write Leveling Internal + 0.5 ^{t}CK Alignment Offset - Upper Byte	(Optional) Write Leveling Internal + 0.5 ^{t}CK Alignment Offset - Lower Byte
8	Write Postamble Settings	Read Postamble Settings	RFU	Write Preamble Settings		Read Preamble Settings		
9	TM	RFU						
10	V_{REFDQ} Calibration Settings							
11	Valid	V_{REFCA} Calibration Settings						
12	Valid	V_{REFCS} Calibration Settings						
13	RFU				^{t}CCD_L/^{t}CCD_L_WR/^{t}CCD_L_WR2/^{t}DLLK			
14	ECS Mode	Reset ECS Counters	Row Mode/Code Word Mode	RFU	CID3	CID2	CID1	CID0
15	x4 Writes	ECS Write-back	RFU		Automatic ECS in Self Refresh	Transparency – ECS Threshold per Gb of Memory Cells		
16	Transparency – Address of Row with Max Errors 1							
17	Transparency – Address of Row with Max Errors 2							
18	RFU	Transparency – Address of Row with Max Errors 3						
19	PASR	RFU	Transparency – Max Row Errors					
20	Transparency – Error Count of Rows or Code Words with Errors							
21	RFU							
22	RFU					MBIST/mPPR Transparency (optional)		
23	RFU			MBIST (optional)	mPPR (optional)	RFU	sPPR	hPPR
24	PPR Guard Key							
25	RFU				Continuous Burst Mode	LFSR1 Pattern Option	LFSR0 Pattern Option	Read Training Pattern Format
26	Read Training Pattern Data0/LFSR0 Seed							
27	Read Training Pattern Data1/LFSR1 Seed							
28	Read Training Pattern Invert DQL7:0 (DQ7:0)							

Table 19: DDR5 Mode Register Assignments (Continued)

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
29	Read Training Pattern Invert DQU7:0 (DQ15:8)							
30	LFSR Assignment DQL7/ DQU7	LFSR Assignment DQL6/ DQU6	LFSR Assignment DQL5/ DQU5	LFSR Assignment DQL4/ DQU4	LFSR Assignment DQL3/ DQU3	LFSR Assignment DQL2/ DQU2	LFSR Assignment DQL1/ DQU1	LFSR Assignment DQL0/ DQU0
31	Read Training Pattern Address							
32	RFU	CA_ODT Strap Value	CS ODT			CK ODT		
33	RFU		DQS_RTT_PARK			CA ODT		
34	RFU		RTT_WR			RTT_PARK		
35	RFU		RTT_NOM_RD			RTT_NOM_WR		
36	RFU					RTT_Loopback		
37	RFU		ODTLoff_WR_offset			ODTLon_WR_offset		
38	RFU		ODTLoff_WR_NT_offset			ODTLon_WR_NT_offset		
39	RFU		ODTLoff_RD_NT_offset			ODTLon_RD_NT_offset		
40	RFU					Read DQS offset timing		
41	RFU							
42	RFU				DCA Training Assist Mode		DCA Types Supported	
43	Sign Bit for OP[6:4]	DCA for IBCLK in 4-phase clocks			Sign Bit for OP[2:0]	DCA for single/two-phase clock(s) or QCKL in 4-phase clocks		
44	RFU				Sign Bit for QBCLK in 4-phase clocks	DCA for QBCLK in 4-phase clocks		
45	DQS Interval Timer Run Time							
46	DQS Oscillator Count – LSB							
47	DQS Oscillator Count – MSB							
48	Write Pattern Mode							
49	RFU							
50	RFU		Write CRC Auto-Disable Status	Write CRC Auto-Disable Enable	Write CRC Error Status	Write CRC Enable Upper Nibble	Write CRC Enable	Read CRC Enable
51	RFU	Write CRC Auto-Disable Threshold						
52	RFU	Write CRC Auto-Disable Window						
53	Loopback Output Mode	Loopback Select Phase		Loopback Output Select				
54	hPPR Resource BG1 Bank 3	hPPR Resource BG1 Bank 2	hPPR Resource BG1 Bank 1	hPPR Resource BG1 Bank 0	hPPR Resource BG0 Bank 3	hPPR Resource BG0 Bank 2	hPPR Resource BG0 Bank 1	hPPR Resource BG0 Bank 0

Table 19: DDR5 Mode Register Assignments (Continued)

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
55	hPPR Resource BG3 Bank 3	hPPR Resource BG3 Bank 2	hPPR Resource BG3 Bank 1	hPPR Resource BG3 Bank 0	hPPR Resource BG2 Bank 3	hPPR Resource BG2 Bank 2	hPPR Resource BG2 Bank 1	hPPR Resource BG2 Bank 0
56	hPPR Resource BG5 Bank 3	hPPR Resource BG5 Bank 2	hPPR Resource BG5 Bank 1	hPPR Resource BG5 Bank 0	hPPR Resource BG4 Bank 3	hPPR Resource BG4 Bank 2	hPPR Resource BG4 Bank 1	hPPR Resource BG4 Bank 0
57	hPPR Resource BG7 Bank 3	hPPR Resource BG7 Bank 2	hPPR Resource BG7 Bank 1	hPPR Resource BG7 Bank 0	hPPR Resource BG6 Bank 3	hPPR Resource BG6 Bank 2	hPPR Resource BG6 Bank 1	hPPR Resource BG6 Bank 0
58	RAAMMT[2:0]			RAAIMT[3:0]				RFM Required
59	RFM RAA Counter		ARFM	RFU				
60	PASR Segment Mask							
61	Reserved			Package Output Driver Test Mode				
62	Vendor Specified							
63	DRAM Scratch Pad							
64	Reserved for Paging Pointer							
65	Serial Number 1							
66	Serial Number 2							
67	Serial Number 3							
68	Serial Number 4							
69	Serial Number 5							
70–102	RFU							
103	DQSL_t IBCLK Sign	RFU	DQSL_t DCA for IBCLK		DQSL_t QCLK Sign	RFU	DQSL_t DCA for QCLK	
104	RFU				DQSL_t QBCLK Sign	RFU	DQSL_t DCA for QBCLK	
105	DQSL_c IBCLK Sign	RFU	DQSL_c DCA for IBCLK		DQSL_c QCLK Sign	RFU	DQSL_c DCA for QCLK	
106	RFU				DQSL_c QBCLK Sign	RFU	DQSL_c DCA for QBCLK	
107	DQSU_t IBCLK Sign	RFU	DQSU_t DCA for IBCLK		DQSU_t QCLK Sign	RFU	DQSU_t DCA for QCLK	
108	RFU				DQSU_t QBCLK Sign	RFU	DQSU_t DCA for QBCLK	
109	DQSU_c IBCLK Sign	RFU	DQSU_c DCA for IBCLK		DQSU_c QCLK Sign	RFU	DQSU_c DCA for QCLK	
110	RFU				DQSU_c QBCLK Sign	RFU	DQSU_c DCA for QBCLK	
111	RFU			Global DFE Tap-4 Enable	Global DFE Tap-3 Enable	Global DFE Tap-2 Enable	Global DFE Tap-1 Enable	Global DFE Gain Enable
112	RFU				DML DFE Gain Bias			

Table 19: DDR5 Mode Register Assignments (Continued)

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
113	DML DFE Tap-1 Bias							
114	DML DFE Tap-2 Bias							
115	DML DFE Tap-3 Bias							
116	DML DFE Tap-4 Bias							
117	RFU							
118	DML V_{REFDQ} Sign	DML V_{REFDQ} Offset			RFU			
119	RFU							
120	RFU				DMU DFE Gain Bias			
121	DMU DFE Tap-1 Bias							
122	DMU DFE Tap-2 Bias							
123	DMU DFE Tap-3 Bias							
124	DMU DFE Tap-4 Bias							
125	RFU							
126	DMU V_{REFDQ} Sign	DMU V_{REFDQ} Offset			RFU			
127	RFU							
128	RFU				DQL0 DFE Gain Bias			
129	DQL0 DFE Tap-1 Bias							
130	DQL0 DFE Tap-2 Bias							
131	DQL0 DFE Tap-3 Bias							
132	DQL0 DFE Tap-4 Bias							
133	DQL0 IBCLK Sign	RFU	DQL0 DCA for IBCLK		DQL0 QCLK Sign	RFU	DQL0 DCA for QCLK	
134	DQL0 V_{REFDQ} Sign	DQL0 V_{REFDQ} Offset			DQL0 QBCLK Sign	RFU	DQL0 DCA for QBCLK	
135	RFU							
136	RFU				DQL1 DFE Gain Bias			
137	DQL1 DFE Tap-1 Bias							
138	DQL1 DFE Tap-2 Bias							
139	DQL1 DFE Tap-3 Bias							
140	DQL1 DFE Tap-4 Bias							
141	DQL1 IBCLK Sign	RFU	DQL1 DCA for IBCLK		DQL1 QCLK Sign	RFU	DQL1 DCA for QCLK	
142	DQL1 V_{REFDQ} Sign	DQL1 V_{REFDQ} Offset			DQL1 QBCLK Sign	RFU	DQL1 DCA for QBCLK	
143	RFU							
144	RFU				DQL2 DFE Gain Bias			
145	DQL2 DFE Tap-1 Bias							

Table 19: DDR5 Mode Register Assignments (Continued)

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
146	DQL2 DFE Tap-2 Bias							
147	DQL2 DFE Tap-3 Bias							
148	DQL2 DFE Tap-4 Bias							
149	DQL2 IBCLK Sign	RFU	DQL2 DCA for IBCLK		DQL2 QCLK Sign	RFU	DQL2 DCA for QCLK	
150	DQL2 V_{REFDQ} Sign	DQL2 V_{REFDQ} Offset			DQL2 QBCLK Sign	RFU	DQL2 DCA for QBCLK	
151	RFU							
152	RFU				DQL3 DFE Gain Bias			
153	DQL3 DFE Tap-1 Bias							
154	DQL3 DFE Tap-2 Bias							
155	DQL3 DFE Tap-3 Bias							
156	DQL3 DFE Tap-4 Bias							
157	DQL3 IBCLK Sign	RFU	DQL3 DCA for IBCLK		DQL3 QCLK Sign	RFU	DQL3 DCA for QCLK	
158	DQL3 V_{REFDQ} Sign	DQL3 V_{REFDQ} Offset			DQL3 QBCLK Sign	RFU	DQL3 DCA for QBCLK	
159	RFU							
160	RFU				DQL4 DFE Gain Bias			
161	DQL4 DFE Tap-1 Bias							
162	DQL4 DFE Tap-2 Bias							
163	DQL4 DFE Tap-3 Bias							
164	DQL4 DFE Tap-4 Bias							
165	DQL4 IBCLK Sign	RFU	DQL4 DCA for IBCLK		DQL4 QCLK Sign	RFU	DQL4 DCA for QCLK	
166	DQL4 V_{REFDQ} Sign	DQL4 V_{REFDQ} Offset			DQL4 QBCLK Sign	RFU	DQL4 DCA for QBCLK	
167	RFU							
168	RFU				DQL5 DFE Gain Bias			
169	DQL5 DFE Tap-1 Bias							
170	DQL5 DFE Tap-2 Bias							
171	DQL5 DFE Tap-3 Bias							
172	DQL5 DFE Tap-4 Bias							
173	DQL5 IBCLK Sign	RFU	DQL5 DCA for IBCLK		DQL5 QCLK Sign	RFU	DQL5 DCA for QCLK	
174	DQL5 V_{REFDQ} Sign	DQL5 V_{REFDQ} Offset			DQL5 QBCLK Sign	RFU	DQL5 DCA for QBCLK	
175	RFU							
176	RFU				DQL6 DFE Gain Bias			

Table 19: DDR5 Mode Register Assignments (Continued)

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
177	DQL6 DFE Tap-1 Bias							
178	DQL6 DFE Tap-2 Bias							
179	DQL6 DFE Tap-3 Bias							
180	DQL6 DFE Tap-4 Bias							
181	DQL6 IBCLK Sign	RFU	DQL6 DCA for IBCLK		DQL6 QCLK Sign	RFU	DQL6 DCA for QCLK	
182	DQL6 V_{REFDQ} Sign	DQL6 V_{REFDQ} Offset			DQL6 QBCLK Sign	RFU	DQL6 DCA for QBCLK	
183	RFU							
184	RFU				DQL7 DFE Gain Bias			
185	DQL7 DFE Tap-1 Bias							
186	DQL7 DFE Tap-2 Bias							
187	DQL7 DFE Tap-3 Bias							
188	DQL7 DFE Tap-4 Bias							
189	DQL7 IBCLK Sign	RFU	DQL7 DCA for IBCLK		DQL7 QCLK Sign	RFU	DQL7 DCA for QCLK	
190	DQL7 V_{REFDQ} Sign	DQL7 V_{REFDQ} Offset			DQL7 QBCLK Sign	RFU	DQL7 DCA for QBCLK	
191	RFU							
192	RFU				DQU0 DFE Gain Bias			
193	DQU0 DFE Tap-1 Bias							
194	DQU0 DFE Tap-2 Bias							
195	DQU0 DFE Tap-3 Bias							
196	DQU0 DFE Tap-4 Bias							
197	DQU0 IBCLK Sign	RFU	DQU0 DCA for IBCLK		DQU0 QCLK Sign	RFU	DQU0 DCA for QCLK	
198	DQU0 V_{REFDQ} Sign	DQU0 V_{REFDQ} Offset			DQU0 QBCLK Sign	RFU	DQU0 DCA for QBCLK	
199	RFU							
200	RFU				DQU1 DFE Gain Bias			
201	DQU1 DFE Tap-1 Bias							
202	DQU1 DFE Tap-2 Bias							
203	DQU1 DFE Tap-3 Bias							
204	DQU1 DFE Tap-4 Bias							
205	DQU1 IBCLK Sign	RFU	DQU1 DCA for IBCLK		DQU1 QCLK Sign	RFU	DQU1 DCA for QCLK	
206	DQU1 V_{REFDQ} Sign	DQU1 V_{REFDQ} Offset			DQU1 QBCLK Sign	RFU	DQU1 DCA for QBCLK	
207	RFU							

Table 19: DDR5 Mode Register Assignments (Continued)

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
208	RFU				DQU2 DFE Gain Bias			
209	DQU2 DFE Tap-1 Bias							
210	DQU2 DFE Tap-2 Bias							
211	DQU2 DFE Tap-3 Bias							
212	DQU2 DFE Tap-4 Bias							
213	DQU2 IBCLK Sign	RFU	DQU2 DCA for IBCLK		DQU2 QCLK Sign	RFU	DQU2 DCA for QCLK	
214	DQU2 V_{REFDQ} Sign	DQU2 V_{REFDQ} Offset			DQU2 QBCLK Sign	RFU	DQU2 DCA for QBCLK	
215	RFU							
216	RFU				DQU3 DFE Gain Bias			
217	DQU3 DFE Tap-1 Bias							
218	DQU3 DFE Tap-2 Bias							
219	DQU3 DFE Tap-3 Bias							
220	DQU3 DFE Tap-4 Bias							
221	DQU3 IBCLK Sign	RFU	DQU3 DCA for IBCLK		DQU3 QCLK Sign	RFU	DQU3 DCA for QCLK	
222	DQU3 V_{REFDQ} Sign	DQU3 V_{REFDQ} Offset			DQU3 QBCLK Sign	RFU	DQU3 DCA for QBCLK	
223	RFU							
224	RFU				DQU4 DFE Gain Bias			
225	DQU4 DFE Tap-1 Bias							
226	DQU4 DFE Tap-2 Bias							
227	DQU4 DFE Tap-3 Bias							
228	DQU4 DFE Tap-4 Bias							
229	DQU4 IBCLK Sign	RFU	DQU4 DCA for IBCLK		DQU4 QCLK Sign	RFU	DQU4 DCA for QCLK	
230	DQU4 V_{REFDQ} Sign	DQU4 V_{REFDQ} Offset			DQU4 QBCLK Sign	RFU	DQU4 DCA for QBCLK	
231	RFU							
232	RFU				DQU5 DFE Gain Bias			
233	DQU5 DFE Tap-1 Bias							
234	DQU5 DFE Tap-2 Bias							
235	DQU5 DFE Tap-3 Bias							
236	DQU5 DFE Tap-4 Bias							
237	DQU5 IBCLK Sign	RFU	DQU5 DCA for IBCLK		DQU5 QCLK Sign	RFU	DQU5 DCA for QCLK	
238	DQU5 V_{REFDQ} Sign	DQU5 V_{REFDQ} Offset			DQU5 QBCLK Sign	RFU	DQU5 DCA for QBCLK	

Table 19: DDR5 Mode Register Assignments (Continued)

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
239	RFU							
240	RFU				DQU6 DFE Gain Bias			
241	DQU6 DFE Tap-1 Bias							
242	DQU6 DFE Tap-2 Bias							
243	DQU6 DFE Tap-3 Bias							
244	DQU6 DFE Tap-4 Bias							
245	DQU6 IBCLK Sign	RFU	DQU6 DCA for IBCLK		DQU6 QCLK Sign	RFU	DQU6 DCA for QCLK	
246	DQU6 V_{REFDQ} Sign	DQU6 V_{REFDQ} Offset			DQU6 QBCLK Sign	RFU	DQU6 DCA for QBCLK	
247	RFU							
248	RFU				DQU7 DFE Gain Bias			
249	DQU7 DFE Tap-1 Bias							
250	DQU7 DFE Tap-2 Bias							
251	DQU7 DFE Tap-3 Bias							
252	DQU7 DFE Tap-4 Bias							
253	DQU7 IBCLK Sign	RFU	DQU7 DCA for IBCLK		DQU7 QCLK Sign	RFU	DQU7 DCA for QCLK	
254	DQU7 V_{REFDQ} Sign	DQU7 V_{REFDQ} Offset			DQU7 QBCLK Sign	RFU	DQU7 DCA for QBCLK	
255	RFU							

MR0–MR31

MR0 Burst Length, CAS Latency

Table 20: MR0 Register and OP-Code Bit Definitions (MA[7:0] = 00h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	CAS Latency					Burst Length	

Function	Type	OP	Description/Data	Notes
Burst Length	R/W	OP[1:0]	00=BL16, 01=BC8 OTF, 10=BL32, 11=BL32 OTF	
CAS Latency	R/W	OP[6:2]	00000=22, 00001=24, 00010=26, 00011=28, 00100=30, 00101=32, 00110=34, 00111=36, 01000=38, 01001=40, 01010=42, 01011=44, 01100=46, 01101=48, 01110=50, 01111=52, 10000=54, 10001=56, 10010=58, 10011=60, 10100=62, 10101=64, 10110=66, 10111-11111=RFU	1, 2
RFU	RFU	OP[7]	RFU	

Notes: 1. Range covers both monolithic and 3DS devices up to 6400.
2. CWL = CL-2.

MR1 PDA Mode Details

Table 21: MR1 Register and OP-Code Bit Definitions (MA[7:0] = 01h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PDA Select ID				PDA Enumerate ID			

Function	Type	OP	Description/Data	Notes
PDA Enumerate ID	R	OP[3:0]	This is a read-only MR field, which is only programmed through an MPC command with the PDA enumerate ID opcode. xxxxb encoding is set with MPC command with the PDA enumerate ID opcode. This can only be set when PDA enumerate programming mode is enabled and the associated DRAM's DQ0 is asserted LOW. The PDA enumerate ID opcode includes 4 bits for this encoding. The default setting is 1111b.	
PDA Select ID	R	OP[7:4]	This is a read-only MR field, which is only programmed through an MPC command with the PDA select ID opcode. xxxxb encoding is set with MPC command with the PDA select ID opcode. The PDA select ID opcode includes 4 bits for this encoding. 1111b = all DRAMs execute MRW, MPC, VREFCA, and VREFCS commands. For all other encodings, DRAMs execute MRW, MPC, VREFCS, and VREFCA commands only if PDA select ID[3:0] = PDA enumerate ID[3:0], with some exceptions for specific MPC commands that execute regardless of PDA select ID. The default setting is 1111b.	

MR2 Functional Modes

Table 22: MR2 Register and OP-Code Bit Definitions (MA[7:0] = 02h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Internal Write Timing	Reserved	Device 15 MPSM	CS Assertion Duration (MPC)	Max Power Saving Mode (MPSM)	2N Mode	Write Leveling Training	Read Preamble Training

Function	Type	OP	Description/Data	Notes
Read Preamble Enable	R/W	OP[0]	0=normal mode (default), 1=read preamble training	
Write Leveling Training	R/W	OP[1]	0=normal mode (default), 1=write leveling	1,2,3
2N Mode	R	OP[2]	0=2N mode (default), 1=1N mode	4
Max Power Saving Mode (MPSM)	R/W	OP[3]	0=disable (default), 1=enable	
CS Assertion Duration (MPC)	R/W	OP[4]	0=only multiple cycles of CS assertion available for MPC, VREFCA, and VREFCS commands (default), 1=only a single cycle of CS assertion available for MPC, VREFCA, and VREFCS commands.	
Device 15 MPSM	R/W	OP[5]	0=disable (default), 1=enable	
Reserved	Reserved	OP[6]	Reserved	
Internal Write Timing	R/W	OP[7]	0=disabled (default), 1=enabled	5,6

Notes: 1. To enter WL training mode, the MR field must be programmed to 1. WL training mode is used when internal write timing mode = 0 (external WL training) and when internal write timing mode = 1 (internal WL training).
2. To exit WL training mode, the MR field must be programmed to 0.
3. MRRs are not supported during write leveling.
4. This MR bit is programmed via an explicit MPC command only.
5. Internal write timing is disabled at the beginning of external write leveling mode and re-enabled at the start of write leveling internal cycle alignment. See the Write Leveling Training Mode section for details.
6. Device implementation may optionally have the same behavior when the internal Write timing mode is enabled instead of disabled. This means the CK and DQS timing paths remain matched internally. The WL internal cycle alignment mode setting must still support pulling the internal WL pulse earlier so that the same WL training flow produces the correct results.

MR3 Write Leveling Internal Cycle Alignment Settings

Table 23: MR3 Register and OP-Code Bit Definitions (MA[7:0] = 03h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Write Leveling Internal Cycle Alignment - Upper Byte				Write Leveling Internal Cycle Alignment - Lower Byte			

Function	Type	OP	Description/Data	Notes
Write Leveling Internal Cycle Alignment - Lower Byte	R/W	OP[3:0]	0000=0 ^{t}CK (default); 0001= -1 ^{t}CK; 0010= -2 ^{t}CK; 0011= -3 ^{t}CK; 0100= -4 ^{t}CK; 0101= -5 ^{t}CK; 0110= -6 ^{t}CK; (optional opcodes: 0111b through 1111b) 0111= -7 ^{t}CK; 1000= -8 ^{t}CK; 1001= -9 ^{t}CK; 1010= -10 ^{t}CK; 1011= -11 ^{t}CK; 1100= -12 ^{t}CK; 1101= -13 ^{t}CK; 1110= -14 ^{t}CK; 1111= -15 ^{t}CK	1,2,3,5
Write Leveling Internal Cycle Alignment - Upper Byte	R/W	OP[7:4]	0000 = 0 ^{t}CK (default); 0001 = -1 ^{t}CK; 0010 = -2 ^{t}CK; 0011 = -3 ^{t}CK; 0100 = -4 ^{t}CK; 0101 = -5 ^{t}CK; 0110 = -6 ^{t}CK; (optional opcodes: 0111b through 1111b) 0111 = -7 ^{t}CK; 1000 = -8 ^{t}CK; 1001 = -9 ^{t}CK; 1010 = -10 ^{t}CK; 1011 = -11 ^{t}CK; 1100 = -12 ^{t}CK; 1101 = -13 ^{t}CK; 1110 = -14 ^{t}CK; 1111 = -15 ^{t}CK	1,2,4,5

Notes: 1. This is set during WL training, after the host DQS has been aligned to the ideal external WL timings. The internal write timing is enabled and the WL internal timing alignment is set to ensure the internal write enable aligns within ^{t}DQS2CK of the external WL trained location. When internal write timing is disabled, the WL internal cycle alignment setting does not change the behavior of the write timings.
2. Device implementation may optionally have the same behavior when the internal write timing is enabled instead of disabled. This would mean that the CK and DQS timing paths remain matched internally. The WL internal cycle alignment setting must still support pulling the internal WL pulse earlier so that the same WL training flow will produce the correct result.
3. Lower byte WL internal cycle alignment is intended for x4, x8 and x16 configurations.
4. Upper byte WL internal cycle alignment is intended for x16 configurations only. Although training of the lower and upper bytes is independent, contact the DRAM vendor regarding recommendations for setting the WICA values to the same offset.
5. Optional opcodes (0111b-1111b) may be needed for certain speed bins.

MR4 Refresh Settings

Table 24: MR4 Register and OP-Code Bit Definitions (MA[7:0] = 04h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	RFU	Wide Range (optional)	Refresh ^{t}RFC Mode	Refresh Interval Rate Indicator	Refresh Rate		

Function	Type	OP	Description/Data	Notes
Refresh Rate	R	OP[2:0]	If Wide Range is not supported (OP[5]=0): 000=RFU; 001=^{t}REFI x1 (1x Ref Rate), <80°C nominal; 010=^{t}REFI x1 (1x Ref Rate), 80-85°C nominal; 011=^{t}REFI /2 (2x Ref Rate), 85-90°C nominal; 100=^{t}REFI /2 (2x Ref Rate), 90-95°C nominal; 101=^{t}REFI /2 (2x Ref Rate), >95°C nominal; 110=RFU, 111=RFU If Wide Range is supported (OP[5]=1): 000=^{t}REFI x1 (1x Ref Rate), <75°C nominal; 001=^{t}REFI x1 (1x Ref Rate), 75-80°C nominal; 010=^{t}REFI x1 (1x Ref Rate), 80-85°C nominal; 011=^{t}REFI /2 (2x Ref Rate), 85-90°C nominal; 100=^{t}REFI /2 (2x Ref Rate), 90-95°C nominal; 101=^{t}REFI /2 (2x Ref Rate), 95-100°C nominal; 110=^{t}REFI /2 (2x Ref Rate), >100°C nominal; 111=RFU	1,2,3,4,5, 6,7,8
Refresh Interval Rate Indicator	SR/W	OP[3]	DRAM status read (SR): 0=not implemented, 1=implemented Host write (W): 0b=disabled (default); 1b=enabled	
Refresh ^{t}RFC Mode	R/W	OP[4]	0=normal (^{t}RFC1); 1=fine granularity refresh mode (^{t}RFC2)	
Wide Range (optional)	R	OP[5]	0=wide range is not supported; 1=wide range is supported	8
RFU	RFU	RFU	RFU	
TUF (Temperature Update Flag)	R	OP[7]	0=no change in OP[2:0] since last MR4 read (default); 1=change in OP[2:0] since last MR4 read	

Notes: 1. The minimum required refresh rate for each OP[2:0] setting applies to ^{t}REFI1 and ^{t}REFI2. OP[2:0] settings specify a nominal temperature range. The ranges defined by OP[2:0] are determined by temperature thresholds used by the system for proper operation.
2. When OP[5]=0, the four temperature thresholds are nominally at 80°C, 85°C, 90°C and 95°C. The <80°C threshold has no minimum value specified and the >95°C threshold has no maximum temperature value specified. When OP[5]=1, the six temperature thresholds are nominally at 75°C, 80°C, 85°C, 90°C, 95°C, and 100°C. The <75°C threshold has no minimum value specified and the >100°C threshold has no maximum temperature value specified.
3. DRAM vendors report all possible settings over the operating temperature range of the device. Each vendor guarantees their device will work at any temperature within the range when the system refresh interval follows these guidelines:
   —Threshold ≤85°C ^{t}REFI x1 (1x Ref Rate) or faster may be used
   —Threshold >85°C ^{t}REFI/2 (2x Ref Rate) or faster is required
4. The 2X refresh rate must be provided by the system before the device T_j has gone up by more than 2°C (temperature margin) since the first report out of OP[2:0]=011b. This condition is reset when OP[2:0] is equal to 010b.
5. The device may not operate properly when OP[2:0]=101b, if T_j has gone up by more than 2°C (temperature margin) since the first report out of OP[2:0]=101b. This condition is reset when OP[2:0] is equal to 100b. OP[2:0]=101b must be a temporary condition of the device, to be addressed by immediately reducing the T_j of the device by throttling its power, and/or the power of nearby devices.
6. OP[7] = 0 at power-up. OP[2:0] bits are valid after initialization sequence (Te).

7. See the Temperature Sensor section for information on the recommended frequency of reading MR4.
8. Support for wide range temperature sensing does not indicate the device may operate properly at temperature ranges above 95°C. Side effects may include loss of data integrity.
9. OP[3] for optional functionality; RFU is not supported by the device.

MR5 I/O Settings

Table 25: MR5 Register and OP-Code Bit Definitions (MA[7:0] = 05h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Pull-down Output Driver Impedance		DM Enable	TDQS Enable	Package Output Driver Test Mode Supported	Pull-up Output Driver Impedance		Data Output Disable

Function	Type	OP	Description/Data	Notes
Data Output Disable	W	OP[0]	0=normal (default), 1=outputs disabled	
Pull-up Output Driver Impedance	R/W	OP[2:1]	00=RZQ/7 (34 ohm), 01= RZQ/6 (40 ohm), 10=RZQ/5 (48 ohm), 11=RFU	
Package Output Driver Test Mode Supported	R	OP[3]	0=function not supported, 1=function supported	
TDQS Enable	R/W	OP[4]	0=disable (default), 1=enable	
DM Enable	R/W	OP[5]	0=disable (default), 1=enable	
Pull-down Output Driver Impedance	R/W	OP[7:6]	00=RZQ/7 (34 ohm), 01=RZQ/6 (40 ohm), 10=RZQ/5 (48 ohm), 11=RFU	

MR6 Write Recovery Time (^{t}WR) and Read to Precharge Time (^{t}RTP)

Table 26: MR6 Register and OP-Code Bit Definitions (MA[7:0] = 06h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Read to Precharge Time (^{t}RTP)				Write Recovery Time (^{t}WR)			

Function	Type	OP	Description/Data	Notes
Write Recovery Time	R/W	OP[3:0]	0000=48CK, 001=54CK, 0010=60CK, 0011=66CK, 0100=72CK, 0101=78CK, 0110=84CK, 0111=90CK, 1000=96CK, all others RFU	1
Read to Precharge Time	R/W	OP[7:4]	0000=12CK, 0001=14CK, 0010=15CK, 0011=17CK, 0100=18CK, 0101=20CK, 0110=21CK, 0111=23CK, 1000=24CK, all others RFU	2

Notes: 1. ^{t}WR (MIN) is defined in the Timing By Speed Bin tables. The host must operate with MR settings resulting in ^{t}CK * MR6:OP [3:0] ≥^{t}WR (MIN).
2. ^{t}RTP (MIN) is defined in the Timing By Speed Bin tables. The host must operate with MR settings resulting in ^{t}CK * MR6:OP [7:4] ≥^{t}RTP (MIN).
3. All *n*CK conversions require rounding algorithm considerations.

MR7 RFU

Table 27: MR7 Register and OP-Code Bit Definitions (MA[7:0] = 07h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU						Write Leveling Internal Upper Byte (optional)	Write Leveling Internal Lower Byte (optional)

Function	Type	OP	Description/Data	Notes
(Optional) Write Leveling Internal + 0.5 ^{t}CK Alignment Offset - Lower Byte	R/W	0	0b: disabled (default); 1b: 0.5 ^{t}CK	1,2
(Optional) Write Leveling Internal + 0.5 ^{t}CK Alignment Offset - Upper Byte	R/W	1	0b: disabled (default); 1b: 0.5 ^{t}CK	1,3
RFU	RFU	OP[7:0]	RFU	

Notes: 1. The WICA 0.5 ^{t}CK offset is a positive adjustment to the target WICA value. (Example: MR3:OP[3:0] = -3 ^{t}CK (0011b) and MR7:OP[0] = 1, WICA + WICAhalfCycle = -3 ^{t}CK + 0.5 ^{t}CK = -2.5 ^{t}CK)
2. Lower byte WL internal cycle alignment is intended for x4, x8, and x16 configurations.
3. Upper byte WL internal cycle alignment is intended for x16 configuration only. Although training of the lower and upper bytes is independent, contact the DRAM vendor regarding recommendations for setting the WICA values to the same offset.

MR8 Preamble/Postamble

Table 28: MR8 Register and OP-Code Bit Definitions (MA[7:0] = 08h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Write Postamble Settings	Read Postamble Settings	RFU	Write Preamble Settings		Read Preamble Settings		

Function	Type	OP	Description/Data	Notes
Read Preamble Settings	R/W	OP[2:0]	000=1^{t}CK - 10 pattern, 001=2^{t}CK - 0010 pattern, 010=2^{t}CK - 1110 pattern, 011=3^{t}CK - 000010 pattern, 100=4^{t}CK - 00001010 pattern, all other encodings RFU	1
Write Preamble Settings	R/W	OP[4:3]	00=reserved, 01=2^{t}CK - 0010 pattern (default), 10=3^{t}CK - 000010 pattern, 11=4^{t}CK - 00001010 pattern	
RFU	RFU	RFU	RFU	
Read Postamble Settings	R/W	OP[6]	0=0.5^{t}CK - 0 pattern, 1=1.5^{t}CK - 010 pattern	
Write Postamble Settings	R/W	OP[7]	0=0.5^{t}CK - 0 pattern, 1=1.5^{t}CK - 000 pattern	

Notes: 1. Refer to the Preamble section for details on read preamble modes and patterns.

MR9 Test Mode Enable

Table 29: MR9 Register and OP-Code Bit Definitions (MA[7:0] = 09h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Test Mode (TM)	RFU						

Function	Type	OP	Description/Data	Notes
RFU	RFU	OP[6:0]	RFU	
Test Mode (TM)	W	OP[7]	0=normal (default), 1=test mode	1

Note: 1.

MR10 V_{refDQ} Calibration Settings

Table 30: MR10 Register and OP-Code Bit Definitions (MA[7:0] = 0Ah)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
V_{refDQ} Cal Settings							

Function	Type	OP	Description/Data	Notes
V_{refDQ} Cal Value	R/W	OP[7:0]	000 0000 = 97.5% 000 0001 = 97.0%... 111 1100 = 35.5% 111 1101 = 35.0% All other encodings RFU	

Notes: 1. Default setting 00101101b (75% of V_{DDQ}).

MR11 V_{refCA} Calibration Settings (Read-Only)

Table 31: MR11 Register and OP-Code Bit Definitions (MA[7:0] = 0Bh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Valid	V_{refCA} Calibration Settings (read-only)						

Function	Type	OP	Description/Data	Notes
V_{refCA} Cal Value	R	OP[6:0]	000 0000 = 97.5% 000 0001 = 97.0%... 111 1100 = 35.5% 111 1101 = 35.0% All other encodings RFU	1,2,3
Valid	R	OP[7]	Valid (V)	

Notes: 1. Default setting 0101101b (75% of V_{DDQ}).
2. Because $V_{REF,CA}$ calibration setting has an explicit command (VREFCA command), it can only be programmed via that command; and therefore, its mode register is read-only.

3. Because the state of CA12 is used to differentiate the VREFCA vs. VREFCS command, VREFCA OP[7] should always be equal to 0; the MR11/12 OP[7] value is defined as valid.

MR12 V_{refCS} Calibration Settings (Read-Only)

Table 32: MR12 Register and OP-Code Bit Definitions (MA[7:0] = 0Bh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Valid	V_{refCS} Calibration Settings (read-only)						

Function	Type	OP	Description/Data	Notes
V_{refCS} Cal Value	R	OP[6:0]	000 0000 = 97.5% 000 0001 = 97.0%... 111 1100 = 35.5% 111 1101 = 35.0% All other encodings RFU	1,2,3
Valid	R	OP[7]	Valid	

Notes: 1. Default setting 0101101b (75% of V_{DDQ}).
2. Because $V_{REF,CS}$ calibration setting has an explicit command (VREFCS command), it can only be programmed via that command; and therefore, its mode register is read-only.
3. Because the state of CA12 is used to differentiate the VREFCA vs. VREFCS command, VREFCA OP[7] should always be equal to 0; the MR11/12 OP[7] value is defined as valid.

MR13 ^{t}CCD_L/^{t}CCD_L_WR/^{t}CCD_L_WR2/^{t}DLLK

Table 33: MR13 Register and OP-Code Bit Definitions (MA[7:0] = 0Ch)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				^{t}CCD_L/^{t}CCD_L_WR/^{t}CCD_L_WR2//^{t}DLLK			

Function	Type	OP	Description/Data	Notes
^{t}CCD_L ^{t}CCD_L_WR ^{t}CCD_L_WR2 ^{t}DLLK	R	OP[3:0]	See table below	1,2,3
RFU	RFU	OP[7:4]	RFU	

Notes: 1. The ^{t}CCD_L/^{t}CCD_L_WR/^{t}CCD_L_WR2/^{t}DLLK should be programmed according to the value defined in the AC parametric table per operating frequency.
2. The register type is R (read only) because MR13 is set by the CONFIGURE ^{t}DLLK/^{t}CCD_L_WR/^{t}CCD_L_WR2/^{t}CCD_L MPC command.
3. Data rate ranges align with Speed Bin Table definitions.

MR13 OP[3:0]	^{t}CCD_L MIN (nCK) ^{t}CCD_L_WR MIN (nCK) ^{t}CCD_L_WR2 MIN (nCK)	^{t}DDLK MIN (nCK)	Details
0000	8, 16, 32	1024	1980 MT/s ≤ data rate ≤ 2100 MT/s and 2933 MT/s ≤ data rate ≤3200 MT/s

MR13 OP[3:0]	tCCD_L MIN (nCK) tCCD_L_WR MIN (nCK) tCCD_L_WR2 MIN (nCK)	tDDLK MIN (nCK)	Details
0001	9, 18, 36	1024	3200 MT/s < data rate ≤3600 MT/s
0010	10, 20, 40	1280	3600 MT/s < data rate ≤4000 MT/s
0011	11, 22, 44	1280	4000 MT/s < data rate ≤4400 MT/s
0100	12, 24, 48	1536	4400 MT/s < data rate ≤4800 MT/s
0101	13, 26, 52	1536	4800 MT/s < data rate ≤5200 MT/s
0110	14, 28, 56	1792	5200 MT/s < data rate ≤5600 MT/s
0111	15, 30, 60	1792	5600 MT/s < data rate ≤6000 MT/s
1000	16, 32, 64	2048	6000 MT/s < data rate ≤6400 MT/s
1001	All other encodings reserved		
...			
1111			

MR14 Transparency — Error Check Scrub (ECS) Configuration

Table 34: MR14 Register and OP-Code Bit Definitions (MA[7:0] = 0Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
ECS Mode	ECS Reset Counters	Row Mode/Code Word Mode	RFU	ECS Error Register Index/MBIST Rank Select			

Function	Type	OP	Description/Data	Notes
ECS Error Register Index/MBIST Rank Select	R/W	OP[3:0]	CID[3:0]	1,2,3,4
RFU	RFU	OP[4]	RFU	
Row Mode/Code Word Mode	R/W	OP[5]	0=ECS counts rows with errors, 1=ECS counts code words with errors	1
ECS Reset Counters	W	OP[6]	0=normal (default), 1=reset ECS counters	1,4
ECS Mode	R/W	OP[7]	0=automatic ECS mode (default), 1=manual ECS mode	1,4

Notes: 1. OP[3:0] applies to CID[3:0] for 3DS devices and must be set to indicate in which slice in the 3DS stack the transparency data resides for MR14 through MR20 and MR22. On 3DS devices that support optional MBIST/mPPR prior to MBIST initialization via MR23:OP[4] followed by guard keys, MR14:OP[3:0] must be programmed according to the logical rank that is desired to perform MBIST.
2. CID[3:0] encoding is based on the stack height of the device and varies depending on the number of dice in the stack.
3. For monolithic devices, CID[3:0] should be set to 0.
4. ECS stands for Error Check Scrub operation.

MR15 Transparency — Transparency ECS Threshold and Automatic ECS in Self Refresh

Table 35: MR15 Register and OP-Code Bit Definitions (MA[7:0] = 0Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
x4 Writes	ECS Write-back	RFU		Automatic ECS in Self Refresh	ECS Error Threshold Count		

Function	Type	OP	Description/Data	Notes
ECS Error Threshold Count (ETC)	R/W	OP[2:0]	000=TBD, 001=TBD, 010=TBD, 011=256 (default), 100=1024, 101=4096, 110-110=RFU	1
Automatic ECS in Self Refresh	W	OP[3]	0=automatic ECS disabled in self refresh in manual ECS mode (default); 1=automatic ECS enabled in self refresh in manual ECS mode	2,3
RFU	RFU	OP[5:4]	RFU	
ECS Writeback	R/W	OP[6]	0=do not suppress writeback of data and ECC check bits (default); 1=suppress writeback of data and ECC check bits (optional)	
x4 Writes	R/W	OP[7]	0=do not suppress writeback of data during RMW (default); 1=suppress writeback of data during RMW (optional)	

Notes: 1. MR15 OP[3:0] applies to CID[3:0] for 3DS and must be set to indicate in which slice in the 3DS stack the transparency data resides for MR14 through MR20.
2. The device performs automatic ECS operation while in self refresh mode by either enabling MR15 OP[3]=1b (automatic ECS in self refresh enable) or disabling MR14 OP[7]=0b (automatic ECS mode enable).
3. If automatic ECS in self refresh is enabled, updated transparency mode registers cannot be controlled by the number of manual ECS operation MPC commands since the ECS counter is increased by both the manual ECS command and the auto ECS operation in self refresh mode.

MR16 Address of Row with Max Errors 1

Table 36: MR16 Register and OP-Code Bit Definitions (MA[7:0] = 10h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Transparency - Address of Row with Max Errors 1							

Function	Type	OP	Description/Data	Notes
Max Row Error Address R[7:0]	R	OP[7:0]	Contains 8 bits of the row address with the highest error count.	1

Notes: 1. MR14 OP[3:0] applies to CID[3:0] for 3DS and must be set to indicate in which slice in the 3DS stack the transparency data resides for MR14 through MR20.

MR17 Address of Row with Max Errors 2

Table 37: MR17 Register and OP-Code Bit Definitions (MA[7:0] = 11h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Transparency - Address of Row with Max Errors 2							

Function	Type	OP	Description/Data	Notes
Max Row Error Address R[15:8]	R	OP[7:0]	Contains 8 bits of the row address with the highest error count.	

Notes: 1. MR14 OP[3:0] applies to CID[3:0] for 3DS and must be set to indicate in which slice in the 3DS stack the transparency data resides for MR14 through MR20.

MR18 Address of Row with Max Errors 3

Table 38: MR18 Register and OP-Code Bit Definitions (MA[7:0] = 12h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	Transparency - Address of Row with Max Errors 3						

Function	Type	OP	Description/Data	Notes
Max Row Error Address BG[2:0],BA[1:0],R[17,16]	R	OP[7:0]	Contains 2 bits of the row address plus the Bank Group address and Bank Address with the highest error count.	
RFU	RFU	RFU	RFU	

Notes: 1. MR14 OP[3:0] applies to CID[3:0] for 3DS and must be set to indicate in which slice in the 3DS stack the transparency data resides for MR14 through MR20.

MR19 Max Row Errors/PASR

Table 39: MR19 Register and OP-Code Bit Definitions (MA[7:0] = 13h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PASR	RFU	Transparency - Max Row Error Count (REC)					

Function	Type	OP	Description/Data	Notes
Max Row Error Count (REC)	R	OP[5:0]	Contains number of errors within the row with the most errors.	1
RFU	RFU	OP[6]	RFU	
PASR	R	OP[7]	0=PASR not supported; 1=PASR supported	

Notes: 1. MR14 OP[3:0] applies to CID[3:0] for 3DS and must be set to indicate in which slice in the 3DS stack the transparency data resides for MR14 through MR20.

MR20 Error Count

Table 40: MR20 Register and OP-Code Bit Definitions (MA[7:0] = 14h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Error Count (EC) bits 7 to 0							

Function	Type	OP	Description/Data	Notes
Error Count (EC) bits 7 to 0	R	OP[7:0]	Contains the error count range data.	1

Notes: 1. MR14 OP[3:0] applies to CID[3:0] for 3DS and must be set to indicate in which slice in the 3DS stack the transparency data resides for MR14 through MR20.

MR21 RFU

Table 41: MR21 Register and OP-Code Bit Definitions (MA[7:0] = 15h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU							

Function	Type	OP	Description/Data	Notes
RFU	RFU	OP[7:0]	RFU	

MR22 MBIST/mPPR Transparency (Optional)

Table 42: MR22 Register and OP-Code Bit Definitions (MA[7:0] = 16h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU					MBIST/mPPR Transparency (optional)		

Function	Type	OP	Description/Data	Notes
MBIST/mPPR Transparency (optional)	R	OP[2:0]	000b: MBIST has not run since INIT or no fails remain after most recent run (default); 001 = Fails remain; 010 = Unrepairable fails remain; 011 = MBIST should be run again; 100-111 = Reserved	1
RFU	RFU	OP[7:3]	RFU	

Notes: 1. The host should track whether or not MBIST has run since INIT. If MBIST runs and no fails are found, this transparency state remains set to 000b.

MR23 MBIST/PPR Settings

Table 43: MR23 Register and OP-Code Bit Definitions (MA[7:0] = 17h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU			MBIST	mPPR	sPPR		hPPR

Function	Type	OP	Description/Data	Notes
hPPR	R/W	OP[0]	0=disable, 1=enable	1
sPPR	R/W	OP[1]	0=disable, 1=enable (see OP[2] definition with sPPR Undo/Lock implemented	
	SR/W	OP[2]	DRAM Status Read (SR): 0=not implemented; 1=sPPR undo/lock implemented Host Write (W) for OP[2:1]: 00=disabled (normal operation); 01=sPPR enabled; 10=sPPR undo enabled; 11=sPPR lock enabled	1
mPPR	W	OP[3]	0=disable; 1=enable (optional)	1
MBIST	SR/W	OP[4]	DRAM Status Read (SR): 0=no MBIST/mPPR support; 1=supports MBIST/mPPR (optional) Host Write: 0=MBIST disabled; 1=MBIST enabled	1,2
RFU	RFU	OP[7:5]	RFU	

Notes: 1. Only one of these op-code bits may be programmed by the host to 1 at any given time. If any one of these op-code bits are enabled, the remaining bits must be programmed to 0.
2. The device automatically writes to 0 when MBIST completes; therefore, the host is not required to program to 0 before performing MBIST again.

MR24 PPR Guard Key

Table 44: MR24 Register and OP-Code Bit Definitions (MA[7:0] = 18h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PPR Guard Key							

Function	Type	OP	Description/Data	Notes
PPR Guard Key	W	OP[7:0]	See the Post Package Repair (PPR) section for sequence	

MR25 Read Training Mode

Table 45: MR25 Register and OP-Code Bit Definitions (MA[7:0] = 19h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				Continuous Burst Mode	LFSR1 Pattern Option	LFSR0 Pattern Option	Read Training Pattern Format

Function	Type	OP	Description/Data	Notes
Read Training Pattern Format	R/W	OP[0]	0=serial, 1=LFSR	
LFSR0 Pattern Option	R/W	OP[1]	0=LFSR, 1=clock	
LFSR1 Pattern Option	R/W	OP[2]	0=LFSR, 1=clock	
Continuous Burst Mode	R/W	OP[3]	0=MRR command-based (default), 1=continuous burst option	
RFU	RFU	OP[7:4]	RFU	

MR26 Read Training Pattern Data0/LFSR0 Seed

Table 46: MR26 Register and OP-Code Bit Definitions (MA[7:0] = 1Ah)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Read Training Pattern Data0/LFSR0 Seed							

Function	Type	OP	Description/Data	Notes
Read Pattern/LFSR Seed UI0	R/W	OP[0]	UI<7:0> data for serial mode, LFSR0 seed for LFSR mode	1
Read Pattern/LFSR Seed UI1	R/W	OP[1]		
Read Pattern/LFSR Seed UI2	R/W	OP[2]		
Read Pattern/LFSR Seed UI3	R/W	OP[3]		
Read Pattern/LFSR Seed UI4	R/W	OP[4]		
Read Pattern/LFSR Seed UI5	R/W	OP[5]		
Read Pattern/LFSR Seed UI6	R/W	OP[6]		
Read Pattern/LFSR Seed UI7	R/W	OP[7]		

Notes: 1. Default = 0x5A

MR27 Read Training Pattern Data1/LFSR1 Seed

Table 47: MR27 Register and OP-Code Bit Definitions (MA[7:0] = 1Bh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Read Training Pattern Data1/LFSR1 Seed							

Function	Type	OP	Description/Data	Notes
Read Pattern/LFSR Seed UI8	R/W	OP[0]	UI<15:8> data for serial mode, LFSR1 seed for LFSR mode	1
Read Pattern/LFSR Seed UI9	R/W	OP[1]		
Read Pattern/LFSR Seed UI10	R/W	OP[2]		
Read Pattern/LFSR Seed UI11	R/W	OP[3]		
Read Pattern/LFSR Seed UI12	R/W	OP[4]		
Read Pattern/LFSR Seed UI13	R/W	OP[5]		
Read Pattern/LFSR Seed UI14	R/W	OP[6]		
Read Pattern/LFSR Seed UI15	R/W	OP[7]		

Notes: 1. Default = 0x3C

MR28 Read Training Pattern Invert Lower Byte DQs

Table 48: MR28 Register and OP-Code Bit Definitions (MA[7:0] = 1Ch)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Read Training Pattern Invert Lower Byte DQs							

Function	Type	OP	Description/Data	Notes
DQ invert (lower DQ bits)	R/W	OP[0]	DQL0 (DQ0): 0=normal, 1=invert	1
	R/W	OP[1]	DQL1 (DQ1): 0=normal, 1=invert	
	R/W	OP[2]	DQL2 (DQ2): 0=normal, 1=invert	
	R/W	OP[3]	DQL3 (DQ3): 0=normal, 1=invert	
	R/W	OP[4]	DQL4 (DQ4): 0=normal, 1=invert	
	R/W	OP[5]	DQL5 (DQ5): 0=normal, 1=invert	
	R/W	OP[6]	DQL6 (DQ6): 0=normal, 1=invert	
	R/W	OP[7]	DQL7 (DQ7): 0=normal, 1=invert	

Notes: 1. Default = 0x00

MR29 Read Training Pattern Invert Upper Byte DQs

Table 49: MR29 Register and OP-Code Bit Definitions (MA[7:0] = 1Dh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Read Training Pattern Invert Upper Byte DQs							

Function	Type	OP	Description/Data	Notes
DQ invert (upper DQ bits)	R/W	OP[0]	DQU0 (DQ8): 0=normal, 1=invert	1
	R/W	OP[1]	DQU1 (DQ9): 0=normal, 1=invert	
	R/W	OP[2]	DQU2 (DQ10): 0=normal, 1=invert	
	R/W	OP[3]	DQU3 (DQ11): 0=normal, 1=invert	
	R/W	OP[4]	DQU4 (DQ12): 0=normal, 1=invert	
	R/W	OP[5]	DQU5 (DQ13): 0=normal, 1=invert	
	R/W	OP[6]	DQU6 (DQ14): 0=normal, 1=invert	
	R/W	OP[7]	DQU7 (DQ15): 0=normal, 1=invert	

Notes: 1. Default = 0x00

MR30 Read LFSR Assignments

Table 50: MR30 Register and OP-Code Bit Definitions (MA[7:0] = 1Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Read LFSR Assignments							

Function	Type	OP	Description/Data	Notes
LFSR Assignment DQ0/DQ8 (DQL0/DQU0)	R/W	OP[0]	0 = read pattern data0/LFSR0, 1 = read pattern data1/LFSR1	1
LFSR Assignment DQ1/DQ9 (DQL1/DQU1)	R/W	OP[1]		
LFSR Assignment DQ2/DQ10 (DQL2/DQU2)	R/W	OP[2]		
LFSR Assignment DQ3/DQ11 (DQL3/DQU3)	R/W	OP[3]		
LFSR Assignment DQ4/DQ12 (DQL4/DQU4)	R/W	OP[4]		
LFSR Assignment DQ5/DQ13 (DQL5/DQU5)	R/W	OP[5]		
LFSR Assignment DQ6/DQ14 (DQL6/DQU6)	R/W	OP[6]		
LFSR Assignment DQ7/DQ15 (DQL7/DQU7)	R/W	OP[7]		

Notes: 1. Default = 0xFE

MR31 Read Training Pattern Address

Table 51: MR31 Register and OP-Code Bit Definitions (MA[7:0] = 1Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Read Training Pattern Address							

Function	Type	OP	Description/Data	Notes
Read Training Pattern Address	R	OP[7:0]	Reserved. No specific register fields are associated with this address. In response to the MRR to this address, the device sends the BL16 read training pattern. All 8 bits associated with this MR address are reserved.	

MR32–MR102

MR32 CK ODT, CS ODT, CA ODT Strap

Table 52: MR32 Register and OP-Code Bit Definitions (MA[7:0] = 20h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	CA_ODT Strap Value	CS ODT			CK ODT		

Function	Type	OP	Description/Data	Notes
CK ODT	R	OP[2:0]	000=RTT_OFF (disable), 001=R_{ZQ}/0.5 (480 ohm), 010=R_{ZQ}/1 (240 ohm), 011=RFU (120 ohm), 100=R_{ZQ}/3 (80 ohm), 101=R_{ZQ}/4 (60 ohm), 110=RFU, 111=R_{ZQ}/6 (40 ohm); Group A default =000, Group B default=111	1

Function	Type	OP	Description/Data	Notes
CS ODT	R	OP[5:3]	000=RTT_OFF (disable), 001=R_{ZQ}/0.5 (480 ohm), 010=R_{ZQ}/1 (240 ohm), 011=RFU (120 ohm), 100=R_{ZQ}/3 (80 ohm), 101=R_{ZQ}/4 (60 ohm), 110=RFU, 111=R_{ZQ}/6 (40 ohm); Group A default =000, Group B default=111	1
CA_ODT Strap Value	R	OP[6]	0=group A, 1=group B	2
RFU	RFU	OP[7]	RFU	

Notes: 1. This mode register is programmed via an explicit MPC command only.
2. Strapping for ODT on Command and Address. The device applies Group A settings if the CA_ODT pin is connected to V_{SS} and Group B settings if the CA_ODT pin is connected to V_{DD}. This MR is used to confirm the device's setting for that configuration.

MR33 CA ODT, DQS_RTT_PARK

Table 53: MR33 Register and OP-Code Bit Definitions (MA[7:0] = 21h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		DQS_RTT_PARK			CA ODT		

Function	Type	OP	Description/Data	Notes
CA ODT	R	OP[2:0]	000=RTT_OFF (default), 001=R_{ZQ}/0.5 (480 ohm), 010=R_{ZQ}/1 (240 ohm), 011=RFU (120 ohm), 100=R_{ZQ}/3 (80 ohm), 101=R_{ZQ}/4 (60 ohm), 110=RFU, 111=R_{ZQ}/6 (40 ohm); Group A default =000, Group B default=0x100	1
DQS_RTT_PARK	R	OP[5:3]	000=RTT_OFF (default), 001=R_{ZQ} (240 ohm), 010=R_{ZQ}/2 (120 ohm), 011=R_{ZQ}/3 (80 ohm), 100=R_{ZQ}/4 (60 ohm), 101=R_{ZQ}/5 (48 ohm), 110=R_{ZQ}/6 (40 ohm); 111=R_{ZQ}/7 (34 ohm)	1
RFU	RFU	OP[7:6]	RFU	

Notes: 1. This mode register is programmed via an explicit MPC command only.

MR34 RTT_PARK and RTT_WR

Table 54: MR34 Register and OP-Code Bit Definitions (MA[7:0] = 22h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		RTT_WR			RTT_PARK		

Function	Type	OP	Description/Data	Notes
RTT_PARK	R	OP[2:0]	000=RTT_OFF (default), 001=R_{ZQ}, 010=R_{ZQ}/2, 011=R_{ZQ}/3, 100=R_{ZQ}/4, 101 = R_{ZQ}/5, 110=R_{ZQ}/6 , 111= R_{ZQ}/7	1
RTT_WR	R/W	OP[5:3]	000=RTT_OFF, 001=R_{ZQ} (default), 010=R_{ZQ}/2, 011=R_{ZQ}/3, 100=R_{ZQ}/4, 101 = R_{ZQ}/5, 110=R_{ZQ}/6 , 111= R_{ZQ}/7	
RFU	RFU	OP[7:6]	RFU	

Notes: 1. This mode register is programmed via an explicit MPC command only.

MR35 RTT_NOM_WR and RTT_NOM_RD

Table 55: MR35 Register and OP-Code Bit Definitions (MA[7:0] = 23h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		RTT_NOM_RD			RTT_NOM_WR		

Function	Type	OP	Description/Data	Notes
RTT_NOM_WR	R/W	OP[2:0]	000=OFF, 001=R_{ZQ}, 010=R_{ZQ}/2, 011=R_{ZQ}/3 (default), 100=R_{ZQ}/4, 101=R_{ZQ}/5, 110=R_{ZQ}/6, 111=R_{ZQ}/7	
RTT_NOM_RD	R/W	OP[5:3]	000=OFF, 001=R_{ZQ}, 010=R_{ZQ}/2, 011=R_{ZQ}/3 (default), 100=R_{ZQ}/4, 101=R_{ZQ}/5, 110=R_{ZQ}/6, 111=R_{ZQ}/7	
RFU	RFU	OP[7:6]	RFU	

MR36 RTT_Loopback

Table 56: MR36 Register and OP-Code Bit Definitions (MA[7:0] = 24h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU					RTT_Loopback		

Function	Type	OP	Description/Data	Notes
RTT_Loopback	R/W	OP[2:0]	000=RTT_OFF (default), 001-100=RFU,101=R_{ZQ}/5 (48 ohm), 110-111=RFU	1
RFU	RFU	OP[7:3]	RFU	

Notes: 1. When Loopback is disabled, both LBDQS and LBDQ pins are either at Hi-Z or termination mode. When Loopback is enabled, it is in driver mode.

MR37 ODT Write Control Offset

Table 57: MR37 Register and OP-Code Bit Definitions (MA[7:0] = 25h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		ODTLoff_WR_Offset			ODTLon_WR_Offset		

Function	Type	OP	Description/Data	Notes
ODTLon_WR_Offset	R/W	OP[2:0]	000=RFU, 001=-4 clocks, 010=-3 clocks, 011=-2 clocks, 100=-1 clocks (default), 101=0 clocks, 110=+1 clock, 111=+2 clocks	
ODTLoff_WR_Offset	R/W	OP[5:3]	000=RFU, 001=+4 clocks, 010=+3 clocks, 011=+2 clocks, 100=+1 clocks, 101=0 clocks (default), 110=-1 clock, 111=-2 clocks	
RFU	RFU	OP[7:6]	RFU	

MR38 ODTL Write NT Control Offset

Table 58: MR38 Register and OP-Code Bit Definitions (MA[7:0] = 26h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		ODTLoff_WR_NT_Offset			ODTLon_WR_NT_Offset		

Function	Type	OP	Description/Data	Notes
ODTLon_WR_NT_Offset	R/W	OP[2:0]	000=RFU, 001=-4 clocks, 010=-3 clocks, 011=-2 clocks, 100=-1 clocks (default), 101=0 clocks, 110=+1 clock, 111=+2 clocks	
ODTLoff_WR_NT_Offset	R/W	OP[5:3]	000=RFU, 001=+4 clocks, 010=+3 clocks, 011=+2 clocks, 100=+1 clocks, 101=0 clocks (default), 110=-1 clock, 111=-2 clocks	
RFU	RFU	OP[7:6]	RFU	

MR39 ODT RD NT Control Offset

Table 59: MR39 Register and OP-Code Bit Definitions (MA[7:0] = 27h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		ODTLoff_RD_NT_Offset			ODTLon_RD_NT_Offset		

Function	Type	OP	Description/Data	Notes
ODTLon_RD_NT_Offset	R/W	OP[2:0]	000=RFU, 001=RFU, 010=-3 clocks, 011=-2 clocks, 100=-1 clocks (default), 101=0 clocks, 110=+1 clock, 111=RFU	
ODTLoff_RD_NT_Offset	R/W	OP[5:3]	000=RFU, 001=RFU, 010=+3 clocks, 011=+2 clocks, 100=+1 clocks, 101=0 clocks (default), 110=-1 clock, 111=RFU	
RFU	RFU	OP[7:6]	RFU	

MR40 Read DQS Offset Timing

Table 60: MR40 Register and OP-Code Bit Definitions (MA[7:0] = 28h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU					Read DQS Offset Timing		

Function	Type	OP	Description/Data	Notes
Read DQS Offset Timing	R/W	OP[2:0]	000=0 clocks (default), 001=1 clock, 010=2 clocks, 011=3 clocks, 100-111=RFU	1
RFU	RFU	OP[7:3]	RFU	

Notes: 1. When operating at low speed (CL ≤30), ^{t}RPRE + Read DQS offset ≥5 clocks cannot be supported.

MR41 RFU

Table 61: MR41 Register and OP-Code Bit Definitions (MA[7:0] = 29h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU							

Function	Type	OP	Description/Data	Notes
RFU	RFU	OP[7:0]	RFU	

MR42 DCA Types Supported

Table 62: MR42 Register and OP-Code Bit Definitions (MA[7:0] = 2Ah)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				DCA Training Assist Mode		DCA Types Supported	

Function	Type	OP	Description/Data	Notes
DCA Types Supported	R	OP[1:0]	00=device does not support DCA, 01=device supports DCA for single/two-phase internal clock(s), 10=device supports DCA for four-phase internal clocks, 11=RFU	
DCA Training Assist Mode	R/W	OP[3:2]	00=disable (default), 01=MRR (or Read) synchronized with IBCLK is blocked, 10=MRR (or Read) synchronized with ICLK is blocked, 11=RFU	1,2,3,4,5, 6
RFU	RFU	OP[7:4]	RFU	

Notes: 1. When "MRR (or Read) synchronized with IBCLK is blocked" is set by MR42 OP[3:2]=01b, DQs caused by MRR (or Read) synchronized with IBCLK are driven HIGH.
2. When "MRR (or Read) synchronized with ICLK is blocked" is set by MR42 OP[3:2]=10b, DQs caused by MRR (or Read) synchronized with ICLK are driven HIGH.
3. DQS_t/DQS_c output normal toggling waveforms meaning that DQS_t/DQS_c are not affected by the settings of DCA Assist Mode MR42 OP[3:2].
4. The CRC function is not supported during DCA Training Assist mode.
5. DCA Training Assist mode is only supported by DRAMs with DCAs that have 4-phase internal clocks.
6. If MR42: OP[3:2] is set to either 01b or 10b, odd-gap READ or odd-gap MODE REGISTER READ PATTERN commands should follow the ^{t}MRR timing specification.

MR43 DCA Settings 1

Table 63: MR43 Register and OP-Code Bit Definitions (MA[7:0] = 2Bh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Sign Bit for OP[6:4]	DCA for IBCLK in 4-phase clock			Sign Bit for OP[2:0]	DCA for single/2-phase clock(s) or QCLK in 4-phase clocks		

Function	Type	OP	Description/Data	Notes
DCA for single/2-phase clock(s) or QCLK in 4-phase clocks	W	OP[2:0]	000=DCA step +0 (default), 001=DCA step +1, 010=DCA step +2, 011=DCA step +3, 100=DCA step +4, 101=DCA step +5, 110=DCA step +6, 111=DCA step +7	1

Function	Type	OP	Description/Data	Notes
Sign Bit for OP[2:0]	W	OP[3]	0=positive offset (default), 1=negative offset	1
DCA for IBCLK in 4-phase clocks	W	OP[6:4]	000=DCA step +0 (default), 001=DCA step +1, 010=DCA step +2, 011=DCA step +3, 100=DCA step +4, 101=DCA step +5, 110=DCA step +6, 111=DCA step +7	2
Sign Bit for OP[6:4]	W	OP[7]	0=positive offset (default), 1=negative offset	2

Notes: 1. These settings can be applied only if MR42[1:0] = 01b or 10b.
2. These settings can be applied only if MR42[1:0] = 10b.

MR44 DCA Settings 2

Table 64: MR44 Register and OP-Code Bit Definitions (MA[7:0] = 2Ch)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				Sign Bit for QBCLK in 4-phase clocks	DCA for QBCLK in 4-phase clocks		

Function	Type	OP	Description/Data	Notes
DCA for QBCLK in 4-phase clocks	W	OP[2:0]	000=DCA step +0 (default), 001=DCA step +1, 010=DCA step +2, 011=DCA step +3, 100=DCA step +4, 101=DCA step +5, 110=DCA step +6, 111=DCA step +7	1
Sign Bit for QBCLK in 4-phase clocks	W	OP[3]	0=positive offset (default), 1=negative offset	1
RFU	RFU	OP[7:4]	RFU	

Notes: 1. These settings can be applied only if MR42[1:0] = 10b.

MR45 DQS Interval Control

Table 65: MR45 Register and OP-Code Bit Definitions (MA[7:0] = 2Dh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS Interval Timer Run Time							

Function	Type	OP	Description/Data	Notes
DQS Interval Timer Run Time	W	OP[7:0]	0000 0000: DQS interval timer stop via MPC command (default) 0000 0001: DQS timer stops at 16th clocks after timer start 0000 0010: DQS timer stops at 32nd clocks after timer start 0000 0011: DQS timer stops at 48th clocks after timer start 0000 0100: DQS timer stops at 64th clocks after timer start ---------- thru ---------- 0011 1111: DQS timer stops at (63X16)th clocks after timer start 01XX XXXX: DQS timer stops at 2048th clocks after timer start 10XX XXXX: DQS timer stops at 4096th clocks after timer start 11XX XXXX: DQS timer stops at 8192nd clocks after timer start	1,2

Notes: 1. MPC command with OP[7:0]=0000 0110b (STOP DQS INTERVAL OSCILLATOR) stops DQS interval timer in case of MR45:OP[7:0] = 00000000b.

2. MPC command with OP[7:0]=0000 0110b (STOP DQS INTERVAL OSCILLATOR) is illegal with non-zero values in MR45:OP[7:0].

MR46 DQS Interval Oscillator Count — LSB

Table 66: MR46 Register and OP-Code Bit Definitions (MA[7:0] = 2Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS Interval Osc Count - LSB							

Function	Type	OP	Description/Data	Notes
DQS Interval Osc Count - LSB	R	OP[7:0]	0-255 LSB	1,2,3

Notes: 1. MR46 reports the LSB bits of the DQS Oscillator count. The DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR46 and MR47 must be read (MRR) and combined to obtain the value of the DQS Oscillator count.
3. A new MPC (START DQS OSCILLATOR) should be issued to reset the contents of MR46/MR47.

MR47 DQS Interval Oscillator Count — MSB

Table 67: MR47 Register and OP-Code Bit Definitions (MA[7:0] = 2Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS Interval Osc Count - MSB							

Function	Type	OP	Description/Data	Notes
DQS Interval Osc Count - MSB	R	OP[7:0]	0-255 MSB	1,2,3

Notes: 1. MR47 reports the MSB bits of the DQS Oscillator count. The DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR46 and MR47 must be read (MRR) and combined to obtain the value of the DQS Oscillator count.
3. A new MPC (START DQS OSCILLATOR) should be issued to reset the contents of MR46/MR47.

MR48 Write Pattern Data

Table 68: MR48 Register and OP-Code Bit Definitions (MA[7:0] = 30h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Write Pattern DQ7/DQ15	Write Pattern DQ6/DQ14	Write Pattern DQ5/DQ13	Write Pattern DQ4/DQ12	Write Pattern DQ3/DQ11	Write Pattern DQ2/DQ10	Write Pattern DQ1/DQ9	Write Pattern DQ0/DQ8

Function	Type	OP	Description/Data	Notes
Write Pattern DQ0/DQ8 (DQL0/DQU0)	R/W	OP[0]	Data for DQ0/DQ8 (DQL0/DQU0)	1,2,3
Write Pattern DQ1/DQ9 (DQL1/DQU1)	R/W	OP[1]	Data for DQ1/DQ9 (DQL1/DQU1)	
Write Pattern DQ2/DQ10 (DQL2/DQU2)	R/W	OP[2]	Data for DQ2/DQ10 (DQL2/DQU2)	
Write Pattern DQ3/DQ11 (DQL3/DQU3)	R/W	OP[3]	Data for DQ3/DQ11 (DQL3/DQU3)	
Write Pattern DQ4/DQ12 (DQL4/DQU4)	R/W	OP[4]	Data for DQ4/DQ12 (DQL4/DQU4)	
Write Pattern DQ5/DQ13 (DQL5/DQU5)	R/W	OP[5]	Data for DQ5/DQ13 (DQL5/DQU5)	
Write Pattern DQ6/DQ14 (DQL6/DQU6)	R/W	OP[6]	Data for DQ6/DQ14 (DQL6/DQU6)	
Write Pattern DQ7/DQ15 (DQL7/DQU7)	R/W	OP[7]	Data for DQ7/DQ15 (DQL7/DQU7)	

Notes: 1. OP[7:0] can be independently programmed with either 0 or 1.
2. Default 0x00.
3. If CRC enabled, ALERT_n will not be issued from the device during Write Pattern mode.

MR49 RFU

Table 69: MR49 Register and OP-Code Bit Definitions (MA[7:0] = 31h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU							

Function	Type	OP	Description/Data	Notes
RFU	RFU	OP[7:0]	RFU	

MR50 CRC Settings

Table 70: MR50 Register and OP-Code Bit Definitions (MA[7:0] = 32h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		Write CRC Auto-Disable Status	Write CRC Auto-Disable Enable	Write CRC Error Status	Write CRC Enable Upper Nibble	Write CRC Enable Lower Nibble	Read CRC Enable

Function	Type	OP	Description/Data	Notes
Read CRC Enable	R/W	OP[0]	0=disable (default), 1=enable	
Write CRC Enable Lower Nibble	R/W	OP[1]	0=disable (default), 1=enable	1
Write CRC Enable Upper Nibble	R/W	OP[2]	0=disable (default), 1=enable	1

Function	Type	OP	Description/Data	Notes
Write CRC Error Status	R/W	OP[3]	0=clear, 1=error (MRW can only set to 0 (clear); it cannot set to 1 (error))	
Write CRC Auto-Disable Enable	R/W	OP[4]	0=disable (default), 1=enable	
Write CRC Auto-Disable Status	R/W	OP[5]	0=not triggered, 1= triggered (MRW can only set to 0 (not triggered); it cannot set to 1 (triggered))	
RFU	RFU	OP[7:6]	RFU	

Notes: 1. When at least one of the two write CRC enable bits is set to 1 in x8, the timing of Write CRC Enable mode is applied to the entire device (that is, both nibbles). When Write CRC is enabled in one nibble and disabled in the other nibble in x8, the device does not check CRC errors on the disabled nibble, and therefore, the ALERT_n signal and any internal status bit related to CRC error is not impacted by the disabled nibble.
2. The host will disable Write CRC, if enabled, prior to entering Write Leveling Training mode.

MR51 Write CRC Auto-Disable Threshold

Table 71: MR51 Register and OP-Code Bit Definitions (MA[7:0] = 33h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	Write CRC Auto-Disable Threshold						

Function	Type	OP	Description/Data	Notes
Write CRC Auto-Disable Threshold	R/W	OP[6:0]	0000000=0...1111111=127 OP[6:0] corresponds to threshold bits [:0]	
RFU	RFU	OP[7]	RFU	

MR52 Write CRC Auto-Disable Window

Table 72: MR52 Register and OP-Code Bit Definitions (MA[7:0] = 34h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	Write CRC Auto-Disable Window						

Function	Type	OP	Description/Data	Notes
Write CRC Auto-Disable Window	R/W	OP[6:0]	0000000=0, 1111111=127 OP[6:0] corresponds to threshold bits [:0]	
RFU	RFU	OP[7]	RFU	

MR53 Loopback

Table 73: MR53 Register and OP-Code Bit Definitions (MA[7:0] = 35h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Loopback Output Mode	Loopback Select Phase		Loopback Output Select				

Function	Type	OP	Description/Data	Notes
Loopback Output Select	R/W	OP[4:0]	00000=loopback disabled (default), 00001=loopback DM(L) (x8 and x16 only), 00010=loopback DMU (X16 only), 00011=vendor-specific, 00100=vendor-specific, 00101=RFU through 01111=RFU, 10000=loopback DQL0, 10001=loopback DQL1, 10010=loopback DQL2, 10011=loopback DQL3, 10100=loopback DQL4 (X8 and X16 only), 10101=loopback DQL5 (X8 and X16 only), 10110=loopback DQL6 (X8 and X16 only), 10111=loopback DQL7 (X8 and X16 only), 11000=loopback DQU0 (X16 only), 11001=loopback DQU1 (X16 only), 11010=loopback DQU2 (X16 only), 11011=loopback DQU3 (X16 only), 11100=loopback DQU4 (X16 only), 11101=loopback DQU5 (X16 only), 11110=loopback DQU6 (X16 only), 11111=loopback DQU7 (X16 only)	1,2
Loopback Select Phase	R/W	OP[6:5]	00=loopback select phase A, 01=loopback select phase B (4-way and 2-way interleave only), 10=loopback select phase C (4-way interleave only), 11=loopback select phase D (4-way interleave only)	3
Loopback Output Mode	R/W	OP[7]	0=normal output (Default), 1=write burst output	4

Notes: 1. When loopback is disabled, both LBDQS and LBDQ pins are either at Hi-Z or termination mode per MR36:OP[2:0]. Loopback termination default value is RTT_OFF.
2. When loopback is enabled, both LBDQS and LBDQ pins are in driver mode using default R_{ON} of 34 ohm.
3. Phase A through D determines which bit in the multiplexer is being selected for loopback output.
4. This configures the loopback output to either send data out every time the DQS toggles in normal output mode, or to send data out only when enabled by the WRITE command, so that only write burst data is sent out via loopback.

MR54 hPPR Resources 1

Table 74: MR54 Register and OP-Code Bit Definitions (MA[7:0] = 36h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
hPPR Resource BG1 Bank 3	hPPR Resource BG1 Bank 2	hPPR Resource BG1 Bank 1	hPPR Resource BG1 Bank 0	hPPR Resource BG0 Bank 3	hPPR Resource BG0 Bank 2	hPPR Resource BG0 Bank 1	hPPR Resource BG0 Bank 0

Function	Type	OP	Description/Data	Notes
hPPR Resource BG0 Bank 0	R	OP[0]	0=hPPR Resource not available, 1=hPPR Resource available	3
hPPR Resource BG0 Bank 1	R	OP[1]	0=hPPR Resource not available, 1=hPPR Resource available	3
hPPR Resource BG0 Bank 2	R	OP[2]	0=hPPR Resource not available, 1=hPPR Resource available	1,3
hPPR Resource BG0 Bank 3	R	OP[3]	0=hPPR Resource not available, 1=hPPR Resource available	1,3
hPPR Resource BG1 Bank 0	R	OP[4]	0=hPPR Resource not available, 1=hPPR Resource available	3
hPPR Resource BG1 Bank 1	R	OP[5]	0=hPPR Resource not available, 1=hPPR Resource available	3
hPPR Resource BG1 Bank 2	R	OP[6]	0=hPPR Resource not available, 1=hPPR Resource available	1,3
hPPR Resource BG1 Bank 3	R	OP[7]	0=hPPR Resource not available, 1=hPPR Resource available	1,3

Notes: 1. Not valid for 8Gb.
2. Not valid for x16 devices.
3. MR14:OP[3:0] applies to CID[3:0] for 3DS devices and must be configured to indicate which slice in the 3DS stack is referenced in the MR54-MR57 hPPR resource information.

MR55 hPPR Resources 2

Table 75: MR55 Register and OP-Code Bit Definitions (MA[7:0] = 37h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
hPPR Resource BG3 Bank 3	hPPR Resource BG3 Bank 2	hPPR Resource BG3 Bank 1	hPPR Resource BG3 Bank 0	hPPR Resource BG2 Bank 3	hPPR Resource BG2 Bank 2	hPPR Resource BG2 Bank 1	hPPR Resource BG2 Bank 0

Function	Type	OP	Description/Data	Notes
hPPR Resource BG2 Bank 0	R	OP[0]	0=hPPR Resource not available, 1=hPPR Resource available	3
hPPR Resource BG2 Bank 1	R	OP[1]	0=hPPR Resource not available, 1=hPPR Resource available	3
hPPR Resource BG2 Bank 2	R	OP[2]	0=hPPR Resource not available, 1=hPPR Resource available	1,3
hPPR Resource BG2 Bank 3	R	OP[3]	0=hPPR Resource not available, 1=hPPR Resource available	1,3
hPPR Resource BG3 Bank 0	R	OP[4]	0=hPPR Resource not available, 1=hPPR Resource available	3
hPPR Resource BG3 Bank 1	R	OP[5]	0=hPPR Resource not available, 1=hPPR Resource available	3
hPPR Resource BG3 Bank 2	R	OP[6]	0=hPPR Resource not available, 1=hPPR Resource available	1,3
hPPR Resource BG3 Bank 3	R	OP[7]	0=hPPR Resource not available, 1=hPPR Resource available	1,3

Notes: 1. Not valid for 8Gb.
2. Not valid for x16 devices.
3. MR14:OP[3:0] applies to CID[3:0] for 3DS devices and must be configured to indicate which slice in the 3DS stack is referenced in the MR54-MR57 hPPR resource information.

MR56 hPPR Resources 3

Table 76: MR56 Register and OP-Code Bit Definitions (MA[7:0] = 38h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
hPPR Resource BG5 Bank 3	hPPR Resource BG5 Bank 2	hPPR Resource BG5 Bank 1	hPPR Resource BG5 Bank 0	hPPR Resource BG4 Bank 3	hPPR Resource BG4 Bank 2	hPPR Resource BG4 Bank 1	hPPR Resource BG4 Bank 0

Function	Type	OP	Description/Data	Notes
hPPR Resource BG4 Bank 0	R	OP[0]	0=hPPR Resource not available, 1=hPPR Resource available	2,3
hPPR Resource BG4 Bank 1	R	OP[1]	0=hPPR Resource not available, 1=hPPR Resource available	2,3
hPPR Resource BG4 Bank 2	R	OP[2]	0=hPPR Resource not available, 1=hPPR Resource available	1,2,3
hPPR Resource BG4 Bank 3	R	OP[3]	0=hPPR Resource not available, 1=hPPR Resource available	1,2,3
hPPR Resource BG5 Bank 0	R	OP[4]	0=hPPR Resource not available, 1=hPPR Resource available	2,3
hPPR Resource BG5 Bank 1	R	OP[5]	0=hPPR Resource not available, 1=hPPR Resource available	2,3
hPPR Resource BG5 Bank 2	R	OP[6]	0=hPPR Resource not available, 1=hPPR Resource available	1,2,3
hPPR Resource BG5 Bank 3	R	OP[7]	0=hPPR Resource not available, 1=hPPR Resource available	1,2,3

Notes: 1. Not valid for 8Gb.
2. Not valid for x16 devices.
3. MR14:OP[3:0] applies to CID[3:0] for 3DS devices and must be configured to indicate which slice in the 3DS stack is referenced in the MR54-MR57 hPPR resource information.

MR57 hPPR Resources 4

Table 77: MR57 Register and OP-Code Bit Definitions (MA[7:0] = 39h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
hPPR Resource BG7 Bank 3	hPPR Resource BG7 Bank 2	hPPR Resource BG7 Bank 1	hPPR Resource BG7 Bank 0	hPPR Resource BG6 Bank 3	hPPR Resource BG6 Bank 2	hPPR Resource BG6 Bank 1	hPPR Resource BG6 Bank 0

Function	Type	OP	Description/Data	Notes
hPPR Resource BG6 Bank 0	R	OP[0]	0=hPPR Resource not available, 1=hPPR Resource available	2,3
hPPR Resource BG6 Bank 1	R	OP[1]	0=hPPR Resource not available, 1=hPPR Resource available	2,3
hPPR Resource BG6 Bank 2	R	OP[2]	0=hPPR Resource not available, 1=hPPR Resource available	1,2,3
hPPR Resource BG6 Bank 3	R	OP[3]	0=hPPR Resource not available, 1=hPPR Resource available	1,2,3
hPPR Resource BG7 Bank 0	R	OP[4]	0=hPPR Resource not available, 1=hPPR Resource available	2,3
hPPR Resource BG7 Bank 1	R	OP[5]	0=hPPR Resource not available, 1=hPPR Resource available	2,3
hPPR Resource BG7 Bank 2	R	OP[6]	0=hPPR Resource not available, 1=hPPR Resource available	1,2,3
hPPR Resource BG7 Bank 3	R	OP[7]	0=hPPR Resource not available, 1=hPPR Resource available	1,2,3

Notes: 1. Not valid for 8Gb.
2. Not valid for x16 devices.
3. MR14:OP[3:0] applies to CID[3:0] for 3DS devices and must be configured to indicate which slice in the 3DS stack is referenced in the MR54-MR57 hPPR resource information.

MR58 RFM Configuration

Table 78: MR58 Register and OP-Code Bit Definitions (MA[7:0] = 3Ah)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Rolling Accumulated ACT Maximum Management Threshold (RAAMMT)			Rolling Accumulated ACT Initial Management Threshold (RAAIMT)				RFM Required

Function	Type	OP	Description/Data	Notes
RFM Required	R	OP[0]	0=refresh management not required; 1=refresh management required	1,3
Rolling Accumulated ACT Initial Management Threshold (RAAIMT)	R	OP[4:1]	0000-0011=RFU (normal), RFU (FGR); 0100=32 (normal), 16 (FGR); 0101=40 (normal), 20 (FGR); ... 1001=72 (normal), 36 (FGR); 1010=80 (normal), 40 (FGR); 1011-1111=RFU (normal), RFU (FGR)	1,2
Rolling Accumulated ACT Maximum Management Threshold (RAAMMT)	R	OP[7:5]	000-010=RFU (normal), RFU (FGR); 011=3x (normal), 6x (FGR); 100=4x (normal), 8x (FGR); 101=5x (normal), 10x (FGR); 110=6x (normal), 12x (FGR); 111=RFU (normal), RFU (FGR)	1,2

Notes: 1. Refresh management settings are vendor-specific by the MR settings.
2. Only applicable if the refresh management required bit is set to 1 (MR58:OP[0] = 1) or ARFM is set to level A, B, or C.
3. Specific attempts to by-pass the on-die circuitry designed to protect data integrity may result in data disturb.

MR59 RFM RAA Counter

Table 79: MR59 Register and OP-Code Bit Definitions (MA[7:0] = 3Bh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RAA Counter Decrement per REF Command		Adaptive RFM (ARFM)		RFU			

Function	Type	OP	Description/Data	Notes
RFU	RFU	OP[3:0]	RFU	
Adaptive RFM (ARFM)	R/W	OP[5:4]	00b=default (RAAIMT, RAAMMT, RAADEC); 01b=level A (RAAIMT-A, RAAMMT-A, RAADEC-A); 10b=level B (RAAIMT-B, RAAMMT-B, RAADEC-B); 11b=level C (RAAIMT-C, RAAMMT-C, RAADEC-C)	1
RAA Counter Decrement per REF Command	R	OP[7:6]	00=RAAIMT, 01=RAAIMT*0.5, 10=RFU, 11=RFU	1,2

Notes: 1. Refresh management settings are vendor-specific by the MR settings.
2. Only applicable if the refresh management required bit is set to 1 (MR58:OP[0] = 1) or ARFM is set to level A, B, or C.

MR60 PASR Segment Mask

Table 80: MR60 Register and OP-Code Bit Definitions (MA[7:0] = 3Ch)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment 7 (000)	Segment 6 (000)	Segment 5 (000)	Segment 4 (000)	Segment 3 (000)	Segment 2 (000)	Segment 1 (000)	Segment 0 (000)

Function	Type	OP	Description/Data	Notes
Segment 0 (000)	W	OP[0]	0 = normal; 1 = masked	
Segment 1 (000)	W	OP[1]		
Segment 2 (000)	W	OP[2]		
Segment 3 (000)	W	OP[3]		
Segment 4 (000)	W	OP[4]		
Segment 5 (000)	W	OP[5]		
Segment 6 (000)	W	OP[6]		1
Segment 7 (000)	W	OP[7]		1

Notes: 1. Must be 0 for 24Gb devices.

MR61 Package Output Driver Test Mode

Table 81: MR61 Register and OP-Code Bit Definitions (MA[7:0] = 3Dh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RSVD			Package Output Driver Test Mode				

Function	Type	OP	Description/Data	Notes
Package Output Driver Test Mode	W	OP[4:0]	00000=package test disabled (default); 00001=package test DML; 00010=package test DMU (x16 only); 00011=RFU; 00100=RFU; 00101=RFU ... thru ... 01111=RFU; 10000=package test DQL0; 10001=package test DQL1; 10010=package test DQL2; 10011=package test DQL3; 10100=package test DQL4 (X8 and X16 only); 10101=package test DQL5 (x8 and x16 only); 10110=package test DQL6 (x8 and x16 only); 10111=package test DQL7 (x8 and x16 only); 11000=package test DQU0 (x16 only); 11001=package test DQU1 (x16 only); 11010=package test DQU2 (x16 only); 11011=package test DQU3 (x16 only); 11100=package test DQU4 (x16 only); 11101=package test DQU5 (x16 only); 11110=package test DQU6 (x16 only); 11111=package test DQU7 (x16 only)	
RSVD	W	OP[7:5]	Must be programmed to 000	

MR62 Vendor-Specified

Table 82: MR62 Register and OP-Code Bit Definitions (MA[7:0] = 3Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specified							

Function	Type	OP	Description/Data	Notes
Vendor-specified	R/W	OP[7:0]	Vendor-specified	

MR63 Scratch Pad

Table 83: MR63 Register and OP-Code Bit Definitions (MA[7:0] = 3Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DRAM Scratch Pad							

Function	Type	OP	Description/Data	Notes
DRAM Scratch Pad	R/W	OP[7:0]	Any value is valid.	1,2

Notes: 1. The contents of this register can be written via MRW and read via MRR but have no function in the device.
2. Details for this function can be found in the DDR5 RCD01 specification.

MR64 Reserved for Paging Pointer

Table 84: MR64 Register and OP-Code Bit Definitions (MA[7:0] = 3Gh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved for Paging Pointer							

Function	Type	OP	Description/Data	Notes
Reserved for Paging Pointer	R/W	OP[7:0]	Any value is valid.	

MR65 Serial Number 1

Table 85: MR65 Register and OP-Code Bit Definitions (MA[7:0] = 3Hh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Serial Number 1							

Function	Type	OP	Description/Data	Notes
Serial Number 1	R	OP[7:0]	Any value is valid.	

MR66 Serial Number 2

Table 86: MR66 Register and OP-Code Bit Definitions (MA[7:0] = 3Ih)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Serial Number 2							

Function	Type	OP	Description/Data	Notes
Serial Number 2	R	OP[7:0]	Any value is valid.	

MR67 Serial Number 3

Table 87: MR67 Register and OP-Code Bit Definitions (MA[7:0] = 3Jh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Serial Number 3							

Function	Type	OP	Description/Data	Notes
Serial Number 3	R	OP[7:0]	Any value is valid.	

MR68 Serial Number 4

Table 88: MR68 Register and OP-Code Bit Definitions (MA[7:0] = 3Kh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Serial Number 4							

Function	Type	OP	Description/Data	Notes
Serial Number 4	R	OP[7:0]	Any value is valid.	

MR69 Serial Number 5

Table 89: MR66 Register and OP-Code Bit Definitions (MA[7:0] = 3Lh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Serial Number 5							

Function	Type	OP	Description/Data	Notes
Serial Number 5	R	OP[7:0]	Any value is valid.	

MR70–102 RFU

Mode registers between M70 and MR102 are undefined.

Mode Register Definitions for Decision Feedback Equalization

The following mode registers are used to configure the Decision Feedback Equalization (DFE), Per Bit Duty Cycle Adjuster, and Per Bit VREFDQ feature. These mode registers (MA[7:0]=70-FFh) are organized in a way such that those used for programming DFE, DCA and VREFDQ configuration per DQ or DM are grouped together. For example:

DQL0 starts at MA[7:0]=80h,

DQL1 starts at MA[7:0]=88h,

...

DQU6 starts at MA[7:0]=F0h,

DQU7 starts at MA[7:0]=F8h

Looking further into the 8-bit binary encoding, MA[6:3] is defined as a direct mapping for DQL0 to DQU7. For example:

MA[7:0]=1000:0XXXb for DQ0,

MA[7:0]=1000:1XXXb for DQ1,

...

MA[7:0]=1111:0XXXb for DQU6

MA[7:0]=1111:1XXXb for DQU7

Additional notes for MR112–MR116:

1. Refer to the DDR5 DFE specification for information on step size, step size tolerance and range values.
2. The step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables.
3. The number of step size, step values and range are speed-dependent.

Table 90: Visual Representation of DFE, Per Bit DCA and Per Bit VREFDQ Mode Register Mapping

MRW Address, Binary	Function	MRW Address Bits [2:0]							
		000b	001b	010b	011b	100b	101b	110b	111b
0111 0XXX	DML	Gain	Tap1	Tap2	Tap3	Tap4	MR address space not currently used		
0111 1XXX	DMU								
1000 0XXX	DQL0								
1000 1XXX	DQL1								
1001 0XXX	DQL2								
1001 1XXX	DQL3								
1010 0XXX	DQL4								
1010 1XXX	DQL5								
1011 0XXX	DQL6								
1011 1XXX	DQL7								
1100 0XXX	DQU0								
1100 1XXX	DQU1								
1101 0XXX	DQU2								
1101 1XXX	DQU3								
1110 0XXX	DQU4								
1110 1XXX	DQU5								
1111 0XXX	DQU6								
1111 1XXX	DQU7								

MR103–MR255

MR103 DQSL_t DCA for IBCLK and QCLK

Table 91: MR103 Register and OP-Code Bit Definitions (MA[7:0] = 67h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQSL_t IBCLK sign	RFU	DQSL_t DCA for IBCLK		DQSL_ t QCLK sign	RFU	DQSL_t DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQSL_t DCA for QCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQSL_t QCLK sign	W	OP[3]	0=positive (default), 1=negative	1
DQSL_t DCA for IBCLK	W	OP[5:4]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[6]	RFU	
DQSL_t IBCLK sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR104 DQSL_t DCA for QBCLK

Table 92: MR104 Register and OP-Code Bit Definitions (MA[7:0] = 68h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				DQSL_t QBLCK sign	RFU	DQSL_t DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQSL_t DCA for QBCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQSL_t QBCLK sign	W	OP[3]	0=positive (default), 1=negative	
RFU	RFU	OP[7:4]	RFU	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR105 DQSL_c DCA fro IBCLK and QCLK

Table 93: MR105 Register and OP-Code Bit Definitions (MA[7:0] = 69h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQSL_c IBCLK sign	RFU	DQSL_c DCA for IBCLK		DQSL_c QCLK sign	RFU	DQSL_c DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQSL_c DCA for QCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQSL_c QCLK sign	W	OP[3]	0=positive (default), 1=negative	
DQSL_c DCA for IBCLK	W	OP[5:4]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[6]	RFU	
DQSL_c IBCLK sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR106 DQSL_c DCA for QBCLK

Table 94: MR106 Register and OP-Code Bit Definitions (MA[7:0] = 6Ah)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				DQSL_c QBCLK sign	RFU	DQSL_c DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQSL_c DCA for QBCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQSL_c QBCLK sign	W	OP[3]	0=positive (default), 1=negative	

Function	Type	OP	Description/Data	Notes
RFU	RFU	OP[7:4]	RFU	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR107 DQSU_t DCA for IBCLK and QCLK

Table 95: MR107 Register and OP-Code Bit Definitions (MA[7:0] = 6Bh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQSU_t IBCLK sign	RFU	DQSU_t DCA for IBCLK		DQSU_t QCLK sign	RFU	DQSU_t DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQSU_t DCA for QCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQSU_t QCLK sign	W	OP[3]	0=positive (default), 1=negative	1
DQSU_t DCA for IBCLK	W	OP[5:4]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[6]	RFU	
DQSU_t IBCLK sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR108 DQSU_t DCA for QBCLK

Table 96: MR108 Register and OP-Code Bit Definitions (MA[7:0] = 6Ch)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				DQSU_t QBCLK sign	RFU	DQSU_t DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQSU_t DCA for QBCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQSU_t QBCLK sign	W	OP[3]	0=positive (default), 1=negative	1
RFU	RFU	OP[7:4]	RFU	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR109 DQSU_c DCA for IBCLK and QCLK

Table 97: MR108 Register and OP-Code Bit Definitions (MA[7:0] = 6Dh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQSU_c IBCLK sign	RFU	DQSU_c DCA for IBCLK		DQSU_c QCLK sign	RFU	DQSU_c DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQSU_c DCA for QCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQSU_c QCLK sign	W	OP[3]	0=positive (default), 1=negative	1
DQSU_c DCA for IBCLK	W	OP[5:4]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	
RFU	RFU	OP[6]	RFU	
DQSU_c IBCK sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR110 DQSU_c DCA for QBCLK

Table 98: MR110 Register and OP-Code Bit Definitions (MA[7:0] = 6Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				DQSU_c QBCLK sign	RFU	DQSU_c DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQSU_c DCA for QBCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, step+3	1
RFU	RFU	OP[2]	RFU	
DQSU_c QBCLK sign	W	OP[3]	0=positive (default), 1=negative	
RFU	RFU	OP[7:4]	RFU	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR111 Global DFE Enable

Table 99: MR111 Register and OP-Code Bit Definitions (MA[7:0] = 6Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU			Global DFE Tap-4 Enable	Global DFE Tap-3 Enable	Global DFE Tap-2 Enable	Global DFE Tap-1 Enable	Global DFE Gain Enable

Function	Type	OP	Description/Data	Notes
Global DFE Gain Enable	R/W	OP[0]	0=DFE Gain Enable (default), 1=DFE Gain Disable	1
Global DFE Tap-1 Enable	R/W	OP[1]	0=DFE Tap-1 Enable (default), 1=DFE Tap-1 Disable	1
Global DFE Tap-2 Enable	R/W	OP[2]	0=DFE Tap-2 Enable (default), 1=DFE Tap-2 Disable	1
Global DFE Tap-3 Enable	R/W	OP[3]	0=DFE Tap-3 Enable (default), 1=DFE Tap-3 Disable	1
Global DFE Tap-4 Enable	R/W	OP[4]	0=DFE Tap-4 Enable (default), 1=DFE Tap-4 Disable	1
RFU	RFU	OP[7:5]	RFU	

Notes: 1. This bit applies to all DM and DQ pins.
2. Setting MR111: OP[4:0]=11111b disables the DFE.

MR112 DML DFE Gain Bias

The MR112 definition covers registers for DML, DMU, DQL[7:0], and DQU[7:0] for DFE Gain Bias. Additional MRs for DFE Gain Bias are positioned every 8 MRs (MR112, MR120, MR128, etc.) until all pins are covered.

Table 100: MR112 Register and OP-Code Bit Definitions (MA[7:0] = 70h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				Sign Bit Gain Bias	DFE Gain Bias		

Function	Type	OP	Description/Data	Notes
DFE Gain Bias	R/W	OP[2:0]	000: DFE Gain Bias step 0 (default), 001: DFE Gain Bias step 1, 010: DFE Gain Bias step 2, 011: DFE Gain Bias step 3, 100–111=RFU	1,2,3
Sign Bit Gain Bias	R/W	OP[3]	0: positive DFE Gain Bias (default), 1: negative DFE Gain Bias	
RFU	RFU	OP[7:4]	RFU	

Notes: 1. Refer to the DDR5 DFE specification for information on step size, step size tolerance and range values.
2. The step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables.
3. The number of step size, step values, and range are speed-dependent.
4. Setting all DFE gain bias bits (in MR112, MR120, MR128, ... MR248 OP[3:0]=0000b and MR113-MR116, MR121-MR124, MR129-MR132, ... MR249-MR152 OP[8:0]=00000000b) disables the DFE.

MR113 DML DFE Tap-1 Bias

The MR113 definition covers registers for DML, DMU, DQL[7:0], and DQU[7:0] for DFE Tap-1. Additional MRs for DFE Tap-1 settings are positioned every 8 MRs (MR113, MR121, MR129, etc.) until all pins are covered.

Table 101: MR113 Register and OP-Code Bit Definitions (MA[7:0] = 71h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Enable/ Disable DFE Tap 1 Bias	Sign Bit DFE Tap 1 Bias	DFE Tap 1 Bias					

Function	Type	OP	Description/Data	Notes
DFE Tap 1 Bias	R/W	OP[5:0]	000000=DFE Tap-1 Bias Step +0 (default), 000001=DFE Tap-1 Bias Step +1, 000010=DFE Tap-1 Bias Step +2, 000011=DFE Tap-1 Bias Step +3, 000100=DFE Tap-1 Bias Step +4, 000101=DFE Tap-1 Bias Step +5, ... 100101=DFE Tap-1 Bias Step +38, 100110=DFE Tap-1 Bias Step +39, 101000=DFE Tap-1 Bias Step +40, 101001-111111=RFU	
Sign Bit DFE Tap 1 Bias	R/W	OP[6]	0=positive DFE Tap-1 Bias (default), 1=negative DFE Tap-1 Bias	
Enable/Disable DFE Tap 1 Bias	R/W	OP[7]	0=DFE Tap-1 disable (default), 1=DFE Tap-1 enable	

Notes: 1. Refer to the DDR5 DFE specification for information on step size, step size tolerance and range values.

2. The step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables.
3. The number of step size, step values, and range are speed-dependent.
4. Setting all DFE gain bias bits (in MR112, MR120, MR128, ... MR248 OP[3:0]=0000b and MR113-MR116, MR121-MR124, MR129-MR132, ... MR249-MR152 OP[8:0]=00000000b) disables the DFE.

MR114 DML DFE Tap-2 Bias

The MR114 definition covers registers for DML, DMU, DQL[7:0], and DQU[7:0] for DFE Tap-2. Additional MRs for DFE Tap-2 settings are positioned every eight MRs (MR114, MR122, MR130, etc) until all pins are covered.

Table 102: MR114 Register and OP-Code Bit Definitions (MA[7:0] = 72h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Enable/ Disable DFE Tap 2 Bias	Sign Bit DFE Tap 2 Bias	DFE Tap 2 Bias					

Function	Type	OP	Description/Data	Notes
DFE Tap 2 Bias	R/W	OP[5:0]	000000=DFE Tap-2 Bias Step +0 (default), 000001=DFE Tap-2 Bias Step +1, 000010=DFE Tap-2 Bias Step +2, 000011=DFE Tap-2 Bias Step +3, 000100=DFE Tap-2 Bias Step +4, 000101=DFE Tap-2 Bias Step +5, ... 001011=DFE Tap-2 Bias Step +13, 001110=DFE Tap-2 Bias Step +14, 001111=DFE Tap-2 Bias Step +15, 0100000-111111=RFU	
Sign Bit DFE Tap 2 Bias	R/W	OP[6]	0=positive DFE Tap-2 Bias (default), 1=negative DFE Tap-2 Bias	
Enable/Disable DFE Tap 2 Bias	R/W	OP[7]	0=DFE Tap-2 disable (default), 1=DFE Tap-2 enable	

Notes: 1. Refer to the DDR5 DFE specification for information on step size, step size tolerance and range values.
2. The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables.
3. The number of step size, step values, and range are speed-dependent.
4. Setting all DFE gain bias bits (in MR112, MR120, MR128, ... MR248 OP[3:0]=0000b and MR113-MR116, MR121-MR124, MR129-MR132, ... MR249-MR152 OP[8:0]=00000000b) disables the DFE.

MR115 DML DFE Tap-3 Bias

The MR115 definition covers registers for DML, DMU, DQL[7:0], and DQU[7:0] for DFE Tap-3. Additional MRs for DFE TAP-3 settings are positioned every eight MRs (MR115, MR123, MR131, etc) until all pins are covered.

Table 103: MR115 Register and OP-Code Bit Definitions (MA[7:0] = 73h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Enable/ Disable DFE Tap 3 Bias	Sign Bit DFE Tap 3 Bias	DFE Tap 3 Bias					

Function	Type	OP	Description/Data	Notes
DFE Tap 3 Bias	R/W	OP[5:0]	000000=DFE Tap-3 Bias Step +0 (default), 000001=DFE Tap-3 Bias Step +1, 000010=DFE Tap-3 Bias Step +2, 000011=DFE Tap-3 Bias Step +3, 000100=DFE Tap-3 Bias Step +4, 000101=DFE Tap-3 Bias Step +5, ... 001010=DFE Tap-3 Bias Step +10, 001011=DFE Tap-3 Bias Step +11, 001100=DFE Tap-3 Bias Step +12, 001101-111111=RFU	1,2,3
Sign Bit DFE Tap 3 Bias	R/W	OP[6]	0=positive DFE Tap-3 Bias (default), 1=negative DFE Tap-3 Bias	
Enable/Disable DFE Tap 3 Bias	R/W	OP[7]	0=DFE Tap-3 disable (default), 1=DFE Tap-3 enable	

Notes: 1. Refer to the DDR5 DFE specification for information on step size, step size tolerance and range values.
2. The step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables.
3. The number of step size, step values, and range are speed-dependent.
4. Setting all DFE gain bias bits (in MR112, MR120, MR128, ... MR248 OP[3:0]=0000b and MR113-MR116, MR121-MR124, MR129-MR132, ... MR249-MR152 OP[8:0]=00000000b) disables the DFE.

MR116 DML DFE Tap-4 Bias

The MR116 definition covers registers for DML, DMU, DQL[7:0], and DQU[7:0] for DFE Tap-4. Additional MRs for DFE TAP-4 settings are positioned every eight MRs (MR116, MR124, MR132, etc) until all pins are covered.

Table 104: MR116 Register and OP-Code Bit Definitions (MA[7:0] = 74h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Enable/ Disable DFE Tap 4 Bias	Sign Bit DFE Tap 4 Bias	DFE Tap 4 Bias					

Function	Type	OP	Description/Data	Notes
DFE Tap 4 Bias	R/W	OP[5:0]	000000=DFE Tap-4 Bias Step +0 (default), 000001=DFE Tap-4 Bias Step +1, 000010=DFE Tap-4 Bias Step +2, 000011=DFE Tap-4 Bias Step +3, 000100=DFE Tap-4 Bias Step +4, 000101=DFE Tap-4 Bias Step +5, 000110=DFE Tap-4 Bias Step +6, 000111=DFE Tap-4 Bias Step +7, 001000=DFE Tap-4 Bias Step +8, 001001=DFE Tap-4 Bias Step+9, 001010-111111=RFU	1,2,3
Sign Bit DFE Tap 4 Bias	R/W	OP[6]	0=positive DFE Tap-4 Bias (default), 1=negative DFE Tap-4 Bias	
Enable/Disable DFE Tap 4 Bias	R/W	OP[7]	0=DFE Tap-4 disable (default), 1=DFE Tap-4 enable	

Notes: 1. Refer to the DFE specification for information on step size, step size tolerance and range values.
2. The step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables.
3. The number of step size, step values and range are speed-dependent.

MR118 DML V_{REFDQ} Offset

Table 105: MR118 Register and OP-Code Bit Definitions (MA[7:0] = 76h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DML V_{REFDQ} Sign	DML V_{REFDQ} Offset			RFU			

Function	Type	OP	Description/Data	Notes
RFU	RFU	OP[3:0]	RFU	
DML V_{REFDQ} Offset	W	OP[6:4]	00=disable (default), 001=step+1, 010=step+2, 011=step+3, 100-111=RFU	1
DML V_{REFDQ} sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR126 DMU V_{REFDQ} Offset

Table 106: MR126 Register and OP-Code Bit Definitions (MA[7:0] = 7Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DMU V_{REFDQ} Sign	DMU V_{REFDQ} Offset			RFU			

Function	Type	OP	Description/Data	Notes
RFU	RFU	OP[3:0]	RFU	
DMU V_{REFDQ} Offset	W	OP[6:4]	00=disable (default), 001=step+1, 010=step+2, 011=step+3, 100-111=RFU	1
DMU V_{REFDQ} sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR133 DQL0 DCA for IBCLK and QCLK

Table 107: MR133 Register and OP-Code Bit Definitions (MA[7:0] = 85h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL0 IBCLK Sign	RFU	DQL0 DCA for IBCLK		DQL0 QCLK Sign	RFU	DQL0 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQL0 DCA for QCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQL0 QCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQL0 DCA for IBCLK	W	OP[5:4]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[6]	RFU	

Function	Type	OP	Description/Data	Notes
DQL0 IBCLK Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR134 DQL0 DCA for QBCLK and DQL0 V_{REFDQ} Offset

Table 108: MR134 Register and OP-Code Bit Definitions (MA[7:0] = 86h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL0 V_{REFDQ} Sign	DQL0 V_{REFDQ} Offset			DQL0 QBCLK Sign	RFU	DQL0 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQL0 DCA for QBCLK	W	OP[1:0]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQL0 QBCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQL0 V_{REFDQ} Offset	W	OP[6:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
DQL0 V_{REFDQ} Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR141 DQL1 DCA for IBCLK and QCLK

Table 109: MR141 Register and OP-Code Bit Definitions (MA[7:0] = 8Dh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL1 IBCLK Sign	RFU	DQL1 DCA for IBCLK		DQL1 QCLK Sign	RFU	DQL1 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQL1 DCA for QCLK	W	OP[1:0]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQL1 QCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQL1 DCA for IBCLK	W	OP[5:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
RFU	RFU	OP[6]	RFU	
DQL1 IBCLK Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR142 DQL1 DCA for QBCLK and DQL1 V_{REFDQ} Offset

Table 110: MR142 Register and OP-Code Bit Definitions (MA[7:0] = 8Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL1 V_{REFDQ} Sign	DQL1 V_{REFDQ} Offset			DQL1 QBCLK Sign	RFU	DQL1 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQL1 DCA for QBCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQL1 QBCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQL1 V_{REFDQ} Offset	W	OP[6:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
DQL1 V_{REFDQ} Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR149 DQL2 DCA for IBCLK and QCLK

Table 111: MR149 Register and OP-Code Bit Definitions (MA[7:0] = 95h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL2 IBCLK Sign	RFU	DQL2 DCA for IBCLK		DQL2 QCLK Sign	RFU	DQL2 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQL2 DCA for QCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQL2 QCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQL2 DCA for IBCLK	W	OP[5:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
RFU	RFU	OP[6]	RFU	
DQL2 IBCLK Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR150 DQL2 DCA for QBCLK and DQL2 V_{REFDQ} Offset

Table 112: MR150 Register and OP-Code Bit Definitions (MA[7:0] = 96h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL2 V_{REFDQ} Sign	DQL2 V_{REFDQ} Offset			DQL2 QBCLK Sign	RFU	DQL2 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQL2 DCA for QBCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQL2 QBCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQL2 V_{REFDQ} Offset	W	OP[6:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
DQL2 V_{REFDQ} Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR157 DQL3 DCA for IBCLK and QCLK

Table 113: MR157 Register and OP-Code Bit Definitions (MA[7:0] = 9Dh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL3 IBCLK Sign	RFU	DQL3 DCA for IBCLK		DQL3 QCLK Sign	RFU	DQL3 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQL3 DCA for QCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQL3 QCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQL3 DCA for IBCLK	W	OP[5:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
RFU	RFU	OP[6]	RFU	
DQL3 IBCLK Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR158 DQL3 DCA for QBCLK and DQL3 V_{REFDQ} Offset

Table 114: MR158 Register and OP-Code Bit Definitions (MA[7:0] = 9Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL3 V_{REFDQ} Sign	DQL3 V_{REFDQ} Offset			DQL3 QBCLK Sign	RFU	DQL3 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQL3 DCA for QBCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQL3 QBCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQL3 V_{REFDQ} Offset	W	OP[6:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
DQL3 V_{REFDQ} Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR165 DQL4 DCA for IBCLK and QCLK

Table 115: MR165 Register and OP-Code Bit Definitions (MA[7:0] = A5h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL4 IBCLK Sign	RFU	DQL4 DCA for IBCLK		DQL4 QCLK Sign	RFU	DQL4 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQL4 DCA for QCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	

Function	Type	OP	Description/Data	Notes
DQL4 QCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQL4 DCA for IBCLK	W	OP[5:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
RFU	RFU	OP[6]	RFU	
DQL4 IBCLK Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR166 DQL4 DCA for QBCLK and DQL4 V_{REFDQ} Offset

Table 116: MR166 Register and OP-Code Bit Definitions (MA[7:0] = A6h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL4 V_{REFDQ} Sign	DQL4 V_{REFDQ} Offset			DQL4 QBCLK Sign	RFU	DQL4 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQL4 DCA for QBCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQL4 QBCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQL4 V_{REFDQ} Offset	W	OP[6:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
DQL4 V_{REFDQ} Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR173 DQL5 DCA for IBCLK and QCLK

Table 117: MR173 Register and OP-Code Bit Definitions (MA[7:0] = ADh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL5 IBCLK Sign	RFU	DQL5 DCA for IBCLK		DQL5 QCLK Sign	RFU	DQL5 DCA for QCKL	

Function	Type	OP	Description/Data	Notes
DQL5 DCA for QCKL	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQL5 QCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQL5 DCA for IBCLK	W	OP[5:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
RFU	RFU	OP[6]	RFU	
DQL5 IBCLK Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR174 DQL5 DCA for QBCLK and DQL5 V_{REFDQ} Offset

Table 118: MR174 Register and OP-Code Bit Definitions (MA[7:0] = AEh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL5 V_{REFDQ} Sign	DQL5 V_{REFDQ}Offset			DQL5 QBCLK Sign	RFU	DQL5 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQL5 DCA for QBCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQL5 QBCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQL5 V_{REFDQ}Offset	W	OP[6:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3, 100-111=RFU	1
DQL5 V_{REFDQ} Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR181 DQL6 DCA for IBCLK and QCLK

Table 119: MR181 Register and OP-Code Bit Definitions (MA[7:0] = B5h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL6 IBCLK Sign	RFU	DQL6 DCA for IBCLK		DQL6 QCLK Sign	RFU	DQL6 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQL6 DCA for QCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQL6 QCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQL6 DCA for IBCLK	W	OP[5:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
RFU	RFU	OP[6]	RFU	
DQL6 IBCLK Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR182 DQL6 DCA for QBCLK and DQL6 V_{REFDQ} Offset

Table 120: MR182 Register and OP-Code Bit Definitions (MA[7:0] = B6h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL6 V_{REFDQ} Sign	DQL6 V_{REFDQ}Offset			DQL6 QBCLK Sign	RFU	DQL6 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQL6 DCA for QBCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1

Function	Type	OP	Description/Data	Notes
RFU	RFU	OP[2]	RFU	
DQL6 QBCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQL6 V_{REFDQ}Offset	W	OP[6:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3, 100-111=RFU	1
DQL6 V_{REFDQ} Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR189 DQL7 DCA for IBCLK and QCLK

Table 121: MR189 Register and OP-Code Bit Definitions (MA[7:0] = BDh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL7 IBCLK Sign	RFU	DQL7 DCA for IBCLK		DQL7 QCLK Sign	RFU	DQL7 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQL7 DCA for QCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQL7 QCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQL7 DCA for IBCLK	W	OP[5:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
RFU	RFU	OP[6]	RFU	
DQL7 IBCLK Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR190 DQL7 DCA for QBCLK and DQL7 V_{REFDQ} Offset

Table 122: MR190 Register and OP-Code Bit Definitions (MA[7:0] = BEh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL7 V_{REFDQ} Sign	DQL7 V_{REFDQ} Offset			DQL7 QBCLK Sign	RFU	DQL7 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQL7 DCA for QBCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQL7 QBCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQL7 V_{REFDQ} Offset	W	OP[6:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3, 100-111=RFU	1
DQL7 V_{REFDQ} Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR197 DQU0 DCA for IBCLK and QCLK

Table 123: MR197 Register and OP-Code Bit Definitions (MA[7:0] = C5h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU0 IBCLK Sign	RFU	DQU0 DCA for IBCLK		DQU0 QCLK Sign	RFU	DQU0 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQU0 DCA for QCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQU0 QCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQU0 DCA for IBCLK	W	OP[5:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
RFU	RFU	OP[6]	RFU	
DQU0 IBCLK Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR198 DQU0 DCA for QBCLK and DQU0 V_{REFDQ} Offset

Table 124: MR198 Register and OP-Code Bit Definitions (MA[7:0] = C6h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU0 V_{REFDQ} Sign	DQU0 V_{REFDQ}Offset			DQU0 QBCLK Sign	RFU	DQU0 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQU0 DCA for QBCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQU0 QBCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQU0 V_{REFDQ}Offset	W	OP[6:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3, 100-111=RFU	1
DQU0 V_{REFDQ} Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR205 DQU1 DCA for IBCLK and QCLK

Table 125: MR205 Register and OP-Code Bit Definitions (MA[7:0] = CDh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU1 IBCLK Sign	RFU	DQU1 DCA for IBCLK		DQU1 QCLK Sign	RFU	DQU1 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQU1 DCA for QCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1

Function	Type	OP	Description/Data	Notes
RFU	RFU	OP[2]	RFU	
DQU1 QCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQU1 DCA for IBCLK	W	OP[5:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
RFU	RFU	OP[6]	RFU	
DQU1 IBCLK Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR206 DQU1 DCA for QBCLK and DQU1 V_{REFDQ} Offset

Table 126: MR206 Register and OP-Code Bit Definitions (MA[7:0] = CEh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU1 V_{REFDQ} Sign	DQU1 V_{REFDQ}Offset			DQU1 QBCLK Sign	RFU	DQU1 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQU1 DCA for QBCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQU1 QBCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQU1 V_{REFDQ}Offset	W	OP[6:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3, 100-111=RFU	1
DQU1 V_{REFDQ} Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR213 DQU2 DCA for IBCLK and QCLK

Table 127: MR213 Register and OP-Code Bit Definitions (MA[7:0] = D5h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU2 IBCLK Sign	RFU	DQU2 DCA for IBCLK		DQU2 QCLK Sign	RFU	DQU2 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQU2 DCA for QCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQU2 QCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQU2 DCA for IBCLK	W	OP[5:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
RFU	RFU	OP[6]	RFU	
DQU2 IBCLK Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR214 DQU2 DCA for QBCLK and DQU2 V_{REFDQ} Offset

Table 128: MR214 Register and OP-Code Bit Definitions (MA[7:0] = D6h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU2 V_{REFDQ} Sign	DQU2 V_{REFDQ}Offset			DQU2 QBCLK Sign	RFU	DQU2 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQU2 DCA for QBCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQU2 QBCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQU2 V_{REFDQ}Offset	W	OP[6:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3, 100-111=RFU	1
DQU2 V_{REFDQ} Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR221 DQU3 DCA for IBCLK and QCLK

Table 129: MR221 Register and OP-Code Bit Definitions (MA[7:0] = DDh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU3 IBCLK Sign	RFU	DQU3 DCA for IBCLK		DQU3 QCLK Sign	RFU	DQU3 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQU3 DCA for QCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQU3 QCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQU3 DCA for IBCLK	W	OP[5:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
RFU	RFU	OP[6]	RFU	
DQU3 IBCLK Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR222 DQU3 DCA for QBCLK and DQU3 V_{REFDQ} Offset

Table 130: MR222 Register and OP-Code Bit Definitions (MA[7:0] = DEh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU3 V_{REFDQ} Sign	DQU3 V_{REFDQ}Offset			DQU3 QBCLK Sign	RFU	DQU3 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQU3 DCA for QBCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1

Function	Type	OP	Description/Data	Notes
RFU	RFU	OP[2]	RFU	
DQU3 QBCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQU3 V_{REFDQ}Offset	W	OP[6:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3, 100-111=RFU	1
DQU3 V_{REFDQ} Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR229 DQU4 DCA for IBCLK and QCLK

Table 131: MR229 Register and OP-Code Bit Definitions (MA[7:0] = E5h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU4 IBCLK Sign	RFU	DQU4 DCA for IBCLK		DQU4 QCLK Sign	RFU	DQU4 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQU4 DCA for QCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQU4 QCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQU4 DCA for IBCLK	W	OP[5:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
RFU	RFU	OP[6]	RFU	
DQU4 IBCLK Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR230 DQU4 DCA for QBCLK and DQU4 V_{REFDQ} Offset

Table 132: MR230 Register and OP-Code Bit Definitions (MA[7:0] = E6h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU4 V_{REFDQ} Sign	DQU4 V_{REFDQ}Offset			DQU4 QBCLK Sign	RFU	DQU4 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQU4 DCA for QBCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQU4 QBCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQU4 V_{REFDQ}Offset	W	OP[6:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3, 100-111=RFU	1
DQU4 V_{REFDQ} Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR237 DQU5 DCA for IBCLK and QCLK

Table 133: MR237 Register and OP-Code Bit Definitions (MA[7:0] = EDh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU5 IBCLK Sign	RFU	DQU5 DCA for IBCLK		DQU5 QCLK Sign	RFU	DQU5 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQU5 DCA for QCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQU5 QCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQU5 DCA for IBCLK	W	OP[5:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
RFU	RFU	OP[6]	RFU	
DQU5 IBCLK Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR238 DQU5 DCA for QBCLK and DQU5 V_{REFDQ} Offset

Table 134: MR238 Register and OP-Code Bit Definitions (MA[7:0] = EEh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU5 V_{REFDQ} Sign	DQU5 V_{REFDQ}Offset			DQU5 QBCLK Sign	RFU	DQU5 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQU5 DCA for QBCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQU5 QBCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQU5 V_{REFDQ}Offset	W	OP[6:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3, 100-111=RFU	1
DQU5 V_{REFDQ} Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR245 DQU6 DCA for IBCLK and QCLK

Table 135: MR245 Register and OP-Code Bit Definitions (MA[7:0] = F5h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU6 IBCLK Sign	RFU	DQU6 DCA for IBCLK		DQU6 QCLK Sign	RFU	DQU6 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQU6 DCA for QCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1

Function	Type	OP	Description/Data	Notes
RFU	RFU	OP[2]	RFU	
DQU6 QCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQU6 DCA for IBCLK	W	OP[5:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
RFU	RFU	OP[6]	RFU	
DQU6 IBCLK Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR246 DQU6 DCA for QBCLK and DQU6 V_{REFDQ} Offset

Table 136: MR246 Register and OP-Code Bit Definitions (MA[7:0] = F6h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU6 V_{REFDQ} Sign	DQU6 V_{REFDQ}Offset			DQU6 QBCLK Sign	RFU	DQU6 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQU6 DCA for QBCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQU6 QBCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQU6 V_{REFDQ}Offset	W	OP[6:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3, 100-111=RFU	1
DQU6 V_{REFDQ} Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR253 DQU7 DCA for IBCLK and QCLK

Table 137: MR253 Register and OP-Code Bit Definitions (MA[7:0] = FDh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU7 IBCLK Sign	RFU	DQU7 DCA for IBCLK		DQU7 QCLK Sign	RFU	DQU7 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQU7 DCA for QCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQU7 QCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQU7 DCA for IBCLK	W	OP[5:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3	1
RFU	RFU	OP[6]	RFU	
DQU7 IBCLK Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR254 DQU7 DCA for QBCLK and DQU7 V_{REFDQ} Offset

Table 138: MR254 Register and OP-Code Bit Definitions (MA[7:0] = FEh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU7 V_{REFDQ} Sign	DQU7 V_{REFDQ}Offset			DQU7 QBCLK Sign	RFU	DQU7 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQU7 DCA for QBCLK	W	OP[1:0]	00=disable (default), 01=step+1, 10=step+2, 11=step+3	1
RFU	RFU	OP[2]	RFU	
DQU7 QBCLK Sign	W	OP[3]	0=positive (default), 1=negative	
DQU7 V_{REFDQ}Offset	W	OP[6:4]	00=disable (default), 01=step +1, 10=step+2, 11=step+3, 100-111=RFU	1
DQU7 V_{REFDQ} Sign	W	OP[7]	0=positive (default), 1=negative	

Notes: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

Command Description and Operation

In the following tables, V=valid logic level HIGH or LOW. X=don't care, in which case the signal may be left floating. BG=bank group address. BA=bank address. R=row address. C=column address. BL=burst length. MRA=mode register address. OP=op code. CID=chip ID. CW=control word. NT = non-target rank. RIR = refresh interval rate (if enabled, H state = 1X REF, L state = 2X REF).

Bank group addresses BG[2:0] and bank addresses BA[1:0] determine which bank is to be operated upon in a specific bank group.

CA10 is used as the auto precharge (AP) bit for the second cycle of several two-cycle commands, and is active LOW.

CA11 is used as the write partial (WR_P) bit for the second cycle of several two-cycle commands, and is active LOW.

CID[0:3] are used for die selection, up to 16 high stacked die.

- Light blue = commands
- Gray = bank and bank group pins
- Dark blue = target/non-target control pins

For command truth table bits such as BG2, BA1, R16, R17, C10, and CID[3:0], which are unused based on a device's density, configuration width, and stacking options, the CA decode is defined as VALID when in these unused states.

Table 139: Command Truth Table: Two-Cycle Commands

Function	Abv.	CS	CA Pins														Note
			CA 0	CA 1	CA 2	CA 3	CA 4	CA 5	CA 6	CA 7	CA 8	CA 9	CA 10	CA 11	CA 12	CA 13	
Activate	ACT	L	L	L	R0	R1	R2	R3	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	1,2, 12
		H	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	CID3/ R17	
Reserved	REXT	L	L	H	Reserved												
		H	Reserved														
RFU	RFU	L	H	L	L	L	L	V	V	V	V	V	V	V	V	V	
		H	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
RFU	RFU	L	H	L	L	L	H	V	V	V	V	V	V	V	V	V	
		H	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
Write Pattern (Zero)	WRP	L	H	L	L	H	L	H	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	1,3,4, 5,12
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V	AP=H	H	V	CID3	
Write Pattern w/Auto Pre-charge	WRPA	L	H	L	L	H	L	H	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	1,3,4, 5,12
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V	AP=L	H	V	CID3	
RFU	RFU	L	H	L	L	H	H	V	V	V	V	V	V	V	V	V	
		H	V	V	V	V	V	V	V	V	V	V	V	V	V	V	

Table 139: Command Truth Table: Two-Cycle Commands (Continued)

Function	Abv.	CS	CA Pins														Note
			CA 0	CA 1	CA 2	CA 3	CA 4	CA 5	CA 6	CA 7	CA 8	CA 9	CA 10	CA 11	CA 12	CA 13	
Mode Register Write	MRW	L	H	L	H	L	L	MRA 0	MRA 1	MRA 2	MRA 3	MRA 4	MRA 5	MRA 6	MRA 7	V	1,6
		H	OP 0	OP 1	OP 2	OP 3	OP 4	OP5	OP6	OP7	V	V	CW	V	V	V	
Mode Register Read	MRR	L	H	L	H	L	H	MRA 0	MRA 1	MRA 2	MRA 3	MRA 4	MRA 5	MRA 6	MRA 7	V	6,7, 13
		H	L	L	V	V	V	V	V	V	V	V	CW	V	V	V	
Mode Register Read **NT**	MRR-**NT**	L	H	L	H	L	H	V	V	V	V	V	V	V	V	V	7,14
		L	L	L	V	V	V	V	V	V	V	V	V	V	V	V	
Write	WR	L	H	L	H	H	L	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	3,5,7, 10,12
		H	C2	C3	C4	C5	C6	C7	C8	C9	C10	V	H	WR_P=L	V	CID3	
Write Auto Pre-charge	WRA	L	H	L	H	H	L	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	3,5,7, 10,12
		H	C2	C3	C4	C5	C6	C7	C8	C9	C10	V	L	WR_P=L	V	CID3	
Write **NT**	WR-**NT**	L	H	L	H	H	L	BL*=L	V	V	V	V	V	V	V	V	3,5,7, 10
		L	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
Read	RD	L	H	L	H	H	H	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	3,5,7, 12
		H	C2	C3	C4	C5	C6	C7	C8	C9	C10	V	H	V	V	CID3	
Read Auto Pre-charge	RDA	L	H	L	H	H	H	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	3,5,7, 12
		H	C2	C3	C4	C5	C6	C7	C8	C9	C10	V	L	V	V	CID3	
Read **NT**	RD-**NT**	L	H	L	H	H	H	BL*=L	V	V	V	V	V	V	V	V	3,5,7
		L	V	V	V	V	V	V	V	V	V	V	V	V	V	V	

Notes: 1. For two-cycle commands with no ODT control (ACT, MRW, WRP [Zero]), the command is not executed if the device receives CS as LOW on the second cycle (a command cancel).
2. CID[3]/R17 is a multimode pin allowing for either 16-high 3DS with CID[3] bit usage or R17 for high-density monolithic usage. These usages are mutually exclusive.
3. If CA5:BL*=LOW, device is placed into alternate burst mode (described in MR0:OP[1:0]) instead of the default burst length.
4. The WRITE PATTERN and WRITE PATTERN WITH AUTO PRECHARGE commands support BL16 and BL32 (non-OTF) only.
5. When CID[3] is not used, its CA decode is VALID.
6. If CW=LOW during the MRW command, the device executes the command and the mode register is written. If CW=HIGH, the device ignores the MRW command and the mode register is not changed. If CW=LOW, the device executes the MRR command. If CW=HIGH, the device may or may not execute the MRR command.
7. CS=LOW during the second cycle of on-die terminating two-cycle WR, RD and MRR commands.

8. CA0, CA1 encoded as LOW on second pulse to meet MRR requirements that only BL16 sequential burst order is supported for MRR command.
9. When the host issues MRR with CRC enabled, data is returned with CRC bit.
10. WR command with WR_partial=LOW indicates a partial WRITE command. This is to help the device start an internal read for read modify writes.
11. CID0-3 bits used for 3DS stacking die selection up to 16 high stacking support.
12. In the case of a device where the density or stacking doesn't require CA[13], the ball location for that function (considering the state of MIR) is connected to V_{DDQ}, and the device decodes CA[13]=L so that the proper selection of die and RA is provided.
13. For command truth table bits such as BG2, BA1, R16, R17, C10 and CID[3:0], which are unused based on a device's density, configuration width, and stacking options, the CA decode is defined as VALID when in these unused states.

Table 140: Command Truth Table: One-Cycle Commands

Function	Abv.	CS	CA Pins														Note
			CA 0	CA 1	CA 2	CA 3	CA 4	CA 5	CA 6	CA 7	CA 8	CA 9	CA 10	CA 11	CA 12	CA 13	
VREF CA	VrefCA	L	H	H	L	L	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7=L	V	
VREF CS	VrefCS	L	H	H	L	L	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7=H	V	
Refresh All	REFab	L	H	H	L	L	H	CID3	V	V	V or RIR	V or H	L	CID0	CID1	CID2	1,5, 13
Refresh Management All	RFMab	L	H	H	L	L	H	CID3	V	V	V	L	L	CID0	CID1	CID2	1,5, 13
Refresh Same Bank	REFsb	L	H	H	L	L	H	CID3	BA0	BA1	V or RIR	V or H	H	CID0	CID1	CID2	4,5, 13
Refresh Management Same Bank	RFMsb	L	H	H	L	L	H	CID3	BA0	BA1	V	L	H	CID0	CID1	CID2	4,5, 13
Precharge All Banks	PREab	L	H	H	L	H	L	CID3	V	V	V	V	L	CID0	CID1	CID2	5,6
Precharge Same Bank	PREsb	L	H	H	L	H	L	CID3	BA0	BA1	V	V	H	CID0	CID1	CID2	5,7
Precharge	PREpb	L	H	H	L	H	H	CID3	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	5,8
Reserved Future Use	RFU	L	H	H	H	L	L	V	V	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	L	H	H	H	L	H	V	V	V	V	H	L	V	V	V	9
Self Refresh Entry w/ Frequency Change	SREF	L	H	H	H	L	H	V	V	V	V	L	L	V	V	V	9

Table 140: Command Truth Table: One-Cycle Commands (Continued)

Function	Abv.	CS	CA Pins													Note
			CA 0	CA 1	CA 2	CA 3	CA 4	CA 5	CA 6	CA 7	CA 8	CA 9	CA 10	CA 11	CA 12	CA 13	
Power-Down Entry	PDE	L	H	H	H	L	H	V	V	V	V	V	H	ODT=L	V	V	10,11
Multi Purpose Command	MPC	L	H	H	H	H	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	V	
No Operation	NOP	L	H	H	H	H	H	V	V	V	V	V	V	V	V	V	13
Deselect	DES	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	

Notes: 1. The REFRESH ALL and REFRESH MANAGEMENT ALL commands are applied to all banks in all bank groups. CA6, CA7 and CA8 must be valid (V). The bank addresses and bank group addresses are don't care.
2. If the refresh management required bit is 0 (MR58:OP[0]=0), CA9 is only required to be valid (V) for a REF command, and the device will treat a RFM command as a REF command. If MR58:OP[0]=1, a REF command requires CA9=H.
3. If the refresh interval rate indicator bit is disabled (MR4:OP[3]=0) by the host, CA8 is only required to be valid (V). If the refresh interval rate indicator bit is enabled (MR4:OP[3]=1) by the host, the host is required to set CA8=H for REF commands issued at the 1X refresh interval rate and CA8=L for REF commands issued at the 2X refresh interval rate. If the host issues 2X REF commands with CA8=L while MR4:OP[3]=1, but the refresh rate requirement is 1X as determined internally by the device, the device may internally align to the 1X refresh rate.
4. The REFRESH SAME BANK and REFRESH MANAGEMENT SAME BANK commands refresh the same bank in all bank group bits. The bank bits, BA0 and BA1 on CA6 and CA7, respectively, specify the bank within each bank group.
5. In the case of a device where the density or stacking doesn't require CA[13], the ball location for that function (considering the state of MIR) will be connected to VDDQ, and the device will decode CA[13]=L so that the proper selection of die and RA is provided.
6. The PRECHARGE ALL command applies to all open banks in all bank groups.
7. The PRECHARGE SAME BANK command applies to the same bank in all bank groups. The bank bits specify the bank within each bank group.
8. The PRECHARGE command applies to a single bank as specified by bank address and bank group bits.
9. The SRE command places the device in self-refresh state.
10. The PDE command places the device is power-down state.
11. ODT=LOW is defined to allow ODT to persist when the device is in power-down mode.
12. For command truth table bits such as BG2, BA1, R16, R17, C10, and CID[3:0], which are unused based on a device's density, configuration width, and stacking options, the CA decode is defined as VALID when in these unused states.
13. Unlike DES, NOP is considered a valid command, and timing from a preceding valid command must satisfy any associated command timings.
14. When CID[3] is not used, its CA decode is VALID.
15. CID0-3 bits used for 3DS stacking die selection up to 16 high stacking support.

2-Cycle Command Cancel

ACT, WRP, WRPA and MRW are 2-cycle commands without associated ODT control requirements. The device does not execute these 2-cycle commands if CS_n is LOW on the second cycle (command cancel).

Figure 8: Command Cancel Timing Diagram

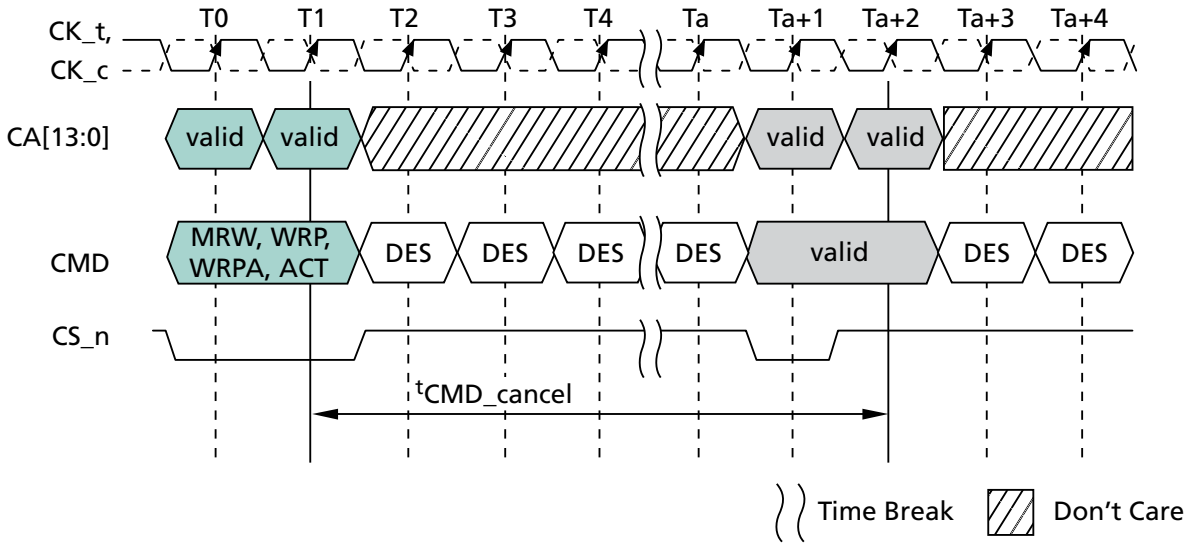


Table 141: Command Cancel Timing Parameters

Parameter	Symbol	3200-6400		6800-8400		Unit
		MIN	MAX	MIN	MAX	
Command cancel timing for ACT, WRP, WRPA, MRW when CS_n is LOW on second cycle	^{t}CMD_cancel	8	-	8	-	*n*CK

CS_n Truth Table

This table outlines the CS_n status while the device is in power-down mode and self refresh mode and trying to exit. It is assumed that after the device enters self refresh mode, the driver switches to CMOS to conserve power while the device switches into a lower power receiver mode. When the device is coming out of reset either at power-up initialization or during a reset with stable power, there are important requirements on the CS_n signal (both prior to, and after, applying a stable clock); refer to the Power-up and Initialization section and the Reset Initialization with Stable Power section for details.

CS_n is ACTIVE LOW.

For more details of all signals, see the command truth table and corresponding sections for Power-down and Self Refresh Operation.

Table 142: CS_n Truth Table

Current State	CS_n			Command (N)	Next Command (N+1)	Action (N)	Note
	Previous Cycle (N-1)[1]	Current Cycle (N)[1]	Next Cycle (N+1)[1]				
Power-down	H	H	H	X	X	Maintain power-down mode	
	H	L	H	PDX (NOP)	DES	Power-down mode exit	2
Self refresh	L	L	L	X	X	Maintain self refresh mode	3
	See footnote and refer to Self Refresh Operation section for details					Self refresh mode exit	4
Reset	X	X	X	X	X	Maintain reset	5
	L	L	H	NOP	DES	Exit reset	6

Notes: 1. CS_n (N) is the logic state of CS_n at clock edge N; CS_n (N-1) is the state of CS_n at the previous clock edge, CS_n (N+1) is the logic state of CS_n at the next clock edge N+1.
2. A single NOP cycle exits power-down mode; additional time is required after the exit before normal operation can resume.
3. To maintain self refresh, CS_n must remain LOW.
4. Self refresh exit is defined by the transition of CS_n LOW to HIGH with a defined pulse width ^{t}CSH_SRexit, followed by three or more NOP commands (^{t}CSL_SRexit) to ensure DRAM stability in recognizing the exit. See Self Refresh Operation section for more details.
5. RESET_n is used exclusively for maintaining the device in RESET. CS only is needed to properly exit.
6. Exiting RESET requires a stable clock and that ^{t}INIT5 is met with CS LOW and NOP on the CA bus followed by CS transitioning HIGH with NOP on the CA bus. CS remains HIGH for ^{t}CSH to allow the device CMOS receiver enough time to register the command.

MULTI-PURPOSE Command (MPC)

The MULTI-PURPOSE command (MPC) is used to issue commands associated with interface initialization, training, and periodic calibration. The MPC command is initiated with CS_n and CA[4:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. The MPC command has eight operands (OP[7:0] = CA[12:5]) that are decoded to execute specific commands.

The MPC command uses an encoding that includes the command encoding and the op-code payload in a single clock cycle. This enables the host to extend the setup and hold for the CA signals beyond the single cycle when the chip select asserts. In addition, the MPC command supports multiple cycles of CS_n assertion. The multiple cycles of CS_n assertion ensure the device captures the MPC command during at least one rising CK_t/CK_c edge.

MPC Op-Codes

Table 143: MPC Command Definition for OP[7:0]

Function	MPC Mode	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Notes
Exit CS Training Mode	CSTMX	0	0	0	0	0	0	0	0	2
Enter CS Training Mode	CSTMN	0	0	0	0	0	0	0	1	2
DLL Reset	DLL RESET	0	0	0	0	0	0	1	0	
Enter CA Training Mode	CATM	0	0	0	0	0	0	1	1	3
ZQCal Latch	ZQCLH	0	0	0	0	0	1	0	0	4
ZQCal Start	ZQCST	0	0	0	0	0	1	0	1	4
Stop DQS Interval Osc	DQSOSCSP	0	0	0	0	0	1	1	0	5
Start DQS Interval Osc	DQSOSCST	0	0	0	0	0	1	1	1	5
Set 2N Command Timing (default)	SET2N	0	0	0	0	1	0	0	0	
Set 1N Command Timing	SET1N	0	0	0	0	1	0	0	1	
Exit PDA Enumerate Program Mode	PDAENPX	0	0	0	0	1	0	1	0	6
Enter PDA Enumerate Program Mode	PDAENPE	0	0	0	0	1	0	1	1	6
Manual ECS Operation	ECS	0	0	0	0	1	1	0	0	
RFU	RFU	0	0	0	0	1	1	0	1	
RFU	RFU	0	0	0	0	1	1	1	0	
Apply VREFCA, VREFCS and RTT_CA/CS/CK	REFRTTAP	0	0	0	1	1	1	1	1	8
Set Group A RTT_CK = xxx	RTTCKA	0	0	1	0	0	x	x	x	7,12
Set Group B RTT_CK = xxx	RTTCKB	0	0	1	0	1	x	x	x	7,12
Set Group A RTT_CS = xxx	RTTCSA	0	0	1	1	0	x	x	x	7,12
Set Group B RTT_CS = xxx	RTTCSB	0	0	1	1	1	x	x	x	7,12
Set Group A RTT_CA = xxx	RTTCAA	0	1	0	0	0	x	x	x	7,12
Set Group B RTT_CA = xxx	RTTCAB	0	1	0	0	1	x	x	x	7,12
Set DQS_RTT_PARK = xxx	DQSRTTPARK	0	1	0	1	0	x	x	x	

Table 143: MPC Command Definition for OP[7:0] (Continued)

Function	MPC Mode	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Notes
Set RTT_PARK = xxx	RTTPARK	0	1	0	1	1	x	x	x	
PDA Enumerate ID	PDAENID	0	1	1	0	x	x	x	x	9
PDA Select ID	PDASLID	0	1	1	1	x	x	x	x	9
Configure ^{t}DLLK/^{t}CCD_L	DLLKCCDL	1	0	0	0	x	x	x	x	11
All Others Reserved	-	-	-	-	-	-	-	-	-	

Notes: 1. For more information on the MPC commands, see the Command Truth Table.
2. See the CS Training Mode section for more information regarding CS training mode entry and exit.
3. See the CA Training Mode section for more information regarding the CA training mode entry and exit.
4. See the ZQ Calibration section for information regarding ZQCal Start and ZQCal Latch.
5. See the DQS Interval Oscillator section for more information regarding Start DQS Osc and Stop DQS Osc.
6. See the Per DRAM Addressability section for more information regarding Enter PDA and Exit PDA modes.
7. Refer to CA ODT Strap Operation for more information regarding Group A and Group B configurations for Set RTT_CA, Set RTT_CS, and Set RTT_CK.
8. REFRTTAP applies the settings previously sent with the VREFCA , VREFCS, and MPC SET RTT_CA/CS/CK commands. Until this MPC REFRTTAP command is sent, the values from those other commands are only loaded into shadow registers. Prior to this, any MRR to the VREFCA, VREFCS and RTT_CA/CS/CK registers will return the currently applied device values. The shadow registers retain the latest set values. Any time the MPC REFRTTAP command is sent, the applied device values will change if updated VREFCA, VREFCS, and/or RTT_CA/CS/CK values were sent to the shadow registers following the previous MPC REFRTTAP command.
9. The PDA Enumerate ID and PDA Select ID op-codes include a 4-bit value, designated by xxxxb in the table. This is the value that is programmed into the MR for these fields. The PDA Enumerate ID can only be changed while in PDA Enumerate Programming mode.
10. For any MPC command that is associated with a mode register, the only way to program (write to) that mode register is via the MPC. Those mode registers are, therefore, read only and do not support MRW commands.
11. See MR13:OP[3:0] for encoding. The MPC ^{t}DLLK/^{t}CCD_L command sends the settings to the MR13:OP[3:0] shadow register and applies the settings to MR13 when the device encounters the DLL RESET command or SREF with CA9=L.
12. RTTCKA and RTTCKB MPC commands are used to set MR32:OP[2:0] CK ODT values; RTTCSA and RTTCSB MPC commands are used to set MR32:OP[5:3] CS ODT values; RTTCAA and RTTCAB MPC commands are used to set MR33:OP[2:0] CA ODT values.

Table 144: PDA Enumerate ID and PDA Select ID Encoding

MPC Function	OP[7:4]	OP[3:0]	Notes
PDA Enumerate ID	0110	0000b: ID 0 0001b: ID 1 0010b: ID 2 0011b: ID 3 0100b: ID 4 0101b: ID 5 0110b: ID 6 0111b: ID 7 1000b: ID 8 1001b: ID 9 1010b: ID 10 1011b: ID 11 1100b: ID 12 1101b: ID 13 1110b: ID 14 1111b: ID 15 - default	

Table 144: PDA Enumerate ID and PDA Select ID Encoding (Continued)

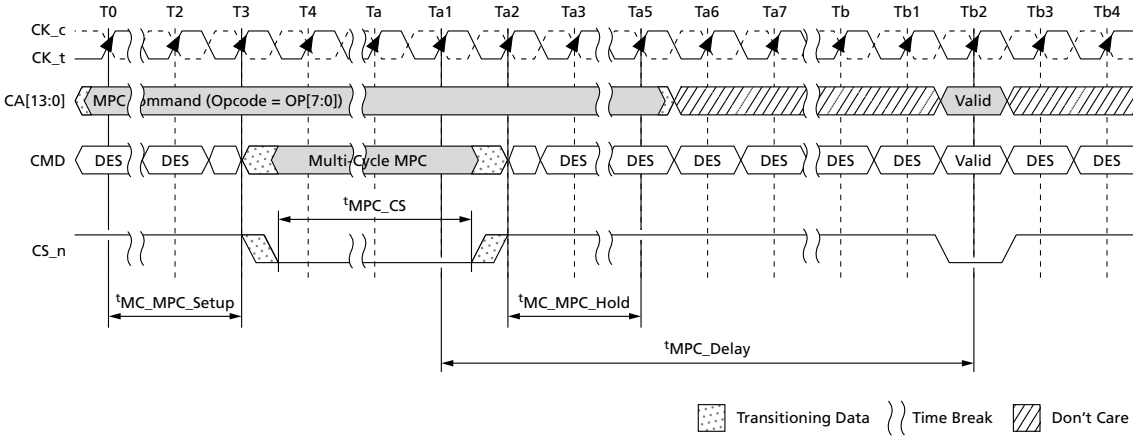
MPC Function	OP[7:4]	OP[3:0]	Notes
PDA Select ID	0111	0000b: ID 0 0001b: ID 1 0010b: ID 2 0011b: ID 3 0100b: ID 4 0101b: ID 5 0110b: ID 6 0111b: ID 7 1000b: ID 8 1001b: ID 9 1010b: ID 10 1011b: ID 11 1100b: ID 12 1101b: ID 13 1110b: ID 14 1111b: ID 15	1

Notes: 1. PDA SELECT ID 15 selects all devices regardless of their enumerate ID.

MPC Command Timing

As shown in the following figure, the MPC CMD timings can be extended to any number of cycles. The CS_n can also be asserted many consecutive cycles, limited by ^{t}MPC_CS. All timings are relative to the final rising CK_t/CK_c within the CS_n assertion window. The min delay from when the MPC is captured to the next valid command is specified as ^{t}MPC_Delay. Prior to CS Training, CA is driven with additional setup and hold beyond the CS_n assertion. For the device to latch the MPC in cases where the alignment between CS_n, CA, and CK may be unknown, the CA inputs must reach the proper command state and provide at least three cycles prior to CS_n transitioning from HIGH to LOW, CS_n must remain LOW for ^{t}MPC_CS, and CA must remain in the proper command state for, and provide at least three cycles after, CS_n transitions from LOW to HIGH. This additional setup and hold is only needed when MR2:OP[4] is set to 0 (multicycle MPC mode).

Figure 9: MPC Command Timing



The device supports an MR setting to indicate when a multicycle CS assertion may be used for MPC, VREFCA and VREFCS commands.

Figure 10: MPC Command Timing to 2-Cycle Command

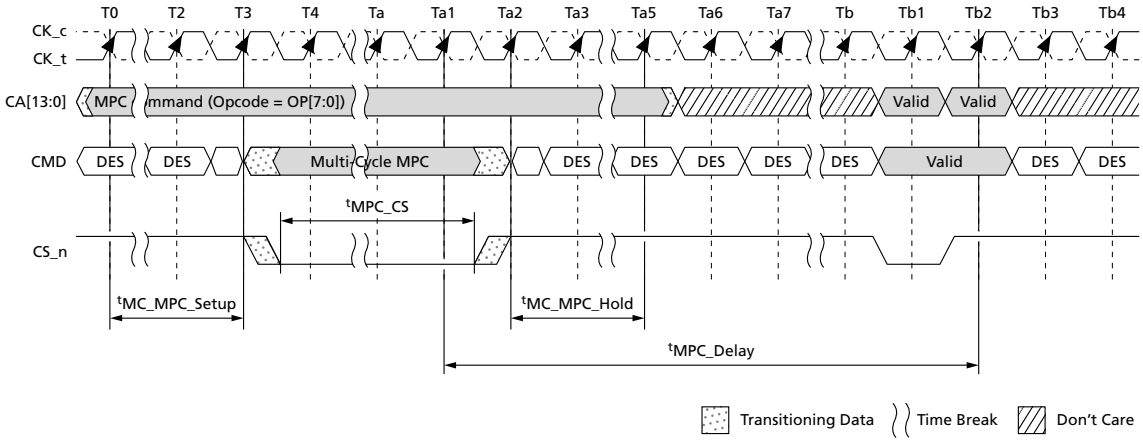


Table 145: MPC, VREFCA and VREFCS Assertion Duration

MR Address	Operating Mode	Description
MR2:OP[4]	CS Assertion Duration	0 = Multiple cycles of CS assertion supported for MPC, VREFCA and VREFCS. 1 = Only a single cycle of CS assertion supported for MPC, VREFCA and VREFCS.

Default value for the CS assertion duration is 0, which allows for multicycle CS assertions during training. The device can go in and out of this mode many times during the initialization and training sequence.

Table 146: MULTI-PURPOSE Command (MPC) Truth Table

Current State	MPC Command	Next State
All Banks Idle	CSTM (enter/exit)	All Banks Idle
	DLL RESET	
	CATM (enter)	
	ZQCAL (latch/start)	
	DQS interval oscillator (start/stop)	
	SET 1N/2N	
	PDA ENUMERATE PROGRAMMING (enter/exit)	
	MANUAL ECS operation	
	Apply $V_{REF,CA}$, $V_{REF,CS}$ and RTT_CA/CS/CK	
	CONFIGURE GROUP A/B RTT_CK/CS/CA	
	SET DQS_RTT_PARK	
	SET RTT_PARK	
	PDA ENUMERATE/SELECT ID	
	CONFIGURE ^{t}DLLK/^{t}CCD_L	

Table 146: MULTI-PURPOSE Command (MPC) Truth Table (Continued)

Current State	MPC Command	Next State
Active	ZQCAL (latch/start)	Active
	DQS Interval Oscillator (start/stop)	
	SET 1N/2N	
	CONFIGURE GROUP A/B RTT_CA/CS/CK	
	CONFIGURE ^{t}DLLK/^{t}CCD_L	

2N Mode

2N mode allows the system to provide more setup and hold on the CA bus. 2N mode is enabled by default on the device, and an MPC is used to change between 2N and 1N modes. MR2:OP[2] allows the state of the 2N mode to be read.

The device has defined two-cycle commands, which require the device to capture the command differently between 1N and 2N modes. In both modes, the first half of the command is sampled on the clock that the chip select is active. In 1N mode, the second half of the command is sampled on the next clock edge. In 2N mode, the second half of the command is sampled two clocks after the first half.

NT ODT signaling (on the chip select) is also delayed by a clock in 2N mode.

One-cycle commands operate the same in 1N and 2N mode, with the command sampled on the same clock where the chip select is active.

A two-cycle or one-cycle command can start on any clock (unlike gear-down mode). The following figure shows the differences between standard 1N mode with a two-cycle READ command followed by a one-cycle PRECHARGE command, along with comparable timing when operated in 2N mode with the same commands. In 2N mode, the host never sends two consecutive chip selects except during explicit cases such as exiting CATM mode.

Table 147: MR2 Functional Modes (For Reference Only)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
V	V	V	V	V	2N mode	V	V

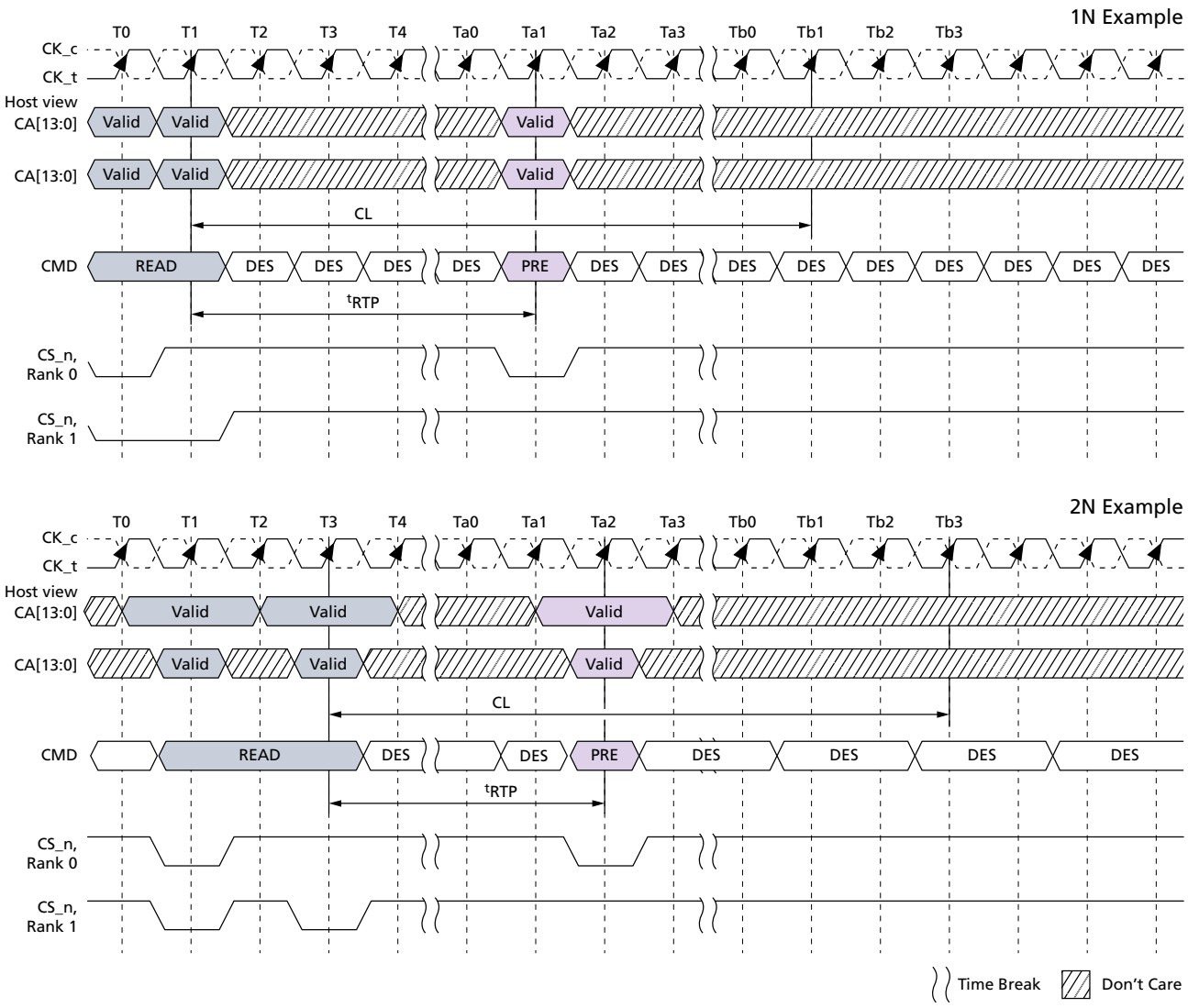
Notes: 1. OP[7:0] can be programmed with either 0 or 1 appropriate to the other bits controlled by MR2.

Table 148: 2N Mode Register Configuration

Function	Register Type	Operand	Data	Notes
2N mode	R	OP[2]	0b: 2N mode (default) 1b: 1N mode	1,2

Notes: 1. To ensure training modes can be enabled and run appropriately, the default (power-on) mode for the device is 2N mode. After CA training, the user can configure this bit to put the device into either 1N mode or 2N mode. Both 1N and 2N modes are valid operating conditions for the device.
2. Since 2N mode setting is an MPC-based command, it can only be programmed via that command and its mode register is therefore read-only.

Figure 11: Example of 1N vs. 2N Mode - Reference Only



Notes: 1. The host view CA[13:0] is shown for clarification, while CA[13:0] is what the device should expect.
2. CS_n Rank 1 is shown for READ NT ODT clarification.
3. ^{t}RTP can be launched on odd or even clocks.

1N/2N Mode Clarifications

Several DDR5 device features require specific CS_n and CA bus behavior to function correctly in 1N and 2N modes. The following shows these behaviors, with additional details in the respective sections of the data sheet.

Table 149: CS_n and CA Bus Required Behaviors

Behavior	CS Assertion Duration	CS_n Required Behavior for 1N	CS_n Required Behavior for 2N	CA Bus Required Behavior for Multicycle CS Assertion/2N
Cold or warm reset exit	Multi (default)	N/A	Static low for 3+ nCK	Static NOP for 3+ nCK

Table 149: CS_n and CA Bus Required Behaviors (Continued)

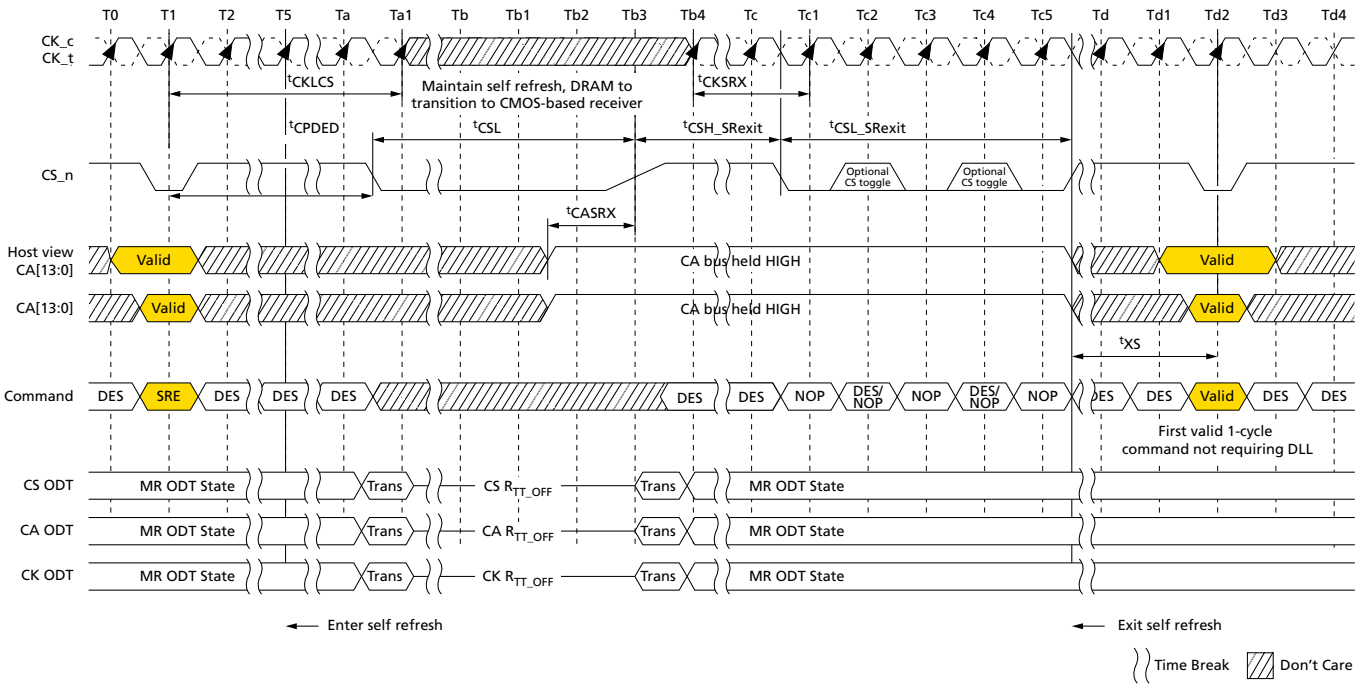
Behavior	CS Assertion Duration	CS_n Required Behavior for 1N	CS_n Required Behavior for 2N	CA Bus Required Behavior for Multicycle CS Assertion/2N
MPC (includes CSTM exit)	Single	Single low pulse	Single low pulse	Single MPC
	Multi	Static multicycle low	Static multicycle low	Static MPC surrounding CS_n low by ^{t}MC_MPC_*
VREFCS/VREFCA	Single	Single low pulse	Single low pulse	Single VREFCS/VREFCA
	Multi	Static multicycle low	Static multicycle low	Static VREFCS/VREFCA surrounding CS_n low by ^{t}MC_VREFCS_* / ^{t}MC_VREFCA_*
CATM exit (NOP Command)	Don't care	Static low for 2+ nCK	Static low for 2+ nCK	Static NOP for the duration of ^{t}CATM_CS_Exit
Power Down Mode Exit (NOP)	Don't care	Single low pulse	Single low pulse	Single NOP
Self Refresh Mode Exit (3 x NOPs)	Don't care	Static low for 3+ nCK	Static low for 3+ nCK	Static NOP for 3+ nCK if CS_n held static low
		Pulsing low 3+ cycles (...0, 1, 0, 1, 0...)	Pulsing low 3+ cycles (...0, 1, 0, 1, 0...)	Static NOP for 5+ nCK if CS_n is pulsed low

Notes: 1. The MR2:OP[4] CS assertion duration setting only applies to the MPC, VREFCA, and VREFCS commands.

Self Refresh in 2N Mode

The following figure shows details for self refresh entry/exit in 2N mode. Only exiting self refresh (3 x NOPs) with a pulsing CS_n (NOP-DES-NOP-DES-NOP) during ^{t}CSL_SRexit to a one-cycle command is shown, but behavior is similar for exiting self refresh (3 x NOPs) to a two-cycle command. Behavior is similar for frequency change during self refresh with or without V_{REF} and/or ODT changes. Pulsing CS_n during ^{t}CSL_SRexit is not required for self refresh exit (for example, CS_n may be held LOW for the full ^{t}CSL_SRexit duration).

Figure 12: Self Refresh Entry/Exit Timing in 2N Mode with One-Cycle Exit Command



Notes: 1. If ^{t}CSH_SRexit timing is not met after CS_n transition from LOW to HIGH or if three or more NOPs are not issued to satisfy ^{t}CSL_SRexit as defined in the specification, device operation cannot be guaranteed.

2. When ^{t}CSH_SRexit expires, the CA bus is allowed to transition from all bits HIGH to any valid (V) level. Prior to CS_n being registered LOW at ^{t}c+1, the CA bus must transition to NOP conforming to the CAI state of the device and complying with applicable device input timing parameters.

ACTIVATE Command

The ACTIVATE command opens (activates) a row in a particular bank for subsequent access. The values on BG[2:0] in x4 and x8 devices and BG[1:0] in x16 devices select the bank group; BA[1:0] (BA[0] only for 8Gb) selects the bank within the bank group. The address provided on the appropriate CA pins for R[17:0] selects the row. In case of a 3DS device, CID[3:0] is also selected to identify the correct die in the stack. This row remains active (open) for accesses until a PRECHARGE command is issued to that bank or a PRECHARGE ALL command is issued. A bank must be precharged before opening a different row in the same bank.

Bank-to-bank command timing for ACTIVATE commands uses two different timing parameters, depending on whether the banks are in the same or different bank group. ^{t}RRD_S (short) is used for timing between banks located in different bank groups. ^{t}RRD_L (long) is used for timing between banks located in the same bank group.

Consecutive ACTIVATE commands, which are allowed to be issued at ^{t}RRDmin, are restricted to a maximum of four within the time period ^{t}FAW (four activate window).

PRECHARGE Command

The PRECHARGE command deactivates the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (^{t}RP) after the PRECHARGE command is issued. After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE command being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. The precharge period is determined by the last PRECHARGE command issued to the bank.

If CA10 is LOW for the second half of a READ or WRITE command, the auto-precharge function engages. This feature enables the precharge operation to be partially or completely hidden during burst read cycles (dependent upon CAS latency), thus improving system performance for random data access. The RAS lockout circuit internally delays the precharge operation until the array restore operation completes (^{t}RAS satisfied) so that the AUTO PRECHARGE command may be issued with any read. Auto-precharge is also implemented during WRITE commands. The precharge operation engaged by the AUTO PRECHARGE command does not begin until the last data of the burst write sequence is properly stored in the memory array. The bank is available for a subsequent row activation at a specified time (^{t}RP) after the hidden PRECHARGE command (AUTO PRECHARGE) is issued to that bank. The precharge-to-precharge delay is defined by ^{t}PPD in the core timing tables. ^{t}PPD applies to any combination of precharge commands (PREab, PREsb, PREpb). ^{t}PPD also applies to any combination of precharge commands to a different die in a 3DS device.

PRECHARGE Command Modes

Three different types of precharge commands are supported:

- PRECHARGE (PREpb): applies precharge to a specific bank defined by BA[1:0] (if applicable) in a specific bank group defined by BG[2:0].
- PRECHARGE ALL (PREab): applies precharge to all banks in all bank groups.
- PRECHARGE SAME BANK (PREsb): applies precharge to a specific bank defined by BA[1:0] in all bank groups.

With a 3DS device, CID[3:0] is also selected to identify the target die.

The different encodings for PREsb, PREab, and PREpb shown in the PRECHARGE Encodings table

Table 150: PRECHARGE Encodings

Function	CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13
PRECHARGE ALL (PREab)	L	H	H	L	H	L	CID3	V	V	V	V	L	CID0	CID1	CID2
PRECHARGE SAME BANK (PREsb)	L	H	H	L	H	L	CID3	BA0	BA1	V	V	H	CID0	CID1	CID2
PRECHARGE (PREpb)	L	H	H	L	H	H	CID3	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2

Note: 1. Refer to the Command Truth Table for details.

Burst Length, Type, and Order

Accesses within a given burst are sequential only; interleaved is not supported. The ordering of accesses within a burst is determined by the burst length and the starting column address, as shown in the tables below. The burst length is defined by bits OP[1:0] of MR0. Burst length options include BC8 OTF, BL16, BL32 (optional), and BL32 OTF.

In the tables:

- T: output driver for data and strobes are in RTT_PARK.
- V: a valid logic level (0 or 1); however, respective buffer input ignores level on input pins.
- X: don't care.

BL16 Mode

Table 151: Burst Type and Order — READ

Burst Length	Burst Type	C3	C2	READ Burst Cycle and Burst Address Sequence															
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
BC8 OTF	Sequential	0	0	0	1	2	3	4	5	6	7	T	T	T	T	T	T	T	T
		0	1	4	5	6	7	0	1	2	3	T	T	T	T	T	T	T	T
		1	0	8	9	A	B	C	D	E	F	T	T	T	T	T	T	T	T
		1	1	C	D	E	F	8	9	A	B	T	T	T	T	T	T	T	T
16	Sequential	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		0	1	4	5	6	7	0	1	2	3	C	D	E	F	8	9	A	B
		1	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1	1	C	D	E	F	8	9	A	B	4	5	6	7	0	1	2	3

Table 152: Burst Type and Order — WRITE

Burst Length	Burst Type	C3	C2	WRITE Burst Cycle and Burst Address Sequence															
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
BC8 OTF	Sequential	0	V	0	1	2	3	4	5	6	7	X	X	X	X	X	X	X	X
		1	V	8	9	A	B	C	D	E	F	X	X	X	X	X	X	X	X
16	Sequential	V	V	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

BL32 Mode

If supported, BL32 (optional) and BL32 OTF (optional) are for x4 devices only.

Table 153: Burst Type and Order — READ

Burst Length	Burst Type	C10	C3	C2	READ Burst Cycle and Burst Address Sequence							
					1-4	5-8	9-12	13-16	17-20	21-24	25-28	29-32
BL32	Sequential	0	0	0	0-3	4-7	8-B	C-F	10-13	14-17	18-1B	1C-1F
		0	0	1	4-7	0-3	C-F	8-B	14-17	10-13	1C-1F	18-1B
		0	1	0	8-B	C-F	0-3	4-7	18-1B	1C-1F	10-13	14-17
		0	1	1	C-F	8-B	4-7	0-3	1C-1F	18-1B	14-17	10-13
		1	0	0	10-13	14-17	18-1B	1C-1F	0-3	4-7	8-B	C-F
		1	0	1	14-17	10-13	1C-1F	18-1B	4-7	0-3	C-F	8-B
		1	1	0	18-1B	1C-1F	10-13	14-17	8-B	C-F	0-3	4-7
		1	1	1	1C-1F	18-1B	14-17	10-13	C-F	8-B	4-7	0-3
BL16 in BL32 OTF	Sequential	0	0	0	0-3	4-7	8-B	C-F	X	X	X	X
		0	0	1	4-7	0-3	C-F	8-B	X	X	X	X
		0	1	0	8-B	C-F	0-3	4-7	X	X	X	X
		0	1	1	C-F	8-B	4-7	0-3	X	X	X	X
		1	0	0	10-13	14-17	18-1B	1C-1F	X	X	X	X
		1	0	1	14-17	10-13	1C-1F	18-1B	X	X	X	X
		1	1	0	18-1B	1C-1F	10-13	14-17	X	X	X	X
		1	1	1	1C-1F	18-1B	14-17	10-13	X	X	X	X

Notes: 1. In case of BL16 in BL32 OTF mode by setting MR0:OP[1:0]=11, the internal write operation starts eight cycles earlier than for BL32 mode. This means that the starting point for ^{t}WR and ^{t}WTR shall be pulled in by eight clocks.

Table 154: Burst Type and Order — WRITE

Burst Length	Burst Type	C10	C3	C2	WRITE Burst Cycle and Burst Address Sequence			
					1-8	0-16	17-24	25-32
BL32	Sequential	0	V	V	0-7	8-F	10-17	18-1F
BL16 in BL32 OTF	Sequential	0	V	V	0-7	8-F	X	X
		1	V	V	10-17	18-1F	X	X

IO Features and Modes

Output Disable

Device outputs can be disabled using the data output disable mode register (MR5:OP[0]). For normal operation, set MR5:OP[0]=0b (default). To disable device outputs, set MR5:OP[0]=1b.

TDQS/DM

The x8 configuration has a package ball that is shared between TDQS_t and DM_n. The Write Data Mask (DM) function is dependent upon Termination Data Strobe (TDQS). If TDQS is enabled, DM is disabled. If TDQS is disabled, DM may be enabled or disabled via mode register setting, as noted in the table below.

TDQS

One pair of Termination Data Strobe (TDQS) pins, TDQS_t/TDQS_c, is supported for the x8 configuration. The TDQS function is programmable via MR5:OP[4]. The x8 is the only configuration that supports the TDQS function. The x4 and x16 configurations do not support this function; therefore, for these configurations, the TDQS MR setting must be disabled (MR5:OP[4] = 0 (default)). When TDQS is enabled (MR5:OP[4] = 1), the same termination resistance function is applied to the TDQS_t/TDQS_c pins that is applied to DQS_t/DQS_c pins, except during READ commands where TDQS does not output any data and remains at RTT_DQS_PARK.

DM

See the Write Data Mask section for data mask functionality.

TDQS/DM Enable

When the TDQS is disabled (MR5:OP[4] = 0), the MR5:OP[5] bit may be used to enable or disable the DM_n pin function.

When both TDQS and DM functions are disabled, termination is turned off and the pins drive Hi-Z. The DM_n pin input receiver will be turned-off and does not expect any valid logic level.

Table 155: x8 TDQS Function Matrix

TDQS (MR5:OP[4])	DM
0: Disabled (default)	MR5:OP[5]
1: Enabled	Disabled

Programmable Preamble and Postamble

The device supports programmable read and write preambles and postambles.

Read Preamble and Postamble

The read preamble (^{t}RPRE) is configured as 1 ^{t}CK, 2 ^{t}CK (two unique modes), 3 ^{t}CK, and 4 ^{t}CK via MR8:OP[2:0]. The read postamble is configured as 0.5 ^{t}CK or 1.5 ^{t}CK via MR8:OP[6].

DQS has an option to drive early by x- ^{t}CK to accommodate different host receiver design as controlled by the read DQS offset in MR40:OP[2:0].

When operating at low speed (CL ≤ 30), ^{t}RPRE + Read DQS Offset ≥ 5 Clocks cannot be supported, as shown in the table below.

Table 156: Valid ^{t}RPRE + Read DQS Offset Combinations for CL ≤ 30

	^{t}RPRE (nCK)	Read DQS Offset (nCK)			
		0	1	2	3
When CL ≤ 30	1	Valid	Valid	Valid	Valid
	2	Valid	Valid	Valid	Invalid
	3	Valid	Valid	Invalid	Invalid
	4	Valid	Invalid	Invalid	Invalid

Figure 13: Example Read Preamble Modes (Default) with 0.5 ^{t}CK Postamble

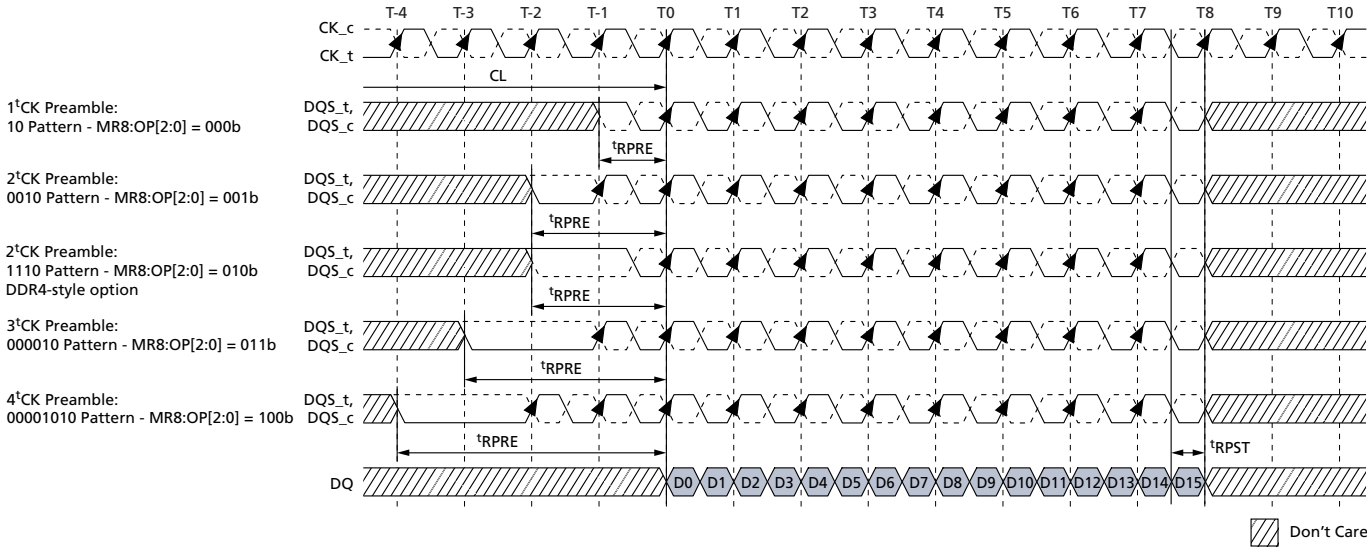


Figure 14: Example Read Preamble Modes (Default) with 1.5 tCK Postamble

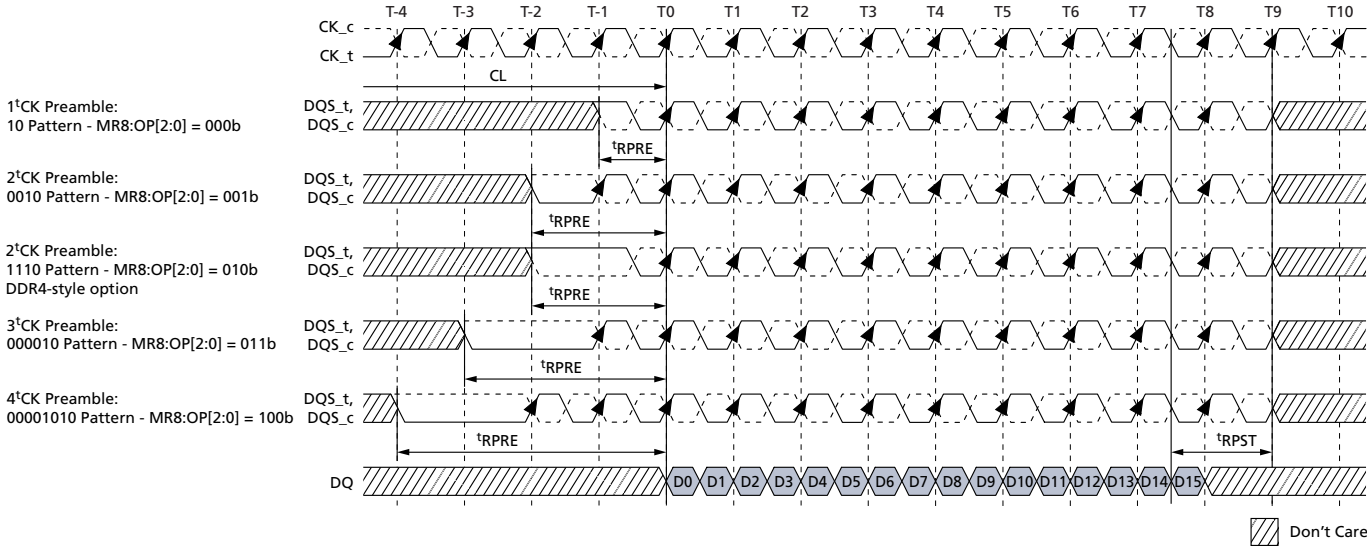
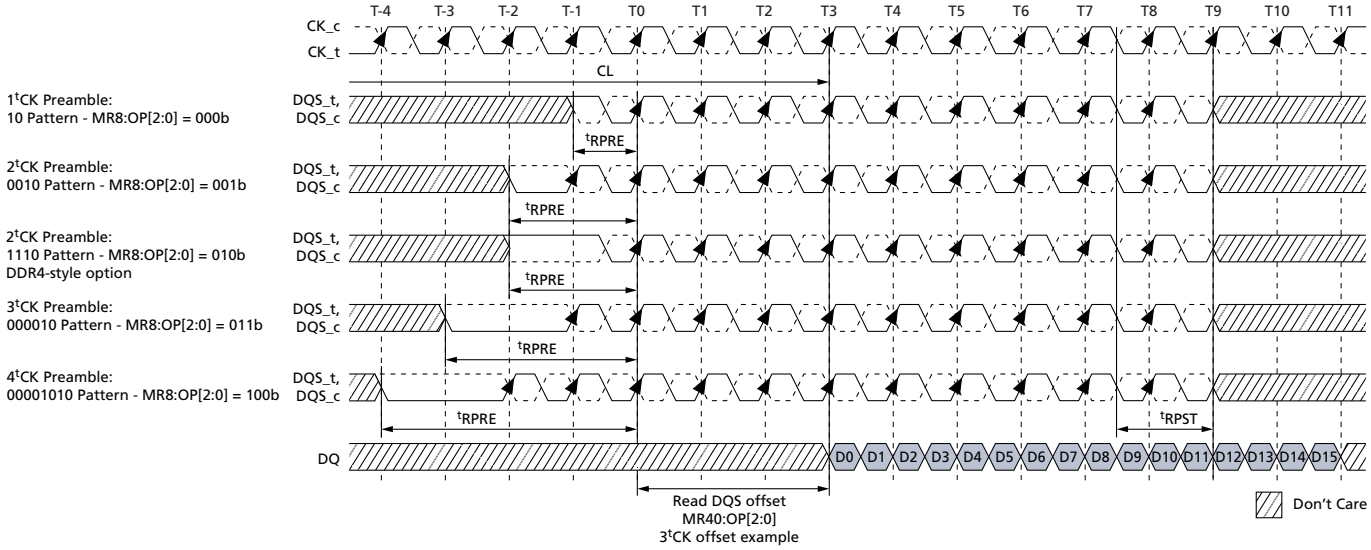


Figure 15: Example Read Preamble Modes (Default) with 3 tCK DQS Offset and with 1.5 tCK Postamble



Write Preamble and Postamble

The device supports a programmable write preamble and postamble. The write preamble is configured as 2 tCK, 3 tCK, and 4 tCK via MR8:OP[4:3]. The write postamble is configured as 0.5 tCK or 1.5 tCK via MR8:OP[7].

Figure 16: Example Write Preamble Modes (Default) with 0.5 tCK Postamble

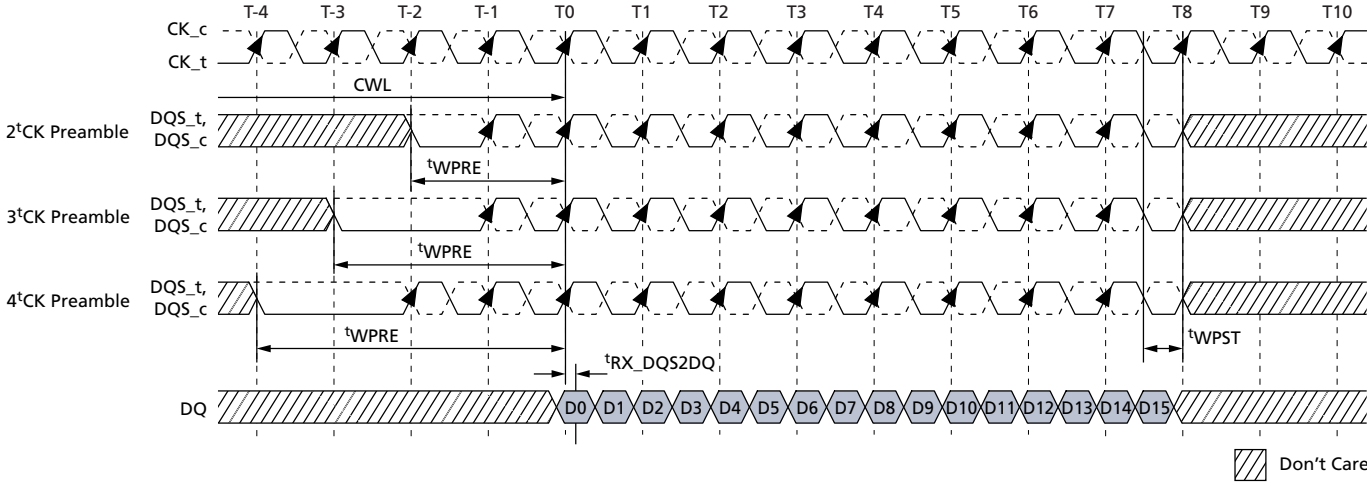
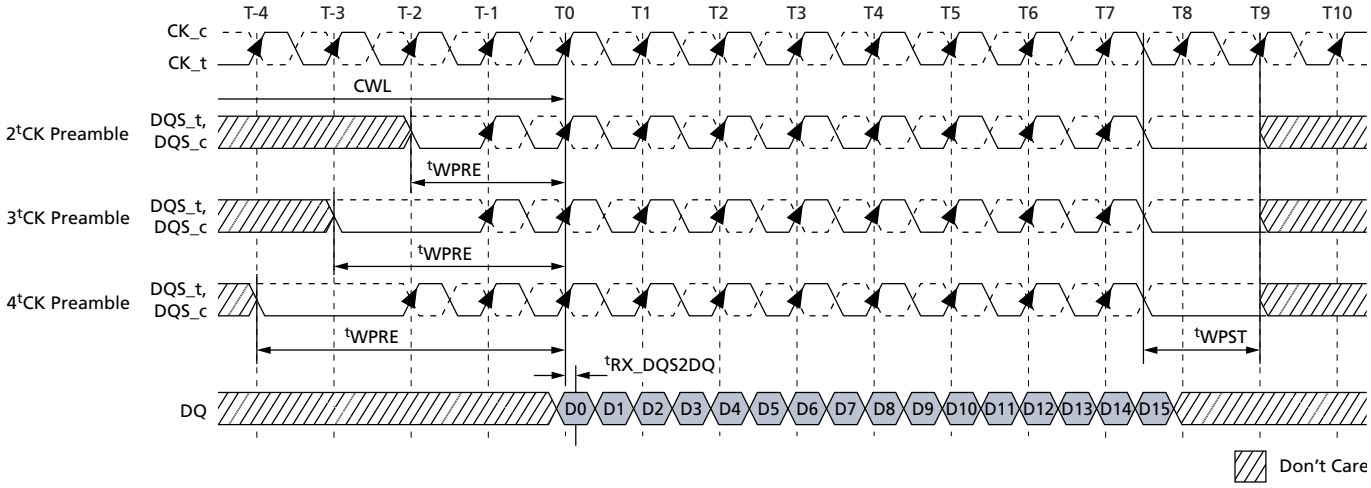


Figure 17: Example: Write Preamble Modes (Default) with 1.5 tCK Postamble



Interamble

The DQS strobe requires a preamble prior to the first latching edge (the rising edge of DQS_t with data valid) and a postamble after the last latching edge. The preamble and postamble options are set via MRW commands. Additionally, the postamble- and preamble-configured size does not force the host to add command gaps in the command interval just to satisfy postamble or preamble settings (that is, preamble = 4 ^{t}CK + postamble = 1.5^{t}CK does not force ^{t}CCD +5).

Read Interamble Timing Diagrams

In READ-to-READ operations with ^{t}CCD = BL/2, postamble for the first command and preamble for the second command disappear to create consecutive DQS latching edges for seamless burst operations. In the case of READ-to-READ operations with a command interval of ^{t}CCD +1, ^{t}CCD +2, etc., the toggles take precedence over static preambles if the postamble and preambles overlap.

Figure 18: Example: Seamless READ Operation: ^{t}CCD=MIN

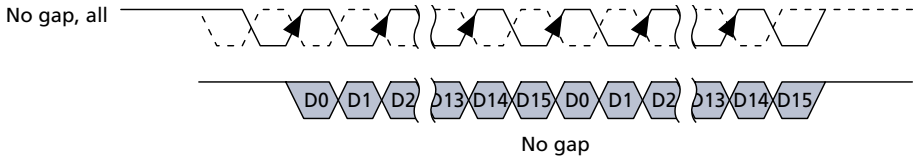


Figure 19: Example: Consecutive READ Operation: ^{t}CCD=MIN+1

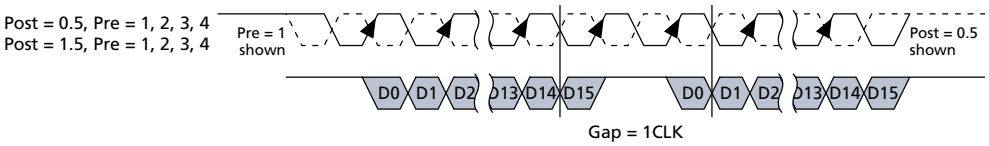


Figure 20: Example: Consecutive READ Operation: ^{t}CCD=MIN+2

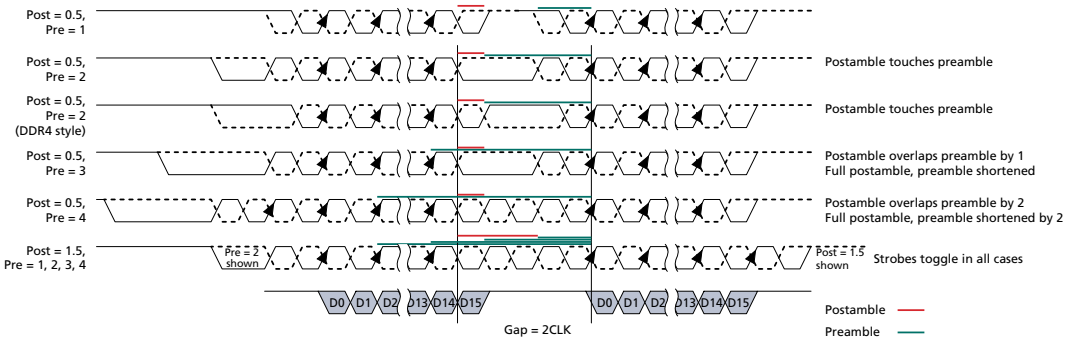


Figure 21: Example: Consecutive READ Operation: ^{t}CCD=MIN+3

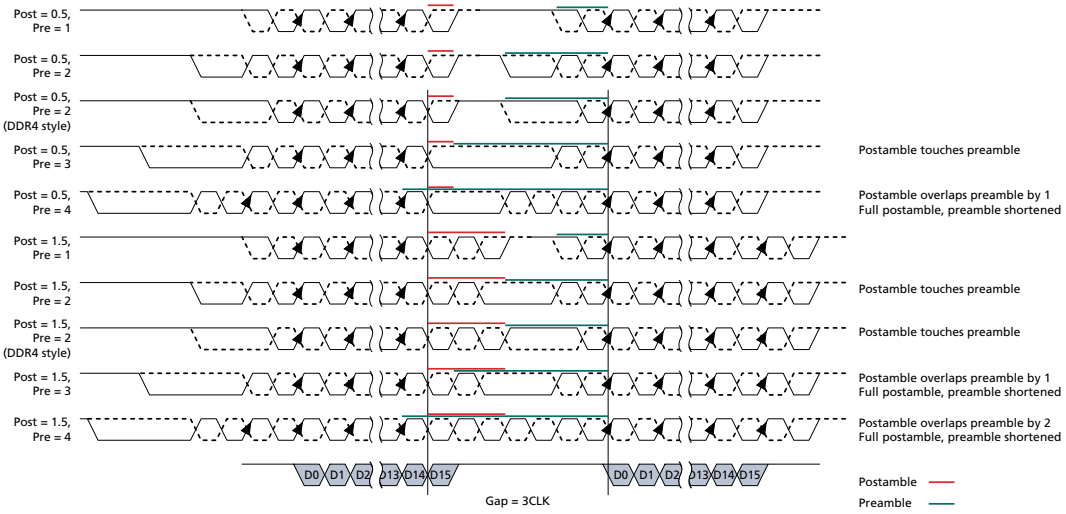


Figure 22: Example: Consecutive READ Operation: ^{t}CCD=MIN+4

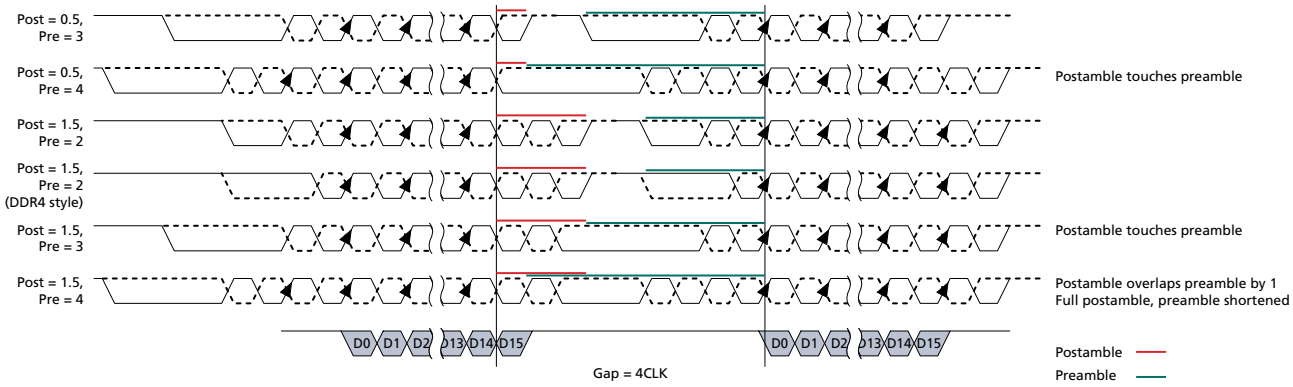
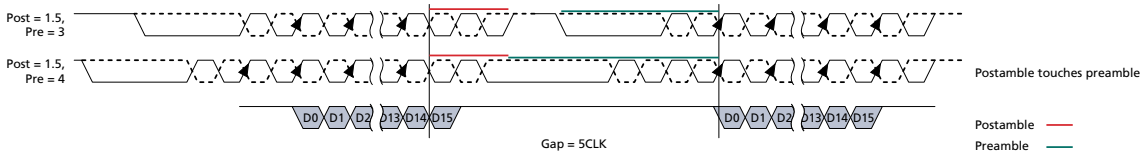


Figure 23: Example: Consecutive READ Operation: ^{t}CCD=MIN+5



Write Interamble Timing Diagrams

In WRITE-to-WRITE operations with ^{t}CCD=BL/2, postamble for the first command and preamble for the second command disappear to create consecutive DQS latching edges for seamless burst operations. In the case of WRITE-to-WRITE operations with a command interval of ^{t}CCD+1, ^{t}CCD+2, etc., the toggles take precedence over static preambles if the postamble and preambles overlap.

Figure 24: Example: Seamless WRITE Operation: ^{t}CCD=MIN

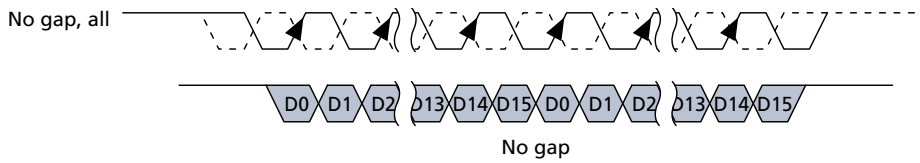


Figure 25: Example: Consecutive WRITE Operation: ^{t}CCD=MIN+1

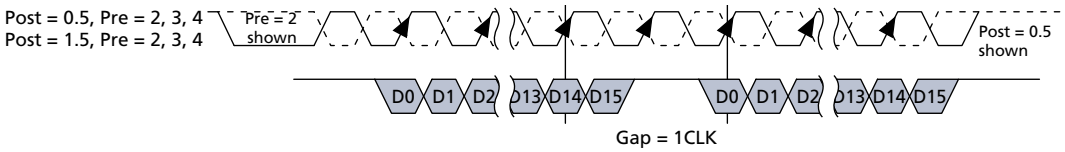


Figure 26: Example: Consecutive WRITE Operation: ^{t}CCD=MIN+2

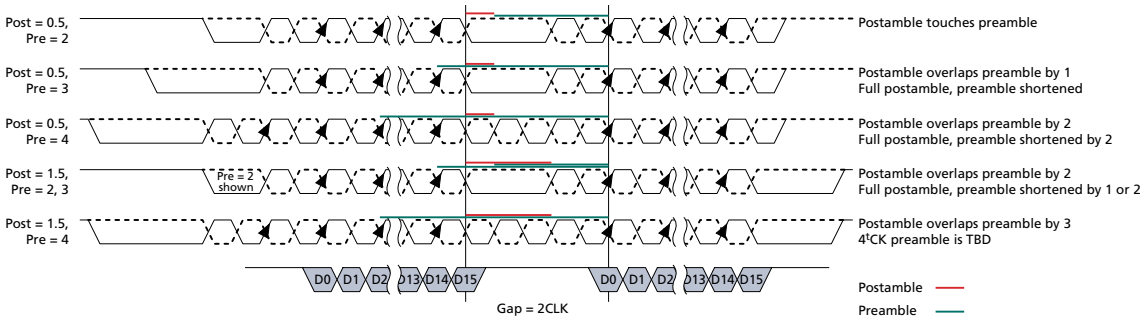


Figure 27: Example: Consecutive WRITE Operation: ^{t}CCD=MIN+3

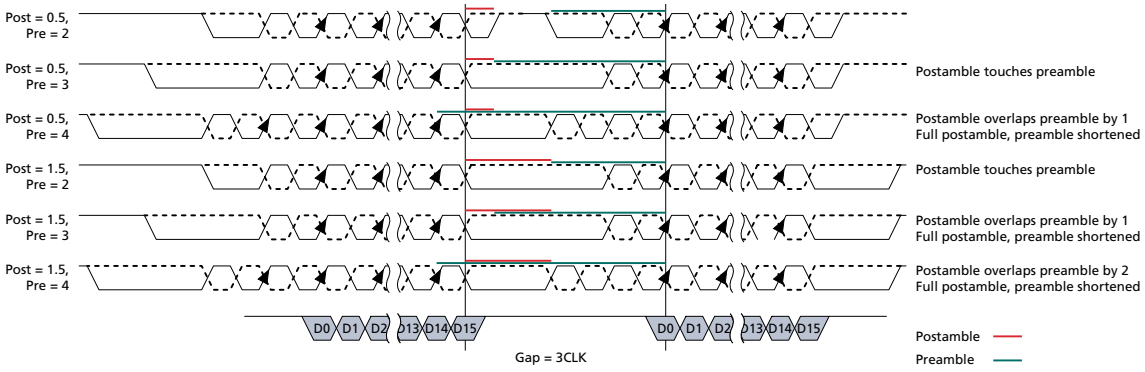


Figure 28: Example: Consecutive WRITE Operation: ^{t}CCD=MIN+4

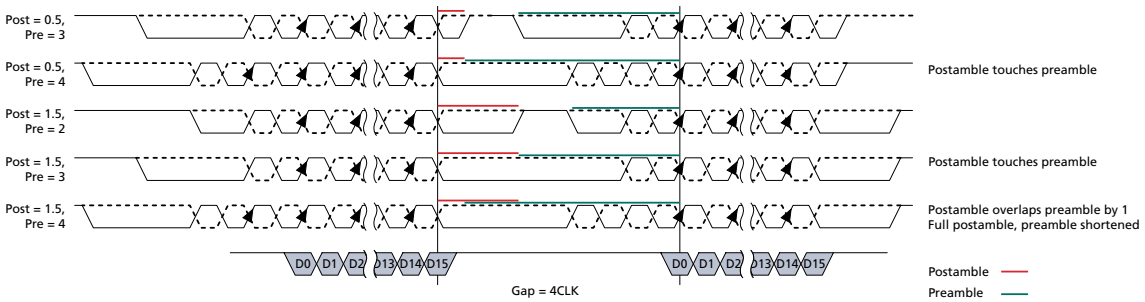
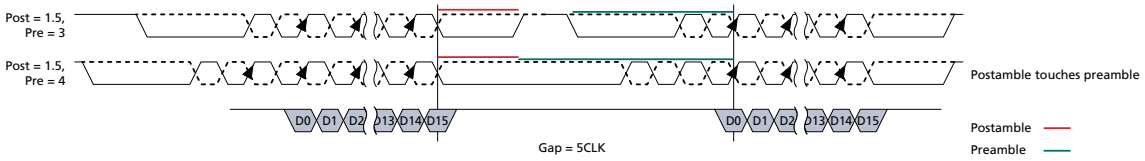


Figure 29: Example: Consecutive WRITE Operation: t_{CCD}=MIN+5



On-Die ECC

Single error correction (SEC) ECC is required to improve the data integrity within the device. The device uses 128 data bits to compute the ECC code of 8 ECC check bits.

For a x4 device, internal prefetch for on-die ECC is 128 bits, even though a x4 is a 64-bit prefetch device. For each read or write transaction in a x4 device, an additional section of the device array is accessed internally to provide the required additional 64 bits used in the 128-bit ECC computation. In other words, in a x4 device, each 8-bit ECC check bit word is tied to two 64-bit sections of the device. In the case of a x8 device, no extra prefetch is required because the prefetch is the same as the external transfer size. For a x16 device, two 128-bit data words and their corresponding 8 check bits are fetched from different internal banks (same external bank address).

Each 128 data bits and the corresponding 8 check bits are checked separately and in parallel.

On reads, the device corrects any single bit errors before returning the data to the memory controller. The device must not write the corrected data back to the array during a READ cycle.

On writes, the device computes ECC and writes data and ECC bits to the array. If the external data transfer size is smaller than the 128 data bit code word (x4 devices), the device will have to perform an internal READ-MODIFY-WRITE operation. The device will correct any single bit errors that result from the internal read before merging the incoming write data and then re-compute 8 ECC check bits before writing data and ECC bits to the array. In the case of a x8 and x16 device, no internal read is required.

For a x16 device, two 136-bit code words are read from two internal banks (same external bank address); one code word is mapped to DQ[0:7] and the other code word is mapped to DQ[8:15].

SEC Overview

The ECC blocks shown in the following figure are the ECC check bit generator, syndrome generator, and syndrome decode and correction. The check bit generator and syndrome generator blocks are fully specified by the H matrix.

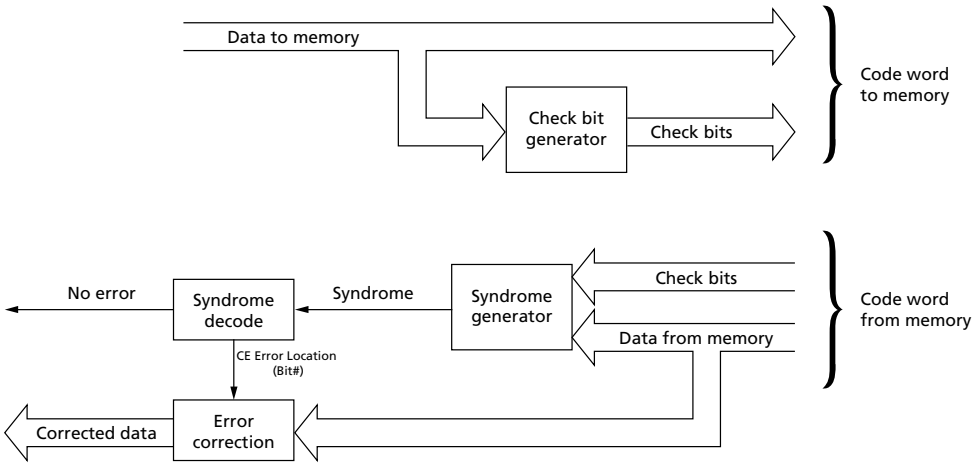
The syndrome decode block executes the following function:

- Zero syndrome => No error
- Non-zero syndrome matches one of the columns of the H matrix => Flip corresponding bit
- Non-zero syndrome that does not match any of the columns in the H matrix => DUE

Where:

- DUE: Detected uncorrected

Figure 30: On-Die ECC Block Diagram

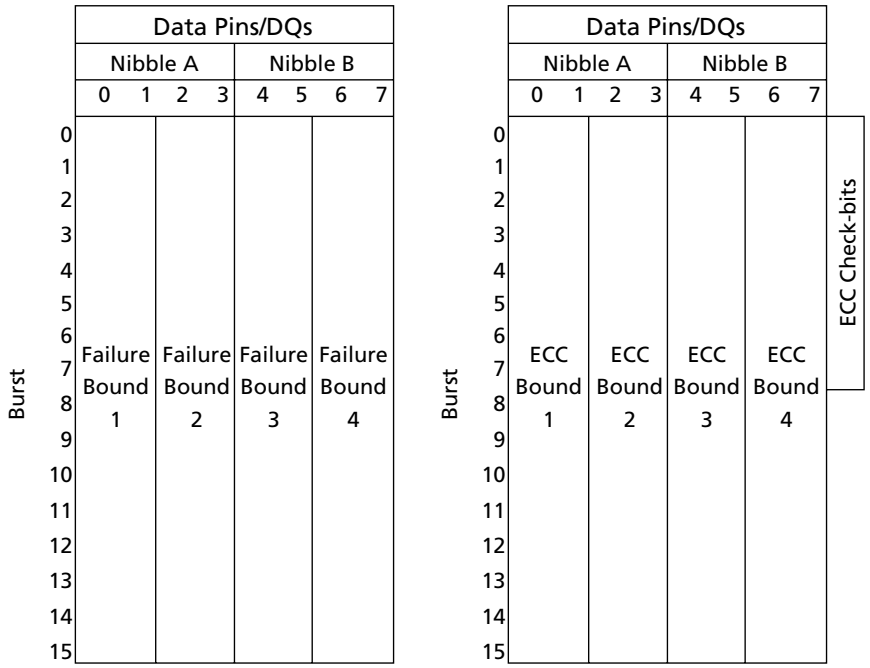


SEC Code Properties

To maintain the bounded failure design guidelines, miscorrections by the on-die ECC must be restricted when a bounded failure causes a multibit error. In devices with bounded failures, it is suggested that the DRAM vendor uses an on-die ECC code that maintains the failure boundaries. That is, if an error is contained in one boundary, the on-die ECC should not spread the error into a second boundary by miscorrection. Note that if failures are not bounded in the device, the on-die ECC does not need to have these properties.

To restrict miscorrection in devices following bounded failure design guidelines, the data may be divided into blocks aligned with the bounded failure and miscorrection should be restricted in case an error is contained in a single data block. The 128 data bits used to compute a set of 8 check bits may be divided into data blocks up to 32 bits in size. These data blocks are to be determined by the memory vendor to best align with internal DRAM failures. For example, a common component failure may impact 32 bits per 128 data bits; the vendor may choose to divide the 128 data bits into four 32-bit blocks each of which correspond to the bits impacted by one of the components failing.

Figure 31: Example Failure Boundaries vs. On-Die ECC Data Blocks



If a multi-bit error occurs on a read and is limited to one data block, the on-die ECC SEC code should do one of the following

- Miscorrect a bit in the data block containing the error
- Miscorrect a bit in the on-die ECC check bits
- Detect the error (a SEC code may detect some multi-bit errors, but detection of these errors is not guaranteed)

The selection of block size and data blocks is determined by the vendor to best suit the device architecture and possible modes of failure.

Reliability Design Guidelines

These reliability design guidelines aim to bound bits impacted by certain device failures. This limits the number of failure patterns seen by the memory controller such that correction of many failures can be reliably performed in DIMMs with one ECC device.

Many internal device failures may impact only a portion of the data from a fetch. The likelihood of a specific component failing may also vary between process generations and DRAM vendors.

These guidelines can be used by devices to bound failures from the components most likely to fail. These design guidelines can only address failures that impact a portion of the data from a 128-bit fetch. Failures that impact all the data in a 128-bit fetch from a device (for example, device failure, bank failure) cannot be bounded as described here.

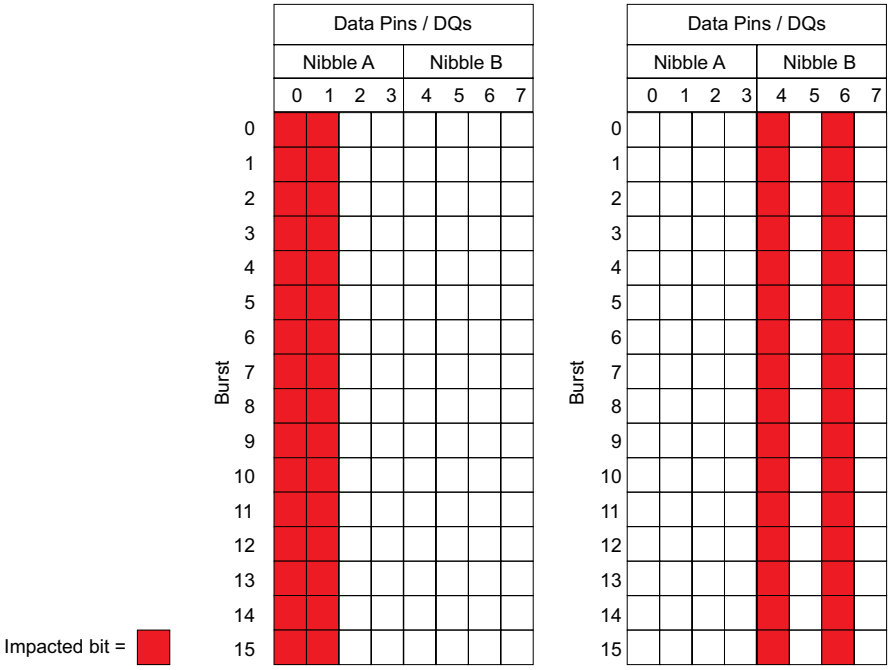
x8 Device Guidelines

In a x8 device, bounded failures are defined by the following qualities:

- A bounded failure does not impact more than 32 bits of data in a 128-bit fetch.
- The data bits impacted by a bounded failure are confined to at most 2 DQs (that is, the failures are DQ-aligned).
- The DQs transmitting data impacted by the failure will both be in either the first nibble or the second nibble of a burst. That is, the impacted DQs will both be in the set of the first 4 DQs (DQ0, DQ1, DQ2, DQ3) or the last four DQs (DQ4, DQ5, DQ6, DQ7).

The figure below shows examples of failure boundaries for x8 devices. The device on the left has a bounded failure in lanes DQ0 and DQ1 in the first nibble. The device on the right has a bounded failure in lanes DQ4 and DQ6 in the second nibble.

Figure 32: Examples of x8 Failure Boundaries



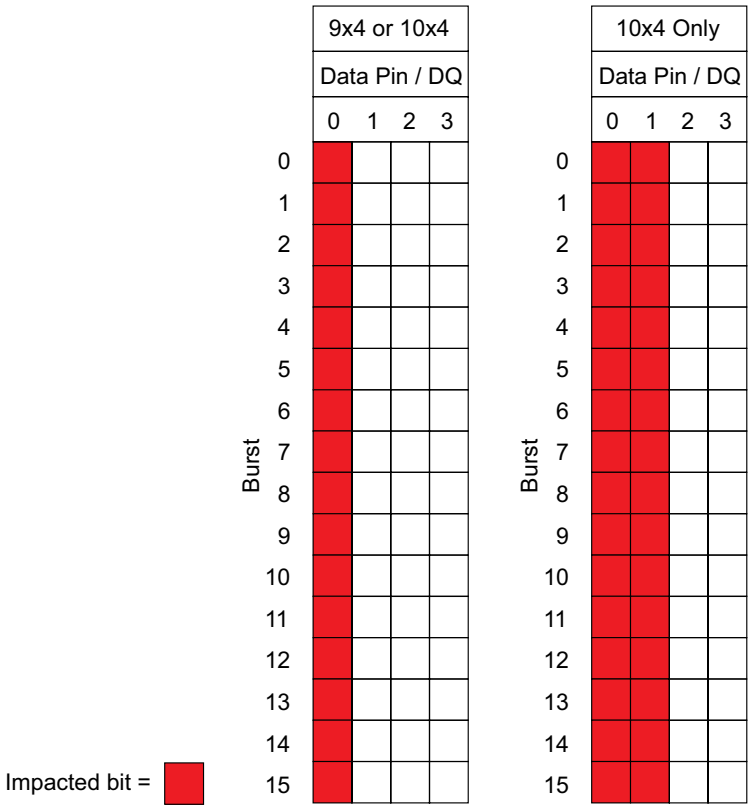
x4 Device Guidelines

A x4 device has similarly defined qualities for the failure boundaries, with the noted exception of the number of bits impacted by a bounded failure. In a device in a 9x4 configuration, bounded failures should not impact more than 16 bits. However, in a 10x4 device, the bounded failure may impact up to 32 bits.

In a x4 device, bounded failures are defined by the following qualities:

- A bounded failure in a device in a 9x4 configuration should not impact more than 16 bits of data in each 64-bit access of a 128-bit prefetch.
- A bounded failure in a device in a 10x4 configuration should not impact more than 32 bits of data in each (either) 64-bit access of a 128-bit prefetch.
- For a device in a 9x4 configuration, the data bits impacted by a bounded failure are confined to one DQ.
- For a device in a 10x4 configuration, the data bits impacted by a bounded failure are confined to at most two DQs.

Figure 33: Examples of x4 Failure Boundaries



Write Operation

The WRITE operation stores data in the device and is initiated by the WRITE command, during which the beginning column address and bank/group address for the data to be written to the array is provided. The data is provided on the DQ inputs CWL cycles after the WRITE command along with the proper waveform on the DQS inputs. CWL is defined and measured from final cycle of the WRITE command to the first rising DQS (excluding write preamble).

Write Data Mask

One write data mask (DM_n) pin for each byte data group is supported on x8 and x16 devices. The DM_n pin/function is enabled via mode register. For the x4 configuration, the DM mode register setting must be disabled. The DM_n pin has identical timings and termination functionality on the WRITE operation as the DQ pins (shown below). The DM_n pin is not used for READ cycles and the pin should behave like a DQ pin driving HIGH or be terminated to RTT_PARK. When the DM function is disabled by MR, the device disables the DM input receiver and output transmitter and does not expect nor drive any valid logic level.

Each data mask burst bit position corresponds to the same bit position in the DQ data burst across the corresponding byte group. If DM is disabled (MR5 OP[5] = 0), WR_partial (WR_P) must be HIGH. DM_n may be HIGH or LOW.

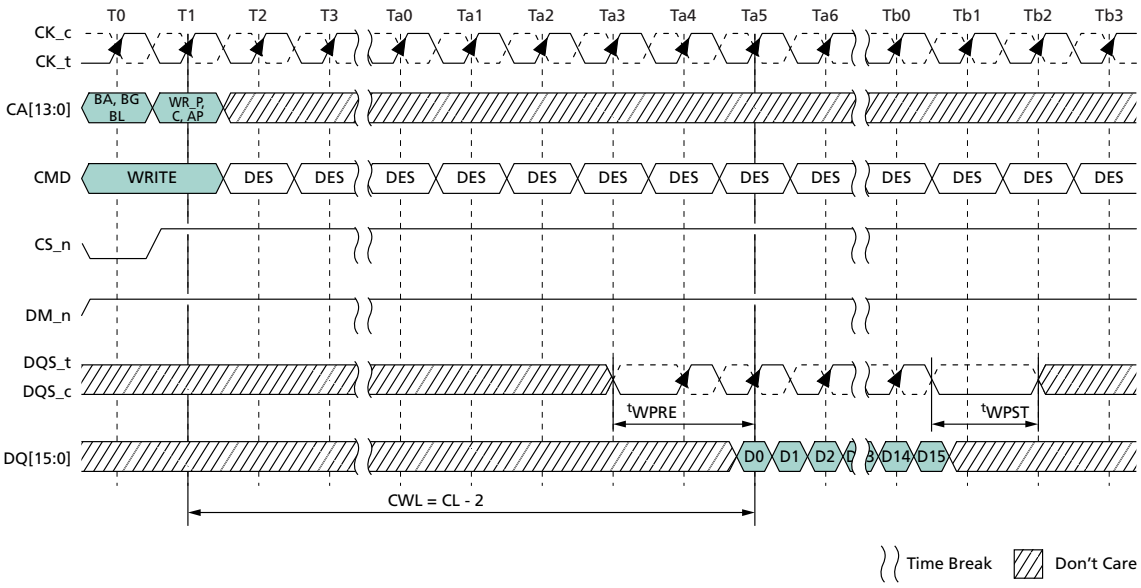
Partial Write

When the Partial Write function is enabled (WR_P = LOW), as part of the WRITE command, it helps start an internal read for READ-MODIFY-WRITE operation during masked writes. This partial write (WR_P = LOW) functionality must be used in conjunction with the DM_n data. If WR_partial = HIGH during write, the mask data on DM_n must be HIGH. If DM is disabled (MR5 OP[5] = 0), WR_P must be HIGH. DM_n may be HIGH or LOW.

WRITE Burst Operation

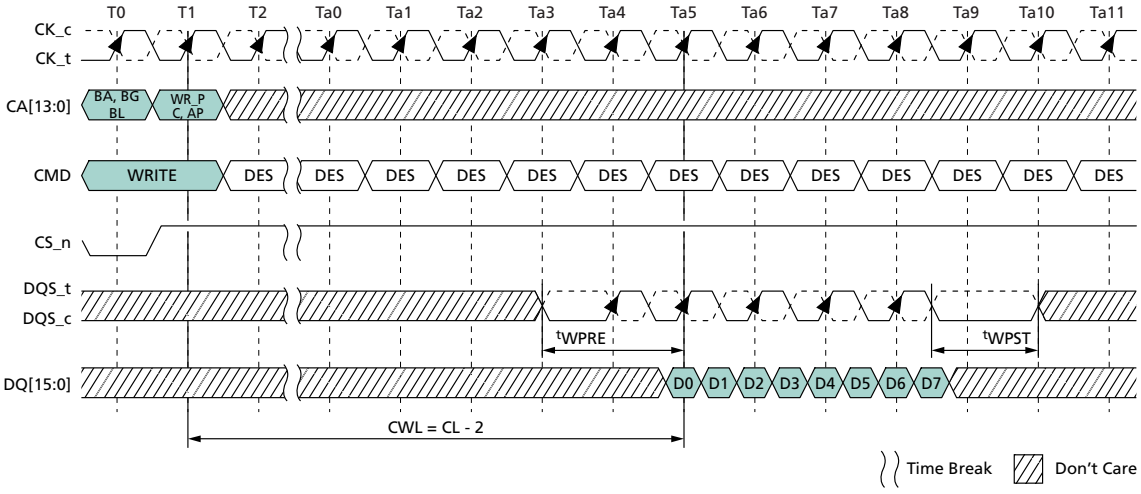
In the following example write timing figures, the details of each write parameter are defined separately for improved understanding. For clarity of illustration, CK and DQS are shown aligned; DQS and DQ are shown center-aligned. Offset between CK and DQS and between DQS and DQ may be appropriate.

Figure 34: WRITE Burst Operation (BL16)



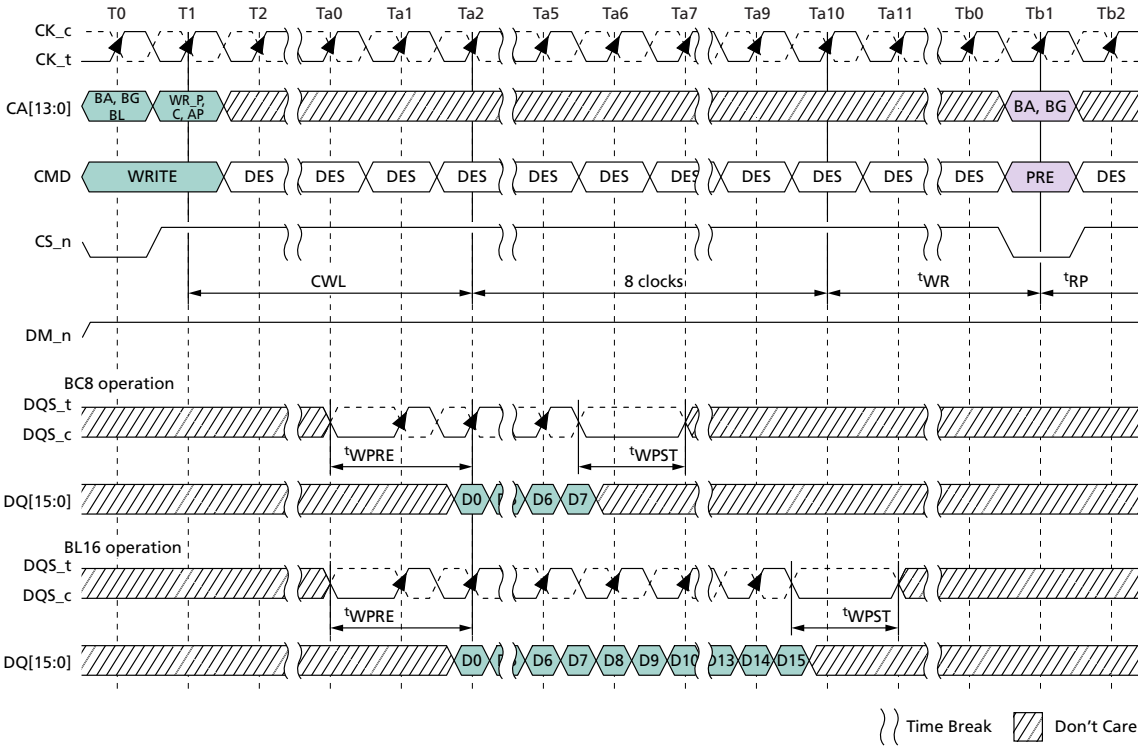
Notes: 1. BL = 16; preamble = 2^{t}CK 0010 pattern; postamble = 1.5^{t}CK.
2. Dn = data-in from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 35: WRITE Burst Operation (BC8 OTF)



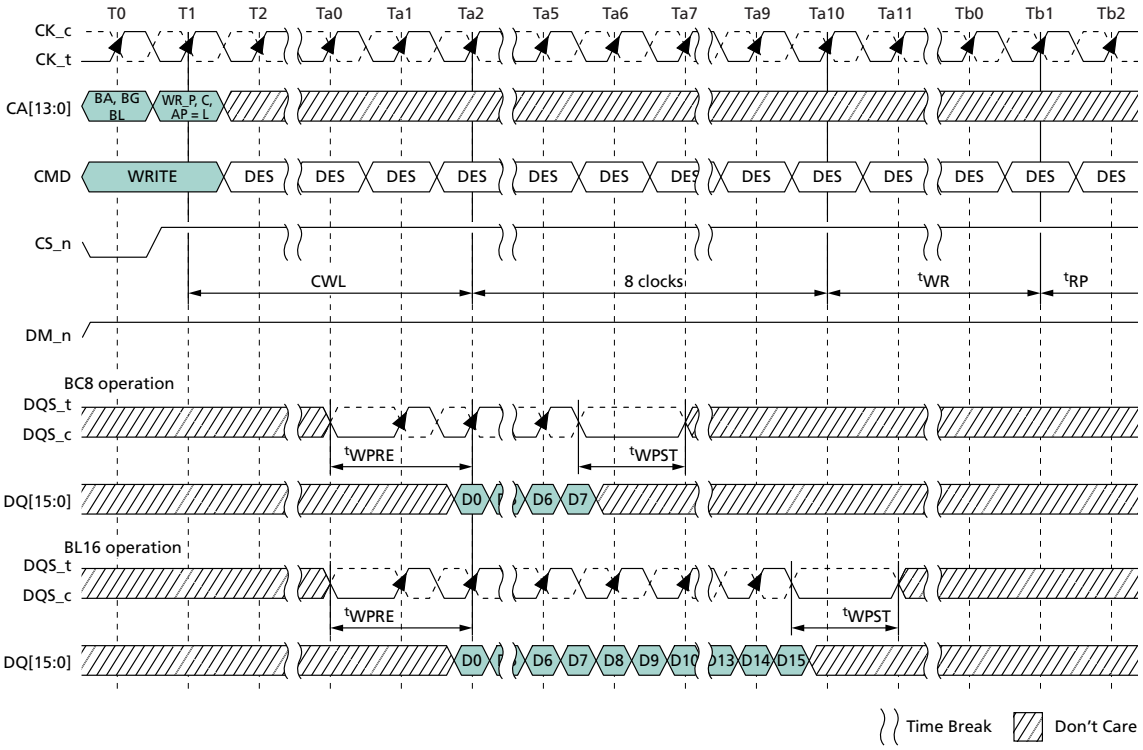
Notes: 1. BL = 16; preamble = 2^{t}CK 0010 pattern; postamble = 1.5^{t}CK.
2. Dn = data-in from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. In non-CRC mode, DQS_t and DQS_c stop toggling at the completion of the BC8 data bursts, plus the postamble.

Figure 36: WRITE (BL16) to PRECHARGE Operation with 2 tCK Preamble



Notes: 1. BL = 16 or BC = 8; preamble = 2tCK - 0010 pattern; postamble = 1.5tCK.
2. Dn = data-in from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. tWR is referenced from the first rising clock edge after the last write data shown at Ta10. tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.

Figure 37: WRITE (BL16) With Auto Precharge Operation with 2tCK Preamble



Notes: 1. BL = 16 or BC = 8; preamble = 2tCK - 0010 pattern; postamble = 1.5tCK.
2. Dn = data-in from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. tWR is referenced from the first rising clock edge after the last write data shown at Ta10. tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.

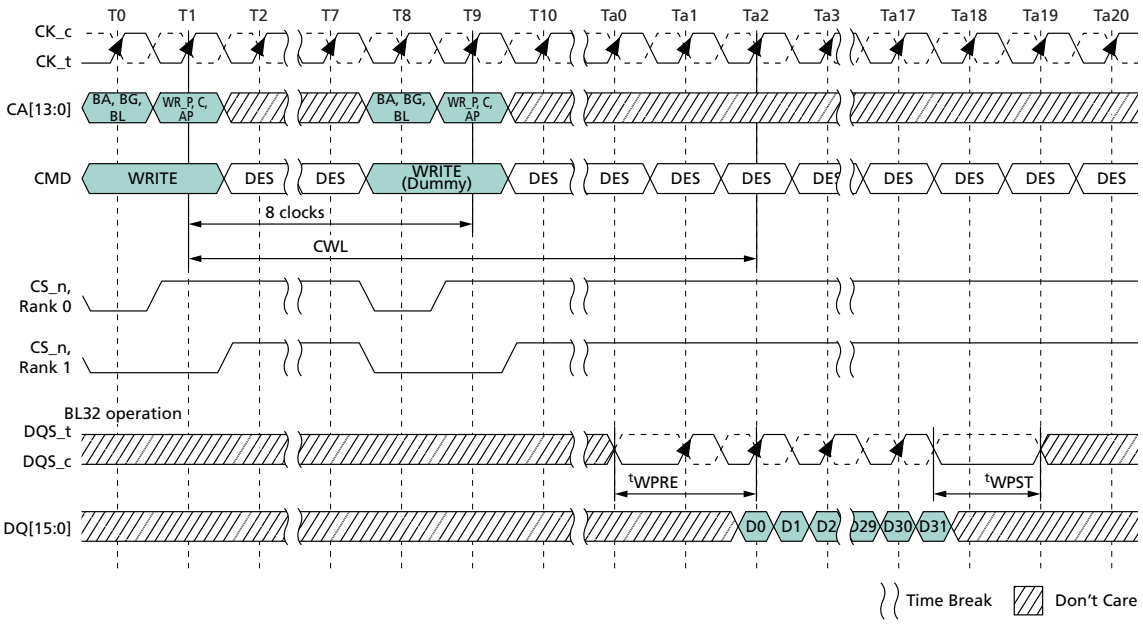
WRITE Burst Operation for Optional BL32 Mode

The following write timing diagrams cover write timings for fixed BL32, BL32 in BL32 OTF mode, and BL16 in BL32 OTF mode for x4 devices only.

For clarity of illustration, CK and DQS are shown aligned; DQS and DQ are shown center-aligned. Offset between CK and DQS and between DQS and DQ may be appropriate.

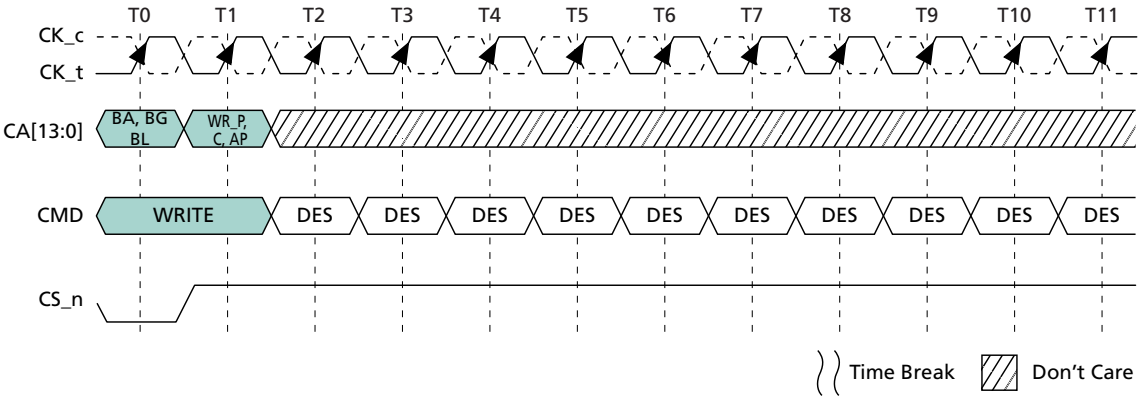
A dummy WRITE command is required for second half of the transfer of BL32. If non-target ODT is needed in the system, then a dummy ODT command must be issued to the non-target rank for second half of the transfer of BL32.

Figure 38: Write Timing for Fixed BL32 and BL32 OTF Mode



Notes: 1. BL = 32; preamble = 2^{t}CK; postamble = 1.5^{t}CK.
2. Dn = data-in from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. A dummy WRITE command is required for the second half of the transfer with a delay of 8 clocks from the first WRITE command.
5. The figure also shows a dummy ODT command being issued to non-target rank 1 for the second half of the transfer.
6. C10 is used for burst ordering and must be LOW for the first WRITE command and HIGH for the dummy WRITE command.
7. The device supports an optional fixed BL32 mode and optional BL32 on-the-fly (OTF) mode for x4 devices only.
8. CA bits other than C10 and AP in dummy WRITE command are the same as the first WRITE command.

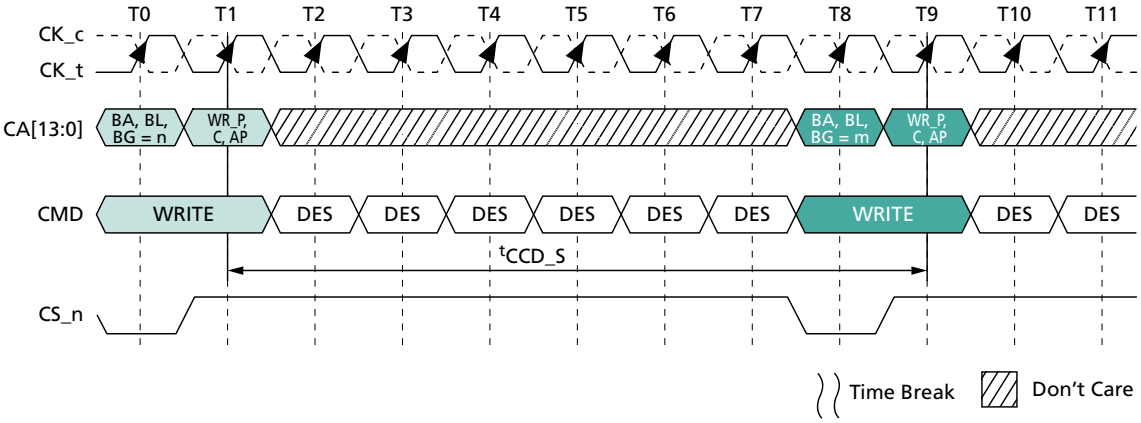
Figure 39: Write Timing for BL16 in BL32 OTF Mode



Notes: 1. The figure shows BL16 WRITE operation when MR0 is programmed to use BL32 OTF mode. In this case, no dummy WRITE command is required because the data transfer size is BL16.
2. DES commands are shown for ease of illustration; other commands may be valid at these times.

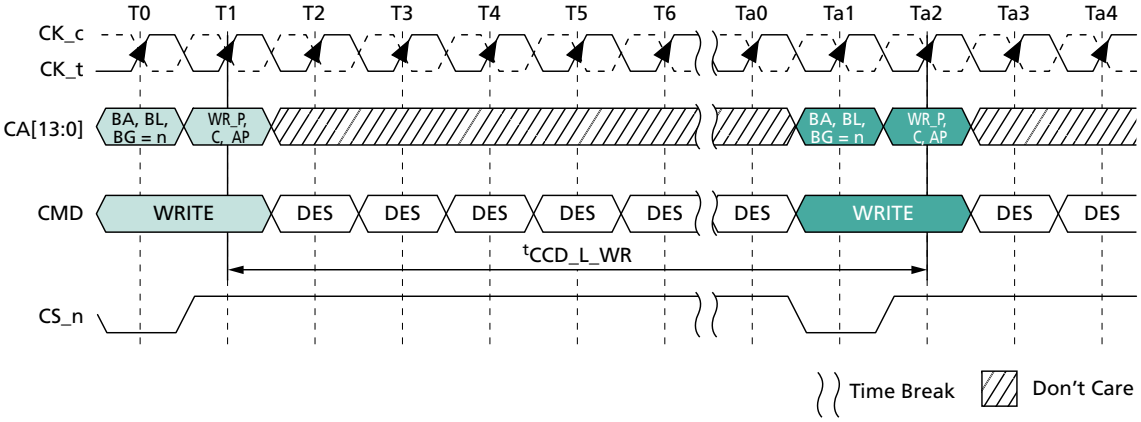
3. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.

Figure 40: Write-to-Write to Different Bank Group for BL16 in BL32 OTF



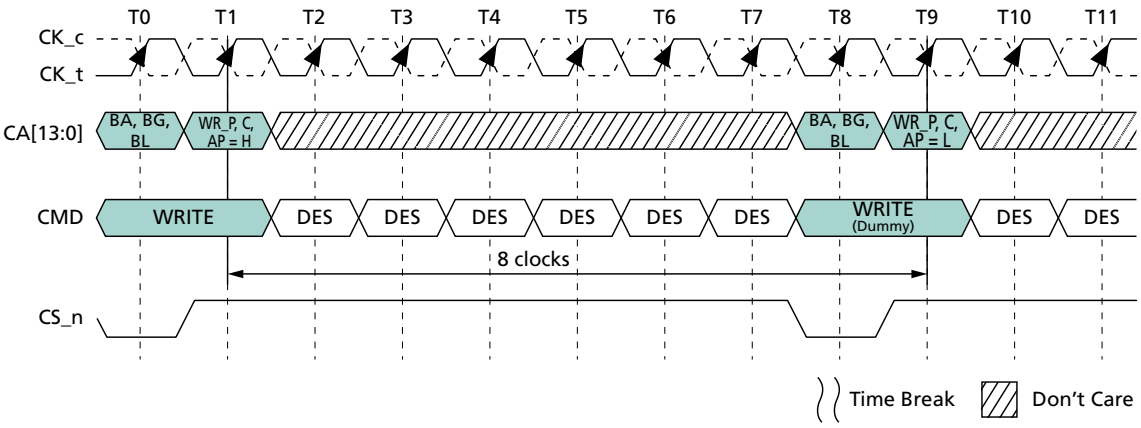
Notes: 1. Figure shows back-to-back BL16 writes to different bank groups.
2. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.

Figure 41: Write-to- Write to Same Bank Group for BL16 in BL32 OTF



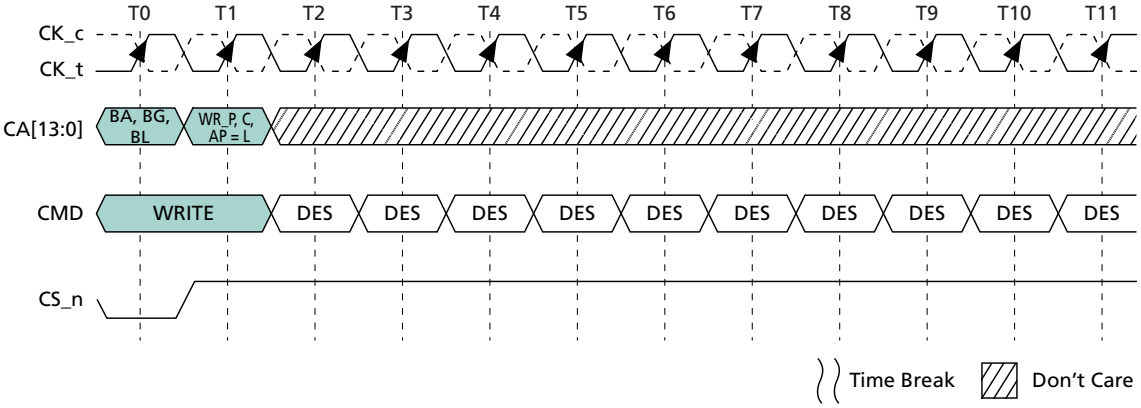
Notes: 1. Figure shows back-to-back BL16 writes to the same bank group using a timing of ^{t}CCD_L_WR.
2. Back-to-back BL32 writes to the same bank group have a minimum separation of 16 clocks.
3. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.

Figure 42: Write with Auto Precharge for Fixed BL32 and BL32 OTF



Notes: 1. The AP bit must be set HIGH for the first WRITE command and LOW for the dummy WRITE command.
2. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.
3. CA bits other than C10 and AP in dummy WRITE command are the same as the first WRITE command.

Figure 43: Write with Auto Precharge for BL16 in BL32 OTF Mode



Notes: 1. The AP bit must be set LOW with the WRITE command.
2. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.

Same Bank Group Write-to-Write Timings

DDR5 devices have different same bank group write-to-write timings, based on whether the second write requires read-modify-write (RMW) access or just-write (JW) access. In JW access, the device updates all 128 bits of data on the addressed codeword, while in RMW access, a part of 128 bits is updated.

Table 157: JW Access and RMW Access Definition

Configuration	BL16		BC8		Optional BL32	Notes
	Normal	Data Mask	Normal	Data Mask		
x4	RMW	-	RMW	-	JW	1,2,3
x8/x16	JW	RMW	RMW		-	1,2,3

Notes: 1. BC8 refers to BC8 OTF mode enabled by MR0 OP[1:0]=01 and WRITE command with BL=L issued.

2. Optional BL32 refers to BL32 fixed mode enabled by MR0 OP[1:0]=10 or BL32 OTF mode enabled by MR0 OP[1:0]=11 and WRITE command with BL=L issued.
3. Data mask refers to data mask mode enabled by MR5 OP[5]=1 and WRITE command with WP=L issued.

Table 158: Same Bank Group Write Access to RMW Access Timings

From	To		Notes
	BL16	BC8	
BL16	^{t}CCD_L_WR	^{t}CCD_L_WR	1,2,3
BC8	^{t}CCD_L_WR	^{t}CCD_L_WR	1,2,3
Optional BL32	8nCK+^{t}CCD_L_WR	-	1,2,3,4

Notes: 1. BC8 refers to BC8 OTF mode enabled by MR0 OP[1:0]=01 and WRITE command with BL=L issued.
2. Optional BL32 refers to BL32 fixed mode enabled by MR0 OP[1:0]=10 or BL32 OTF mode enabled by MR0 OP[1:0]=11 and WRITE command with BL=L issued.
3. With Optional BL32, this timing table is regarding the first command, not the dummy command.
4. There is no BL32 to BC8 case.

Table 159: Same Bank Group Write Access to JW Access Timings

From	To		Notes
	BL16	Optional 32	
BL16	^{t}CCD_L_WR2	^{t}CCD_L_WR2	1,2,3
BC8	^{t}CCD_L_WR2	-	1,2,3,4
Optional BL32	-	8nCK+^{t}CCD_L_WR2	1,2,3

Notes: 1. BC8 refers to BC8 OTF mode enabled by MR0 OP[1:0]=01 and WRITE command with BL=L issued.
2. Optional BL32 refers to BL32 fixed mode enabled by MR0 OP[1:0]=10 or BL32 OTF mode enabled by MR0 OP[1:0]=11 and WRITE command with BL=L issued.
3. With Optional BL32, this timing table is regarding the first command, not the dummy command.
4. There is no BL32 to BC8 case.

Different Bank Group Write-to-Write Timings

Table 160: Different Bank Group Write-to-Write Timings

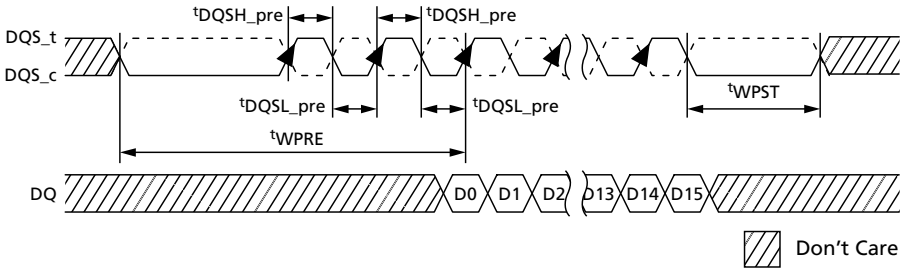
From	To			Notes
	BL16	BC8	Optional BL32	
BL16	8 nCK	8 nCK	8 nCK	1,2,3
BC8	8 nCK	8 nCK	–	1,2,3,4
Optional BL32	16 nCK	-	16 nCK	1,2,3,4

Notes: 1. BC8 refers to BC8 OTF mode enabled by MR0 OP[1:0]=01 and WRITE command with BL=L issued.
2. Optional BL32 refers to BL32 fixed mode enabled by MR0 OP[1:0]=10 or BL32 OTF mode enabled by MR0 OP[1:0]=11 and WRITE command with BL=L issued.
3. With Optional BL32, this timing table is regarding the first command, not the dummy command.
4. There is no BC8 to BL32 case (and vice versa).

Write Preamble Timings

During WRITE operations, the input receiver strobe with the DQ according to the preamble settings, and the strobe should meet the timing requirements (^{t}DQSH_pre, ^{t}DQSL_pre) to guarantee enough of a timing margin by setting the window for the strobe during the write preamble time frame. This timing requirement is applied to all configurations of write preamble set by MR8 OP[4:3], which is 2^{t}CK, 3^{t}CK, and 4^{t}CK write preamble, for write-to-write operations as well as the normal write operations.

Figure 44: DQS Timing While Write Preamble

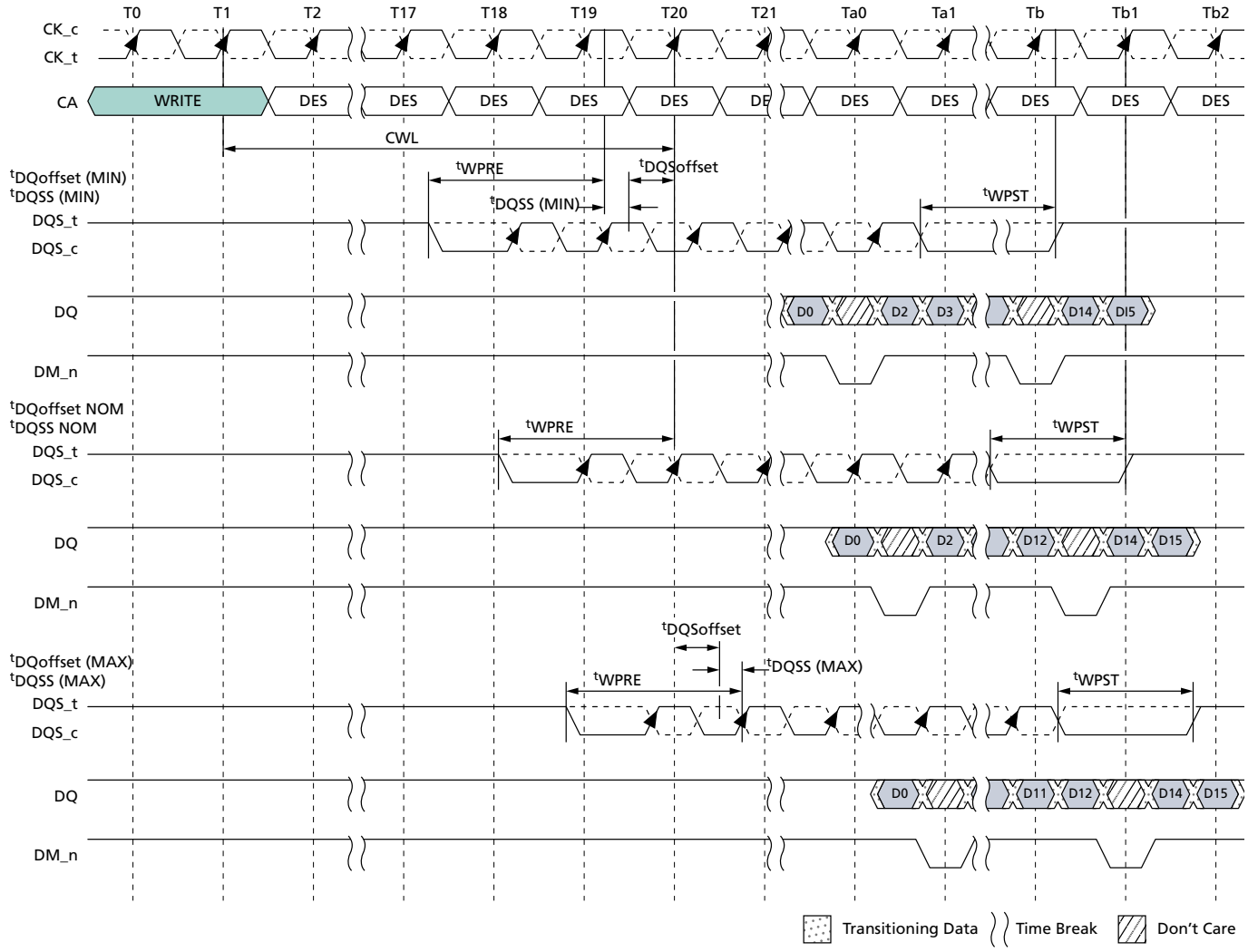


Notes: 1. BL=16; preamble = 4^{t}CK.
2. ^{t}DQSH_pre and^{t}DQSL_pre are shown and apply to all toggles during the preamble.
3. Second preamble during WRITE-to-WRITE operation follows the same requirements.

Write Timing Parameters

The following figure is for example only and illustrates the strobe edges for a particular WRITE burst. For a valid burst, all timing parameters for each edge of a burst must be satisfied.

Figure 45: Write Timing Parameters



Notes: 1. BL=16; preamble = 2^{t}CK - 0010 pattern; postamble = 1.5^{t}CK.
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. ^{t}DQSS must be met at each rising clock edge.
4. Example figure assumes device internal WL training is complete.
5. DQ/DM_n pulse timing and DQS to DQ skew defined by Rx strobe jitter sensitivity specifications for the respective speed bin.

tWPRE Calculation

The method for calculating differential pulse widths for tWPRE is shown in the figure below.

Figure 46: Method for Calculating tWPRE Transitions and Endpoints

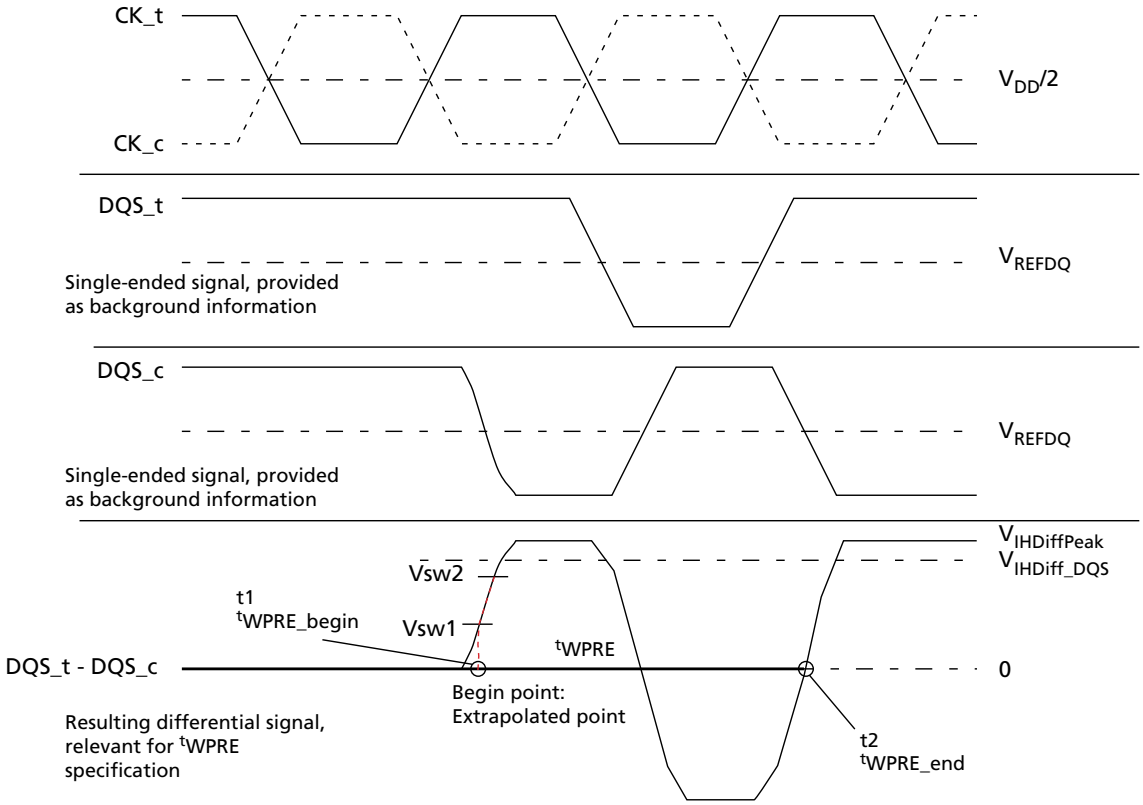


Table 161: Reference Voltage for tWPRE Timing Measurements

Measured Parameter	Measured Parameter Symbol	$V_{SW1[V]}$	$V_{SW2[v]}$	Notes
DQS_t, DQS_c differential WRITE Preamble	tWPRE	V_{IHDiff_DQS} x 0.1	V_{IHDiff_DQS} x 0.9	

tWPST Calculation

The method for calculating differential pulse widths for tWPST is shown in the figure below.

Figure 47: tWPST Calculation

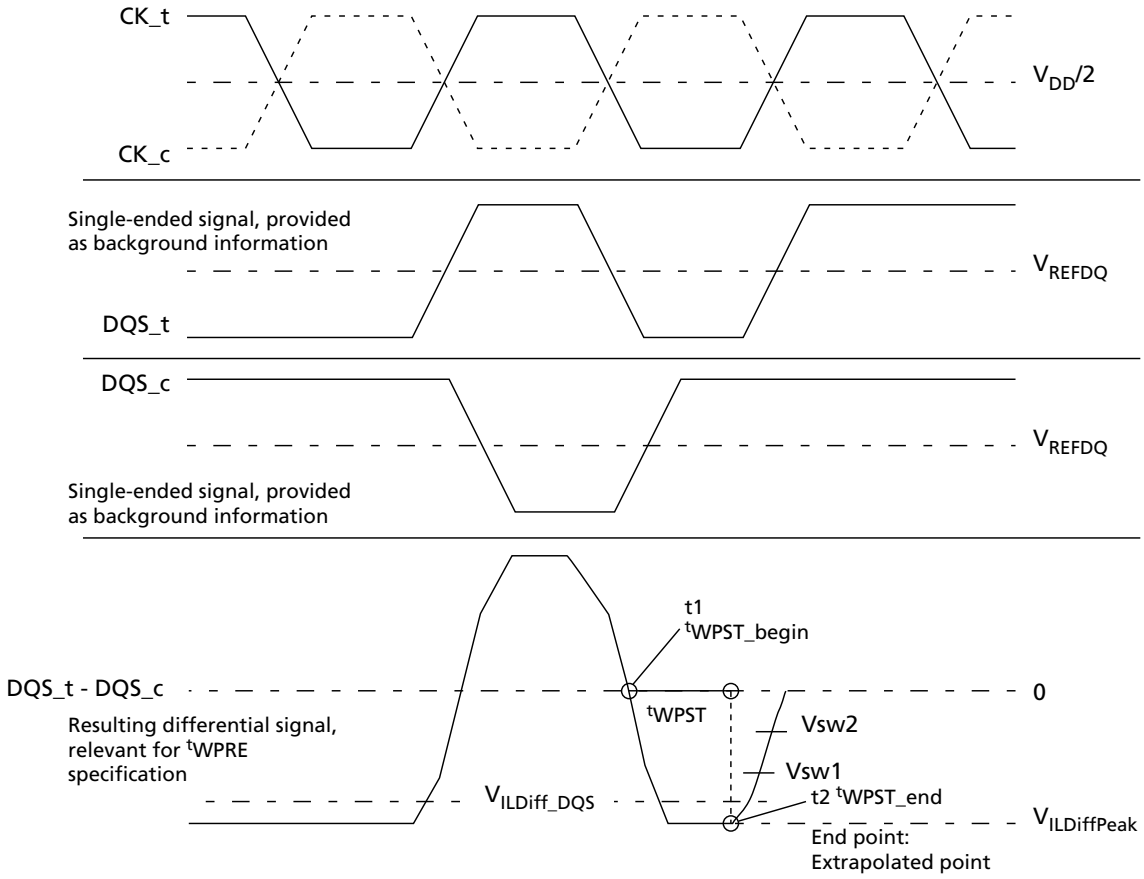


Table 162: Reference Voltage for tWPST Timing Measurements

Measured Parameter	Measured Parameter Symbol	$V_{SW1[V]}$	$V_{SW2[v]}$	Notes
DQS_t, DQS_c differential WRITE Postamble	tWPST	V_{IHDiff_DQS} x 0.9	V_{IHDiff_DQS} x 0.1	

Write Enable Timings

The following specifies the relationship between the write enable timing window ^{t}WPRE_EN_ntck and the DRAM-related DQS to CK drift window ^{t}DQSD, as well as the system-related DQS to CK drift window ^{t}DQSS around the final DQS to CK offset trained pass/fail point ^{t}DQSoffset, based on write-leveling feedback in order to support n-^{t}CK preamble mode. Functional operation requires that the following condition is met.

^{t}WPRE_EN_ntck ≥ |^{t}DQSS (MIN)| + ^{t}DQSS (MAX) + |^{t}DQSD (MIN)| + ^{t}DQSD (MAX)

Figure 48: ^{t}DQSS – External CLK-to-DQS Variation

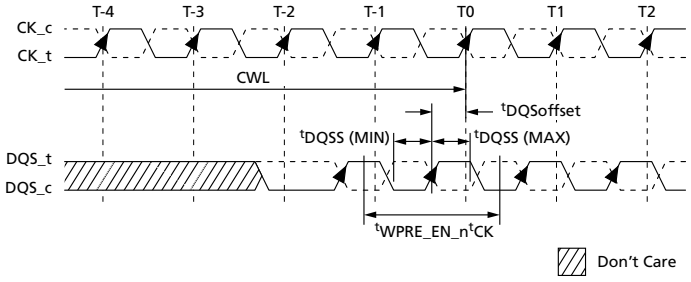
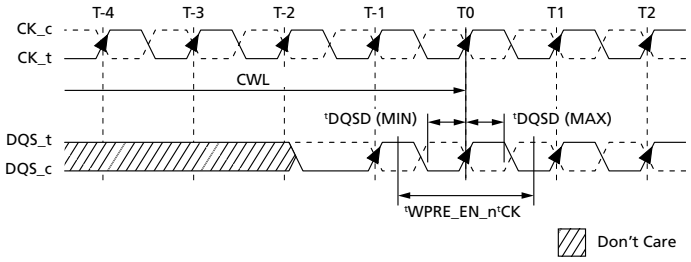


Figure 49: tDQSD – Internal CLK-to-DQS Variation



Module Rank and Channel Limitations for DIMMs During WRITE Operations

To achieve efficient module power supply design for JEDEC-standard DDR5 DIMMs, minimum timings as well as limitations in the number of DRAMs are provided for WRITE operations occurring on a single module. Additionally, since these modules are organized as two independent 36-bit or 40-bit channels (32 bits for non-ECC DIMMs), additional restrictions apply to limit localized power delivery noise on the module.

To provide best performance, the different channels may initiate commands on the same cycle provided the rank-to-rank timings are met, the maximum number of DRAMs in a given WRITE operation is not exceeded, and the applicable component timings shown elsewhere in this specification are met. Timing and operational relationships for DDR5 DIMMs are shown below.

Table 163: Module Rank and Channel Timings for DDR5 DIMMs

DIMM Configuration	Maximum Number of Die Simultaneous or Overlapping Activity	
	WRITE, WRITE-PATTERN	
	Die per Channel	Die per DIMM
SR x16	No restrictions	
DR x16	2	4
SR x8	No restrictions	

Table 163: Module Rank and Channel Timings for DDR5 DIMMs (Continued)

DIMM Configuration	Maximum Number of Die Simultaneous or Overlapping Activity	
	WRITE, WRITE-PATTERN	
	Die per Channel	Die per DIMM
DR x8	5	10
SR x4	No restrictions	
DR x4	10	20
DR x4 (2H 3DS)	10	20
DR x4 (4H 3DS)	10	20
DR x4 (8H 3DS)	10	20

Notes: 1. Any combination of commands, with up to the maximum of die per channel and per DIMM, per condition is allowed.
2. ^{t}CCD parameters must be met for WRITE and WRITE-PATTERN commands to different logical ranks or physical ranks within the same channel; no overlapping write data bus activity is allowed on two physical or logical ranks within the same channel.
3. WRITE and WRITE-PATTERN commands to different channels do not require stagger.
4. Each rank consists of one group of DRAMs making up a 36- or 40-bit channel (32 bits for non-ECC DIMMs).
5. Restrictions apply to some DIMMs built with certain lower power PMICs, but may not apply to DIMMs built with higher current capacity PMICs.

Write Timing Violations

Motivation

Generally, if write timing parameters are violated, a complete reset/initialization procedure has to be initiated to ensure the device works properly. However, for certain violations specified below, the device is guaranteed to not "hang up," and that errors are limited to that particular operation.

For the following, assume that there are no timing violations with regards to the WRITE command itself (including ODT, etc.) and that it does satisfy all timing requirements not mentioned below.

Data to Strobe Eye Height or Width Violations

If the required data to strobe timing or voltage parameters are violated (such as ^{t}Rx_DQ_^{t}Margin, ^{t}Rx_DQS2DQ, VRx_DQS, VRx_DQ, etc.), for any of the data/strobe timing edges or data/strobe voltage limits associated with a WRITE burst data eye, then incorrect data might be written to the memory locations addressed with this WRITE command.

In the example (Figure TBD), the relevant strobe edges for write burst A are associated with the clock edges: T_{n}, $T_{n+0.5}$, T_{n+1}, ... $T_{n+8.5}$.

Subsequent reads from that location might result in unpredictable read data; however, the device will work properly otherwise.

Strobe and Strobe to Clock Timing Violations

Should the strobe timing requirements (^{t}WPRE, ^{t}WPST) or the strobe to clock timing requirements (^{t}DQSS, ^{t}DQSoffset) be violated for any of the strobe edges associated with a WRITE burst, then wrong data might be written to the memory location addressed with the offending WRITE command.

Subsequent reads from that location might result in unpredictable read data; however, the DRAM will work properly otherwise with the following constraints:

1. Both write CRC and data burst OTF are disabled; timing specifications other than ^{t}WPRE, ^{t}WPST, ^{t}DQSS, ^{t}DQSoffset are not violated.
2. The offending write strobe (and preamble) arrive no earlier or later than six DQS transition edges from the write latency position.
3. A READ command following an offending WRITE command from any open bank is allowed.
4. One or more subsequent WR or a subsequent WRA {to same bank as offending WR} may be issued ^{t}CCD_L later but incorrect data could be written; subsequent WR and WRA can be either offending or non-offending writes. Reads from these writes may provide incorrect data.
5. One or more subsequent WR or a subsequent WRA {to a different bank group} may be issued ^{t}CCD_S later but incorrect data could be written; subsequent WR and WRA can be either offending or non-offending writes. Reads from these writes may provide incorrect data.
6. Once one or more precharge commands (PREpb, PREsb or PREab) are issued to device after offending WRITE command and all banks become precharged state (idle state), a subsequent, non-offending WR or WRA to any open bank shall be able to write correct data.
7. DQS strobes including preamble must align to each WRITE commands data burst length configuration. If the DRAM fails to capture or incorrectly de-serializes the incoming data stream because of misalignment or missing strobe edges, errors may occur. These errors will propagate indefinitely until the DRAM is put into an idle state, i.e., all banks are in the precharged state with ^{t}RP satisfied.

WRITE PATTERN and WRITE PATTERN AUTO PRECHARGE Commands

Because of the significant percentage of writes that contain all zeros, the WRITE PATTERN command is being included in the DDR5 specification.

The WRITE PATTERN (WRP) and WRITE PATTERN AUTO PRECHARGE (WRPA) commands can save power and improve performance by not actually sending a specific data pattern (such as all-zeros) across the external data bus.

These commands operate very similar to a standard WRITE (WR) or WRITE AUTO PRECHARGE (WRA) commands except for a few important differences: the data pattern written is the contents of MR48 instead of the data on the external DQ bus, toggling of DQ and DQS is therefore unnecessary, and the device does not turn on internal ODT. ECC parity is based on the write pattern mode data in MR48.

Upon receiving the WRP or WRPA command, the device sources the input for the memory array from the write pattern mode registers instead of from the DQs. The DQ mapping across the burst is shown the Write Pattern DQ Output Mapping table that follows. The host does not send any data during this time.

All timing constraints are still measured from the clocks where the WRITE command data would have transferred. For example, ^{t}WR is measured from the end of the write burst to the PRE command (shown in the WRITE PATTERN command example figure that follows).

The pattern used for this mode is in defined by the contents of MR48:OP[7:0]. That pattern can be all zeros, all ones, or something else, and can be changed with a MRW command to MR48. The power-on default for this mode register is all zeros. The WRP and WRPA commands support burst lengths of BL16 and BL32, and do not support BC8 OTF or BC32 OTF.

Table 164: Write Pattern Mode Register

MR Address	Write Pattern	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
48	UI	V	V	V	V	V	V	V	V

Notes: 1. OP[7:0] can be independently programmed with either 0 or 1.
2. Default MR48:OP[7:0] = 0000 0000b.
3. If CRC is enabled, ALERT_n is not issued from the device during write pattern mode and ^{t}CCD_S = 9 ^{t}CK should be satisfied.

The table that follows details how the pattern stored in MR48 will be mapped in the device array across the DQ bits and burst. The pattern is described as follows:

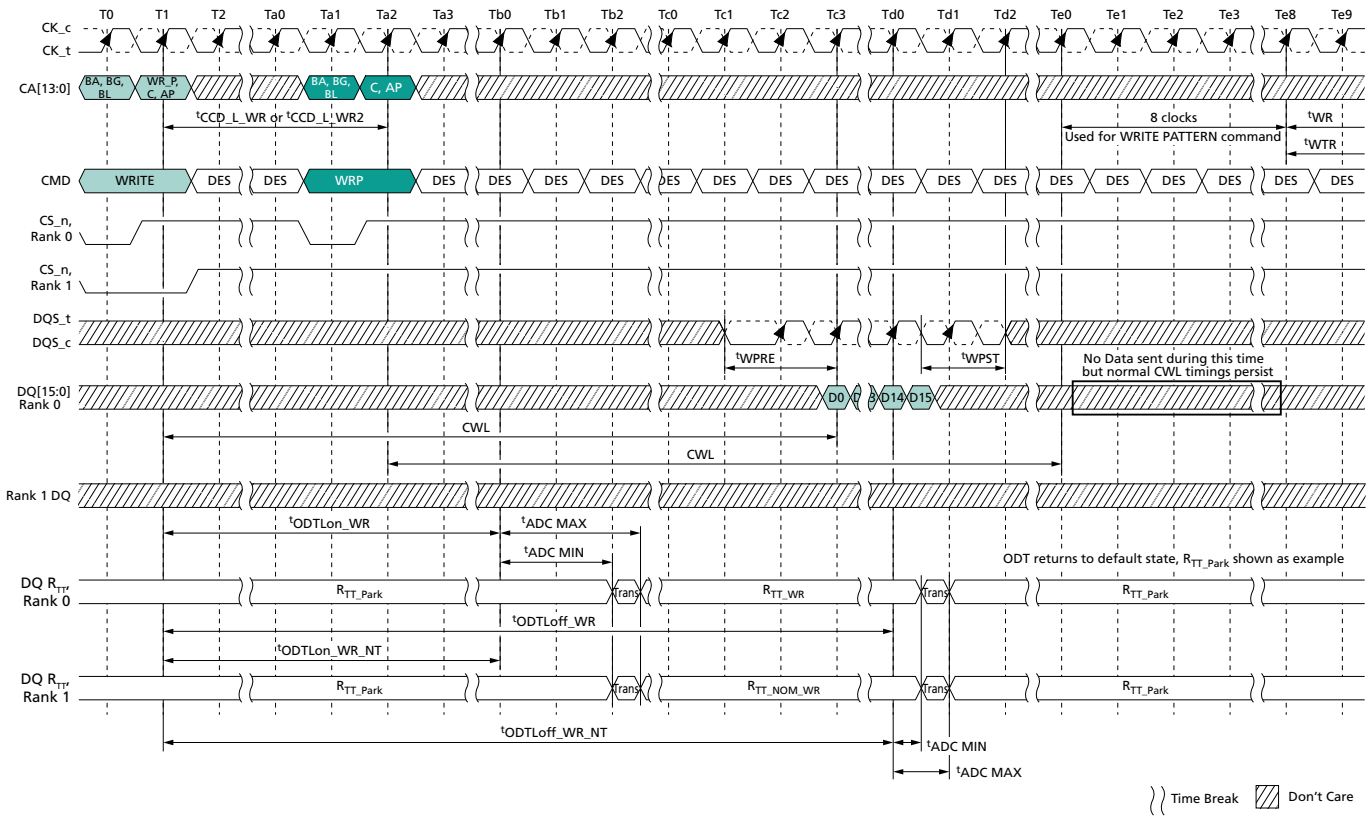
- In the case of a x4 device, only OP[3:0] is used with each bit of pattern corresponding to DQ[3:0], respectively. The same OP value is repeated over the entire burst for that bit (DQ0 stores OP0 on every UI of the burst). Although OP[7:4] are not used for the x4 device, the previously programmed MRW values are still read during a MRR (OP[7:4] does not revert to the default 0).
- In the case of a x8 device, the whole pattern OP[7:0] is used, with each bit of the pattern corresponding to DQ[7:0], respectively. The same OP[7:0] pattern is repeated over the entire burst for that bit. (DQ0 stores OP0 on every UI of the burst.)
- In the case of a x16 device, the whole pattern OP[7:0] is used, with each bit of the pattern corresponding to DQ[7:0], respectively, and then that pattern is repeated for DQ[15:8]. The same OP[7:0] pattern is repeated over the entire burst for that bit (DQ0 store OP0 on every UI of the burst).

The BL supported in write pattern mode is based on MR0:OP[1:0]; however WRP and WRPA do not support on-the-fly (OTF), limiting the choice to either fixed BL16 or BL32.

Table 165: Write Pattern DQ Output Mapping

Config	BL16 x16	BL16 x8	BL16 x4	BL32 x4
UI	0–15	0–15	0–15	0–31
DQ0	OP0	OP0	OP0	OP0
DQ1	OP1	OP1	OP1	OP1
DQ2	OP2	OP2	OP2	OP2
DQ3	OP3	OP3	OP3	OP3
DQ4	OP4	OP4	–	–
DQ5	OP5	OP5	–	–
DQ6	OP6	OP6	–	–
DQ7	OP7	OP7	–	–
DQ8	OP0	–	–	–
DQ9	OP1	–	–	–
DQ10	OP2	–	–	–
DQ11	OP3	–	–	–
DQ12	OP4	–	–	–
DQ13	OP5	–	–	–
DQ14	OP6	–	–	–
DQ15	OP7	–	–	–
DML_n/DML_n	INVALID	INVALID	–	–
DMU_n	INVALID	–	–	–

Figure 50: Example of WRITE PATTERN Command



Note: 1. See the JW Access and RMW Access Definition Table for guidance.

READ Operations

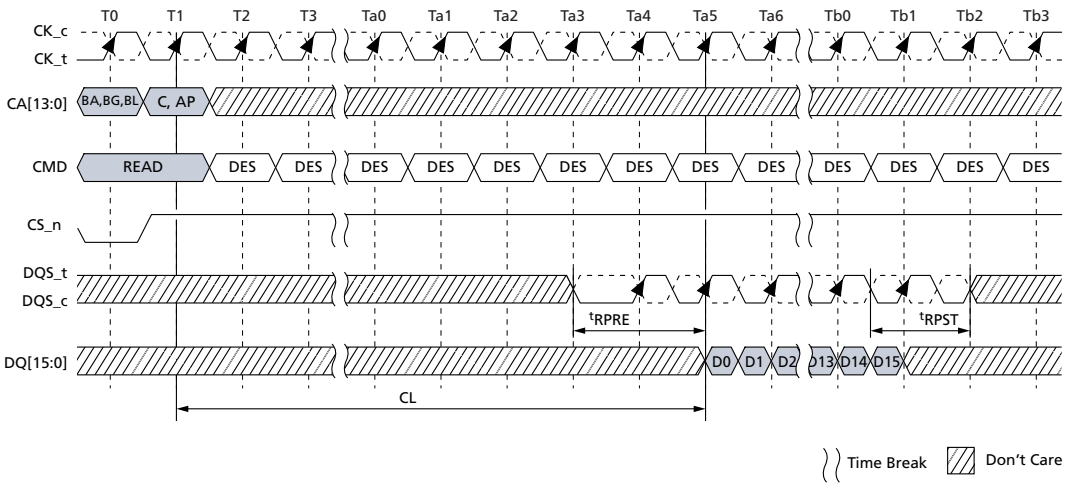
The READ operation causes the device to retrieve and output data stored in its array. The READ operation is initiated by the READ command during which the beginning column address and bank/ group address for the data to be retrieved from the array is provided. The retrieved data is driven on to the DQ pins CL cycles after the READ command along with the proper waveform on the DQS inputs. CL is defined from the READ command to data and is not affected by the read DQS offset timing (MR40 OP[2:0]).

In these read timing diagrams, for clarity of illustration, CK and DQS are shown aligned. As well, DQS and DQ are shown center-aligned. Offset between CK and DQS, and between DQS and DQ may be approximate.

READ Burst Operation

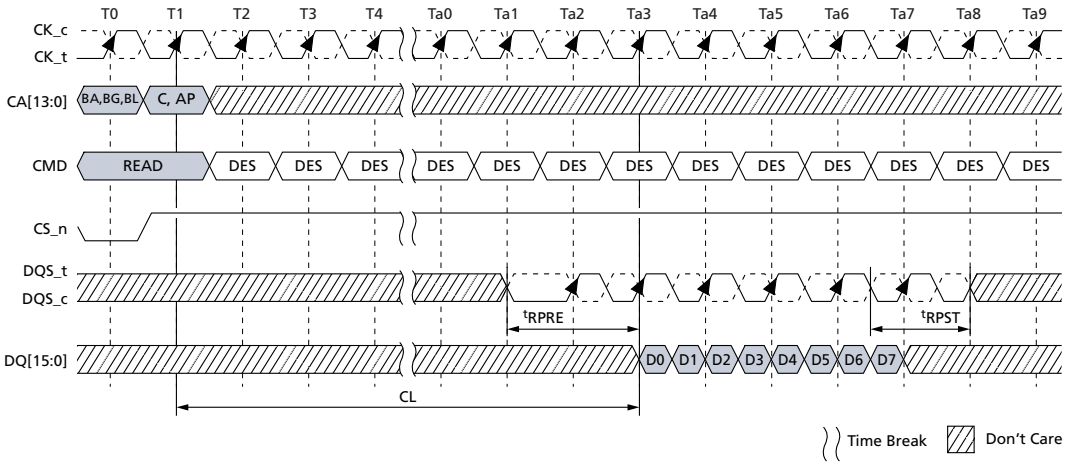
The device supports BL16, BC8 OTF, BL32 (optional), or BL32 OTF (optional) during the READ or WRITE command (auto precharge can be enabled or disabled based on the state of the CA10 pin during the 2nd cycle of the command). MR0[1:0] is used to select BL16, BC8 OTF, BL32 OTF, or BL32 operation mode.

Figure 51: READ Burst Operation (BL16)



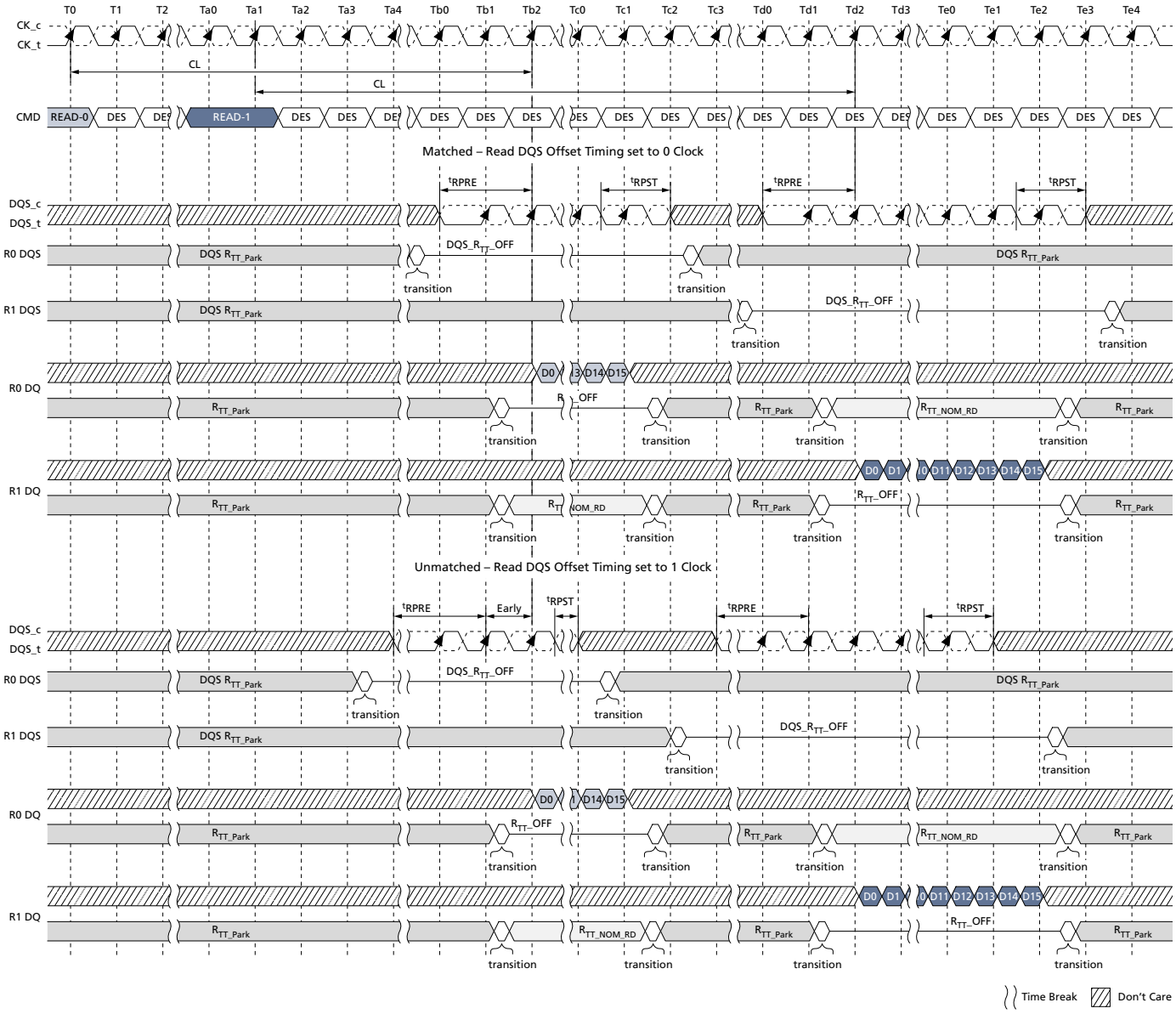
Notes: 1. BL = 16; preamble = 2^{t}CK 0010 pattern; postamble = 1.5^{t}CK.
2. Dn = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. In this example, read DQS offset timing is set to 0 clocks.

Figure 52: READ Burst Operation (BC8 OTF)



Notes: 1. BL = 8; preamble = 2^{t}CK 0010 pattern; postamble = 1.5^{t}CK.
2. Dn = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. In this example, read DQS offset timing is set to 0 clocks.
5. In non-CRC mode, DQS_t and DQS_c stop toggling at the completion of the BC8 data bursts, plus the postamble.

Figure 53: READ to READ, Different Ranks Operation With Read DQS Offset Usage (BL16)



Notes: 1. BL = 16; preamble = 2^{t}CK 0010 pattern; postamble = 1.5^{t}CK.
2. Dn = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. Two different examples are shown side by side: The top with the default setting for read DQS offset = 0 clocks; the lower with a 1 clock setting. In the lower case, the DQS is started 1 clock earlier than normal with respect to CL. In both cases, the data does not move.

Burst READ Operation Followed by a Precharge

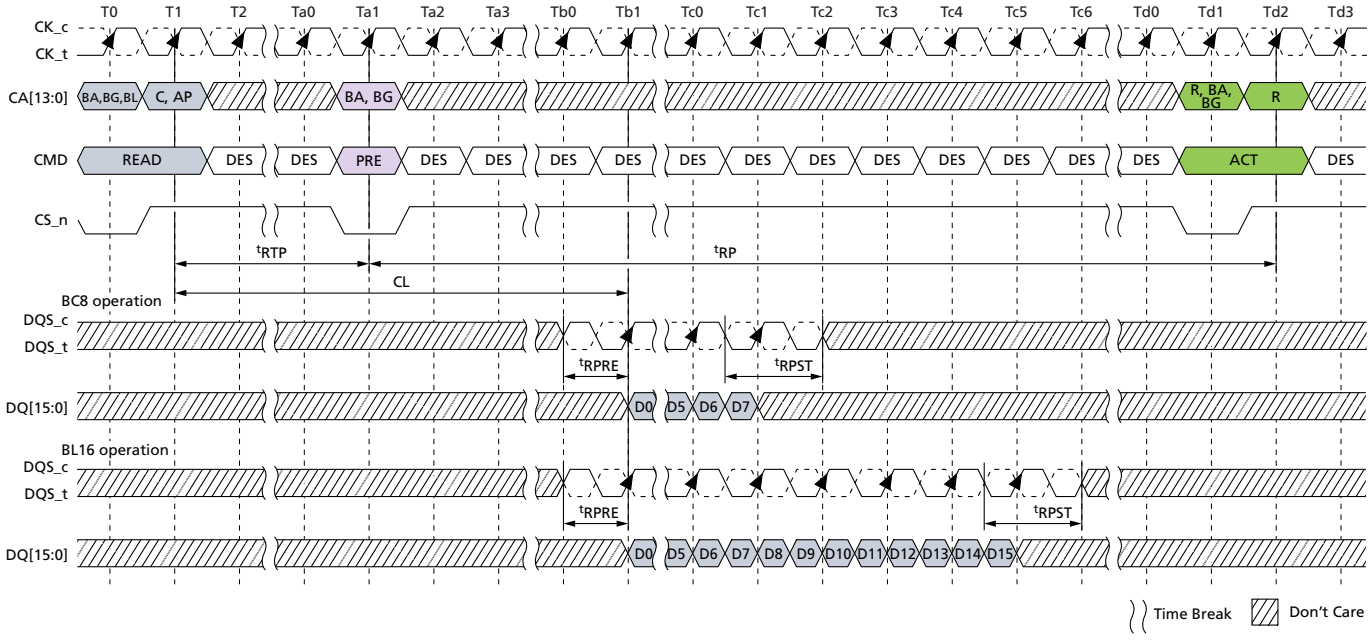
The minimum external READ command to PRECHARGE command spacing to the same bank is equal to ^{t}RTP with ^{t}RTP being the internal READ command to PRECHARGE command delay. Note that the minimum ACT to PRE timing, ^{t}RAS, must be satisfied as well. The minimum value for the internal READ command to PRECHARGE command delay is given by ^{t}RTP,min. A new bank ACTIVE command may be issued to the same bank if the following two conditions are satisfied simultaneously:

The minimum RAS precharge time (^{t}RP,min) has been satisfied from the clock at which the precharge begins.

The minimum RAS cycle time (^{t}RC,min) from the previous bank activation has been satisfied.

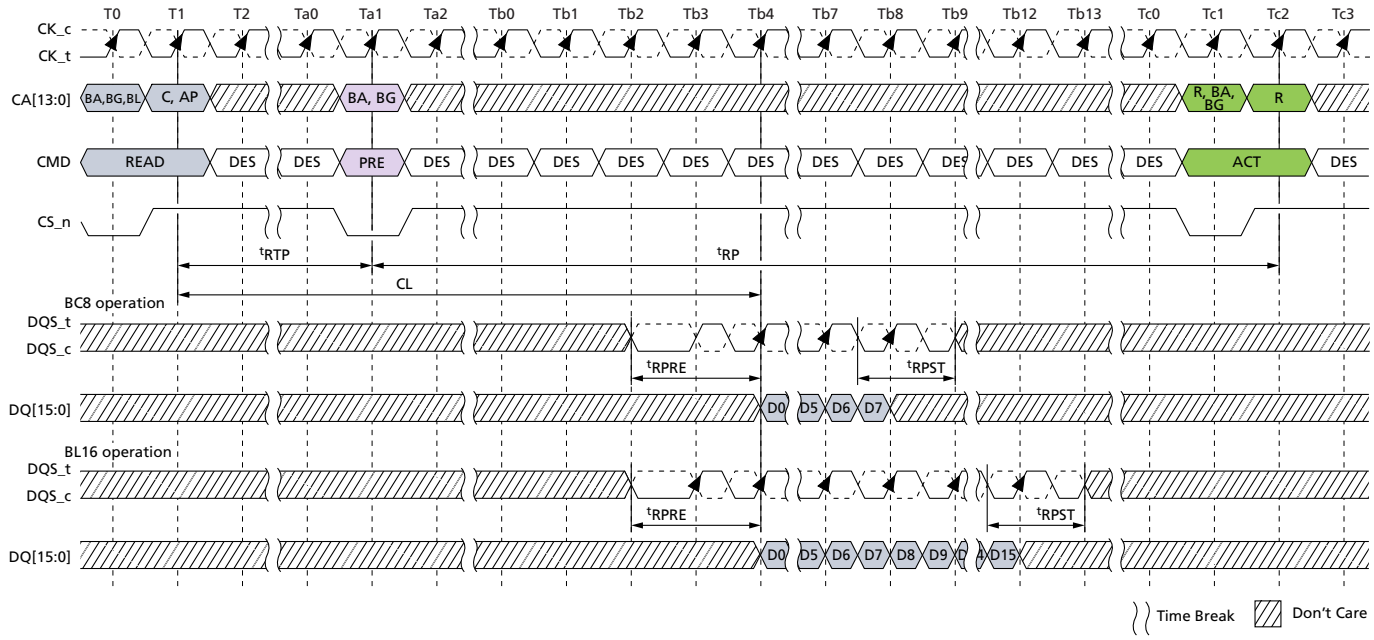
Examples of READ commands followed by precharge are shown below.

Figure 54: READ to PRECHARGE, With 1^{t}CK Preamble



Notes: 1. BL = 16; preamble = 1^{t}CK; postamble = 1.5^{t}CK.
2. Dn = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes ^{t}RAS,min is satisfied at PRECHARGE command time (^{t}a1) and that ^{t}RC,min is satisfied at the next ACTIVE command time (^{t}d2).

Figure 55: READ to PRECHARGE, With 2tCK Preamble



Notes: 1. BL = 16; preamble = 2tCK 0010 pattern; postamble = 1.5tCK.
2. Dn = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumestRAS,min is satisfied at PRECHARGE command time (ta1) and thattRC,min is satisfied at the next ACTIVE command time (td2).

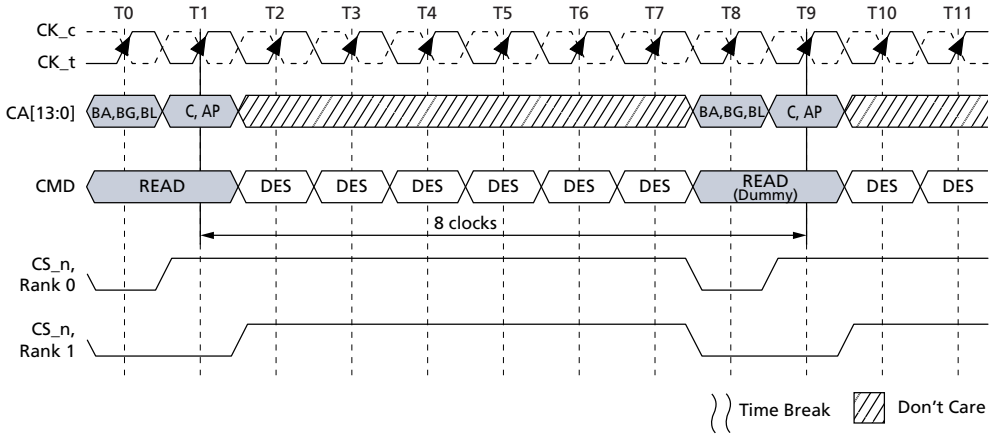
READ Burst Operation for Optional BL32 Mode

The following read timing diagrams cover read timings for fixed BL32, BL32 in BL32 OTF mode, and BL16 in BL32 OTF mode for x4 devices only.

In these read timing diagrams, for clarity of illustration, CK and DQS are shown aligned. As well, DQS and DQ are shown center-aligned. Offset between CK and DQS, and between DQS and DQ may be appropriate.

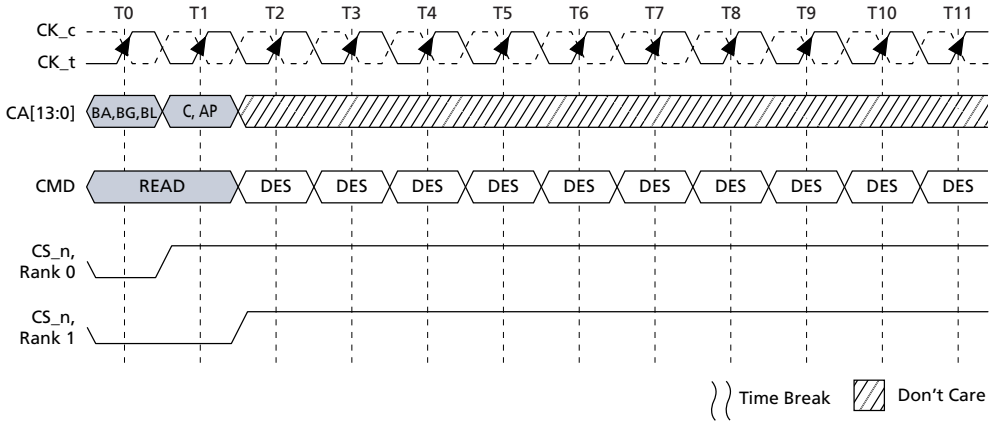
A dummy READ command is required for the second half of the transfer of BL32. If non-target ODT is needed in the system, then a dummy ODT command must be issued to the non-target rank for the second half of the transfer of BL32.

Figure 56: Read Timing for Fixed BL32 and BL32 in BL32 OTF Mode



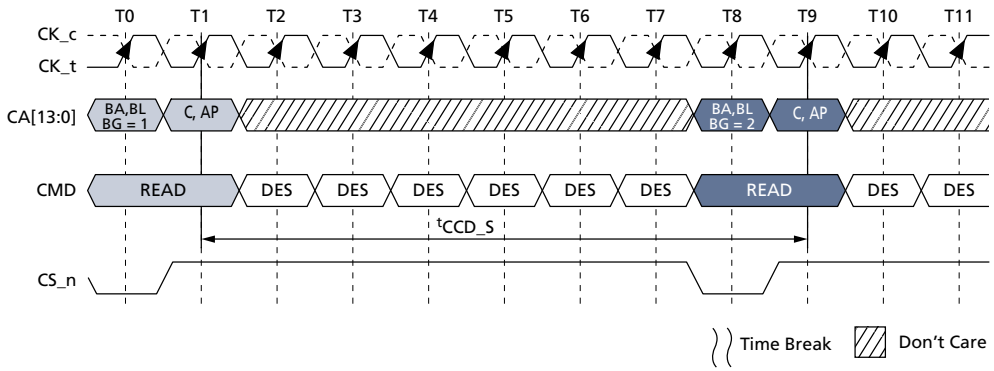
Notes: 1. DES commands are shown for ease of illustration; other commands may be valid at these times.
2. A dummy READ command is required for the second half of the transfer with a delay of 8 clocks from the first READ command.
3. The figure also shows a dummy ODT command being issued to non-target rank 1 for the second half of the transfer.
4. C10 is used for burst ordering and can be LOW or HIGH for the first READ command. C10 for the dummy READ command must be the opposite value from the first READ command.
5. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.
6. CA bits other than C10 and AP in the dummy READ command are the same as the first READ command.

Figure 57: READ Timing for BL16 in BL32 OTF Mode



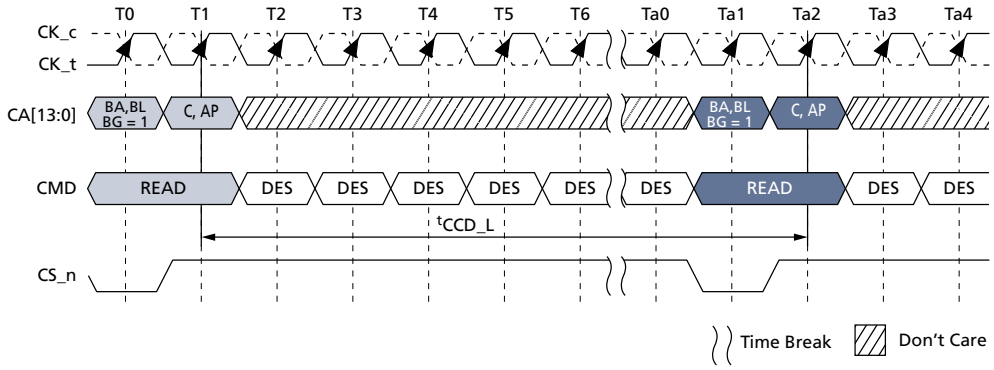
Notes: 1. The figure shows BL16 READ operation when MR0 is programmed to use BL32 OTF mode. In this case, no dummy READ command is required as transfer size is BL16.
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.

Figure 58: READ to READ to Different Bank Group for BL16 in BL32 OTF



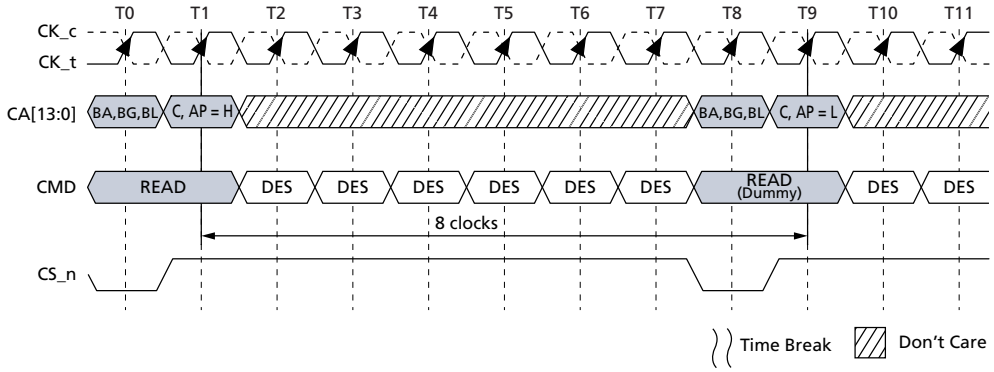
Notes: 1. The figure shows back-to-back BL16 reads to different bank groups.
2. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.

Figure 59: READ to READ to Same Bank Group for BL16 in BL32 OTF



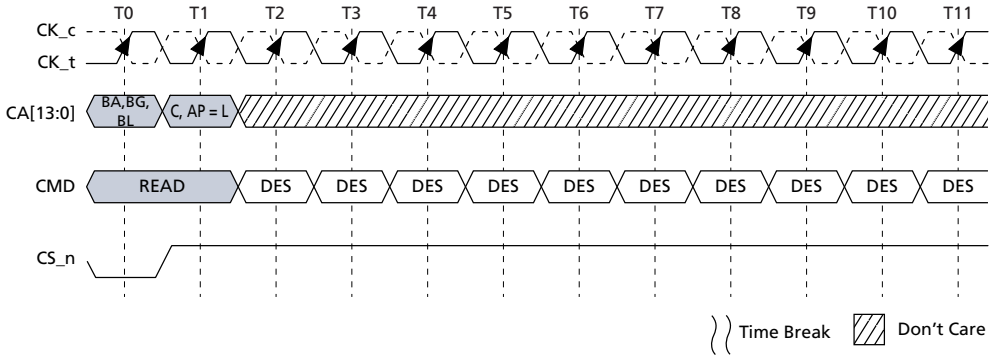
Notes: 1. The figure shows back-to-back BL16 reads to same bank group using a timing of ^{t}CCD_L..
2. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.

Figure 60: READ to READ With Auto Precharge for Fixed BL32 and BL32 in BL32 OTF Mode



Notes: 1. AP bit must be set HIGH for first READ command and LOW for dummy READ command.
2. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.
3. CA bits other than C10 and AP in dummy READ command are the same as the first READ command.

Figure 61: READ With Auto Precharge for BL16 in BL32 OTF Mode



Notes: 1. AP bit must be set LOW with the READ command.
2. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.

READ and WRITE Command Interval

READ to WRITE as well as WRITE to READ command interval timing requirements are described in the following tables.

Table 166: Minimum READ and WRITE Command Timings (3200-6400)

Bank Group	Parameter (MIN)	DDR5 - 3200 - 6400	Notes
Same	READ-to-WRITE	CL - CWL + RBL/2 + 2^{t}CK - (Read DQS offset) + (^{t}RPST - 0.5^{t}CK) +^{t}WPRE	1, 3, 4
	WRITE-to-READ	CWL + WBL/2 +^{t}WTR_L	2, 4, 5
	WRITE-to-READ AP, same bank	CWL + WBL/2 +^{t}WTRA	2, 4, 6
Different	READ-to-WRITE	CL - CWL + RBL/2 + 2^{t}CK - (Read DQS offset) + (^{t}RPST - 0.5^{t}CK) +^{t}WPRE	1, 3, 4
	WRITE-to-READ	CWL + WBL/2 + ^{t}WTR_S	2, 4

Notes: 1. RBL: Read burst length associated with READ command:
   1. RBL = 32 (36 with RCR on) for fixed BL32 and BL32 in BL32 OTF mode
   2. RBL = 16 (18 with RCRC on) for fixed BL16 and BL16 in BL32 OTF mode
   3. RBL = 16 (18 with RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

2. WBL: Write burst length associated with WRITE command:
   1. WBL = 32 (36 w/ WCRC on) for fixed BL32 and BL32 in BL32 OTF mode
   2. WBL = 16 (18 w/ WCRC on) for fixed BL16 and BL16 in BL32 OTF mode
   3. WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

3. The following is considered for ^{t}RTW equation:
   1. 1^{t}CK needs to be added due to ^{t}DQSoffset
   2. Read DQS offset timing can pull in the ^{t}RTW timing
   3. 1^{t}CK needs to be added when using 1.5^{t}CK postamble

4. CWL = CL - 2.
5. ^{t}WTRA must be satisfied instead of ^{t}WTR_L for same bank access when read with auto precharge.
6. ^{t}WTRA = ^{t}WR -^{t}RTP, allows the precharge generated by the read with auto precharge to meet ^{t}WR from the preceding write when it occurs within the same bank.

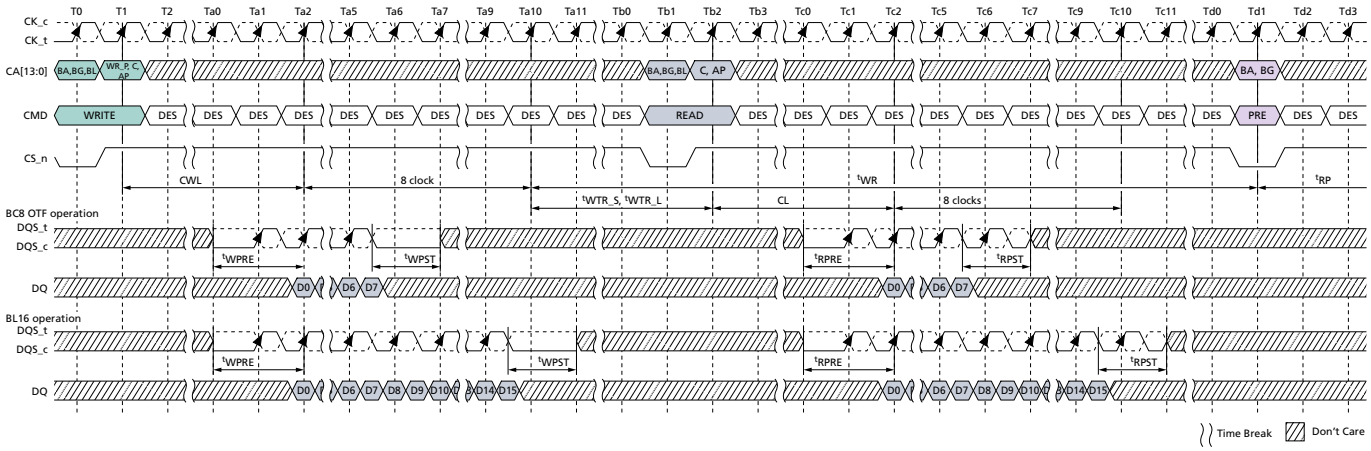
Table 167: Minimum READ and WRITE Command Timings (6800-8800)

Bank Group	Parameter (MIN)	DDR5 - 6800-8800	Notes
Same	READ-to-WRITE	TBD	1, 3, 4
	WRITE-to-READ	TBD	2, 4, 5
	WRITE-to-READ AP, same bank	TBD	2, 4, 6
Different	READ-to-WRITE	TBD	1, 3, 4
	WRITE-to-READ	TBD	2, 4

Notes: 1. RBL: Read burst length associated with READ command:
   1. RBL = 32 (36 with RCR on) for fixed BL32 and BL32 in BL32 OTF mode
   2. RBL = 16 (18 with RCRC on) for fixed BL16 and BL16 in BL32 OTF mode
   3. RBL = 16 (18 with RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

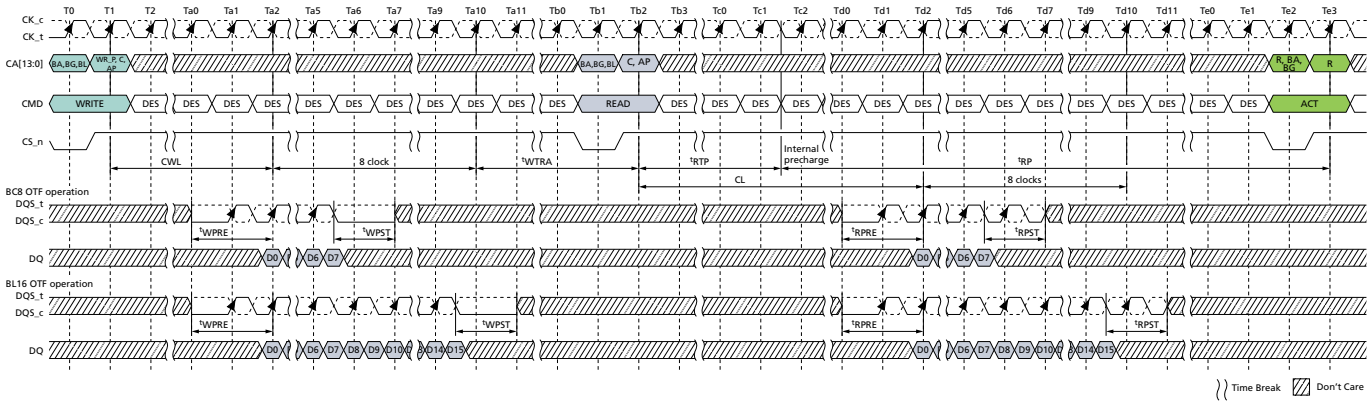
2. WBL: Write burst length associated with WRITE command:
    1. WBL = 32 (36 w/ WCRC on) for fixed BL32 and BL32 in BL32 OTF mode
    2. WBL = 16 (18 w/ WCRC on) for fixed BL16 and BL16 in BL32 OTF mode
    3. WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
3. The following is considered for ^{t}RTW equation:
    1. 1^{t}CK needs to be added due to ^{t}DQSoffset
    2. Read DQS offset timing can pull in the ^{t}RTW timing
    3. 1^{t}CK needs to be added when using 1.5^{t}CK postamble
4. CWL = CL - 2.
5. ^{t}WTRA must be satisfied instead of ^{t}WTR_L for same bank access when read with auto precharge.
6. ^{t}WTRA = ^{t}WR -^{t}RTP, allows the precharge generated by the read with auto precharge to meet ^{t}WR from the preceding write when it occurs within the same bank.

Figure 62: WRITE to READ Timing



Notes: 1. BC OTF = 8 or BL = 16; preamble = 2^{t}CK - 0010 pattern; postamble = 1.5^{t}CK.
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. The write recovery time (^{t}WR) is referenced from the first rising clock edge after the last write data shown at Ta10. ^{t}WR specifies the last burst write cycle until the PRECHARGE command can be issued to the same bank.

Figure 63: WRITE to READ With Auto Precharge in the Same Bank Timing



Notes: 1. BC OTF = 8 or BL = 16; preamble = 2^{t}CK - 0010 pattern; postamble = 1.5^{t}CK.

2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. The write recovery time (^{t}WR) is referenced from the first rising clock edge after the last write data shown at Ta10. The internal precharge after the read with auto precharge cannot begin before ^{t}WR is satisfied, which is equivalent to ^{t}WTRA + ^{t}RTP.

READ and WRITE Command Interval for Optional BL32 Modes

READ to WRITE as well as WRITE to READ command interval timing requirements for BL32 modes of operation are described in the following tables.

Table 168: Minimum READ to READ Command Timings – Same Bank Group

From	To		Notes
	BL16 in BL32 OTF Mode	BL32 to BL32 OTF Mode	
BL16 in BL32 OTF mode	^{t}CCD_L	^{t}CCD_L	1
BL32 in BL32 OTF mode	16 clocks	16 clocks	1

Notes: 1. The device supports an optional fixed BL32 mode and optional OTF mode for x4 devices only.

Table 169: Minimum READ to READ Command Timings – Different Bank Group

From	To		Notes
	BL16 in BL32 OTF Mode	BL32 to BL32 OTF Mode	
BL16 in BL32 OTF mode	^{t}CCD_S	^{t}CCD_S	1
BL32 in BL32 OTF mode	16 clocks	16 clocks	1

Notes: 1. The device supports an optional fixed BL32 mode and optional OTF mode for x4 devices only.

Table 170: Minimum WRITE to WRITE Command Timings – Same Bank Group

From	To		Notes
	BL16 in BL32 OTF Mode	BL32 to BL32 OTF Mode	
BL16 in BL32 OTF mode	^{t}CCD_L_WR	^{t}CCD_L_WR	1
BL32 in BL32 OTF mode	TBD	TBD	1

Notes: 1. The device supports an optional fixed BL32 mode and optional OTF mode for x4 devices only.

Table 171: Minimum WRITE to Write Command Timings – Different Bank Group

From	To		Notes
	BL16 in BL32 OTF Mode	BL32 to BL32 OTF Mode	
BL16 in BL32 OTF mode	^{t}CCD_S	^{t}CCD_S	1
BL32 in BL32 OTF mode	16 clocks	16 clocks	1

Notes: 1. The device supports an optional fixed BL32 mode and optional OTF mode for x4 devices only.

READ Command Timing Definitions

Read timing shown in this section is applied when the DLL is enabled and locked.

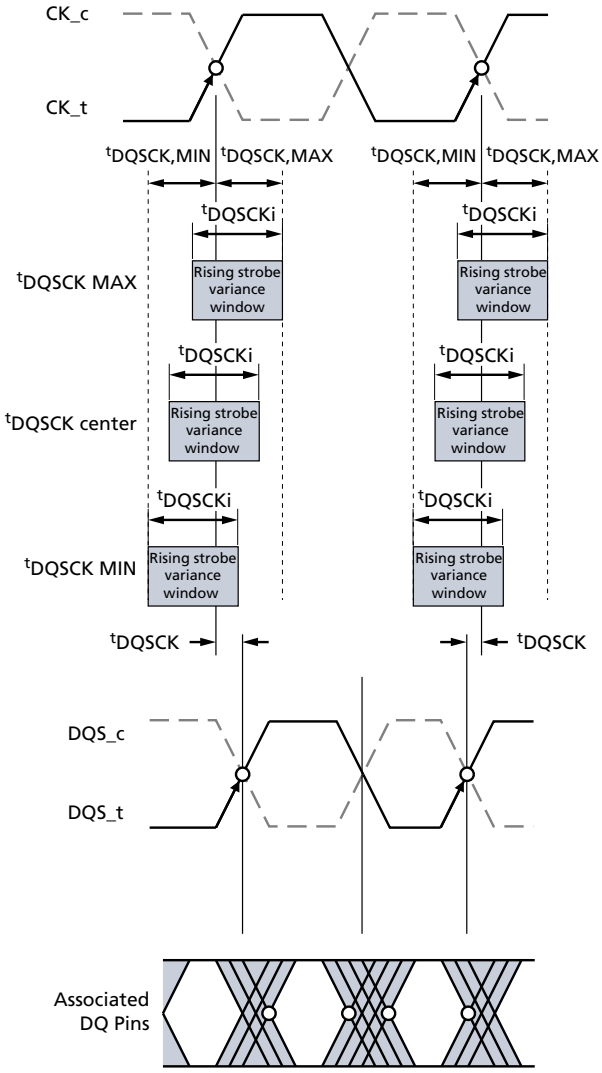
Rising data strobe edge parameters:

- ^{t}DQSCK,MIN/MAX describes the allowed range for a rising data strobe edge relative to CK_t, CK_c
- ^{t}DQSCK is the actual position of a rising strobe edge relative to CK_t, CK_c

^{t}DQSCK,MIN limit = Earliest of {^{t}DQSCKi at any valid V_{DD} and temperature, all DQS pairs and parts}.

^{t}DQSCK,MAX limit = Latest of {^{t}DQSCKi at any valid V_{DD} and temperature all DQS pairs and parts}.

Figure 64: ^{t}DQSCK Timing Definition



Temperature Sensor

The device features a temperature sensor whose status (MR4:OP[2:0]) can be read to determine the minimum required refresh rate. The temperature sensor read-out or the device T_{OPER} may be used to determine whether the refresh rate and operating temperature requirements are being met. Additionally, the device's temperature status (MR4:OP[2:0]) can be read by the system to determine the current approximate temperature range sensed by the device.

The device monitors device temperature and updates MR4 according to ^{t}TSI. Upon completion of device initialization, the device temperature status bits will be no older than ^{t}TSI. MR4 is updated even when the device is in the self refresh state.

When using the temperature sensor, an actual device case temperature (T_{CASE}) measurement may be higher than the T_{OPER} specification that applies to standard or elevated temperature ranges, as long as the temperature sensor readings remain within range. For example, T_{CASE} may be above 85°C when MR4:OP[2:0]=010b, as long as the sensor readings remain at or below 85°C. The device allows for a 2°C temperature margin between the point at which the device updates the MR4 value and the point at which the controller reconfigures the system accordingly.

When MR4:OP[5]=0 (wide range temperature sensor not supported), the four thresholds of the temperature sensor will be nominally 80°C, 85°C, 90°C and 95°C.

The second threshold (nominally 85°C) should be used by the system to switch to 2X refresh. The fourth threshold (nominally 95°C) should be used to throttle activity/traffic to keep the device at a safe operating temperature. The first threshold (nominally 80°C) allows the system to take actions to avoid reaching the second threshold. The third threshold (nominally 90°C) allows the system to take actions to avoid reaching the fourth threshold.

When MR4:OP[5]=1 (optional wide range extended temperature sensor range supported), the six thresholds of the temperature sensor will be nominally 75°C, 80°C, 85°C, 90°C, 95°C, and 100°C. The third threshold (nominally 85°C) is used by the system to switch to 2X refresh. The fifth threshold (nominally 95°C) is used by the system to throttle activity to keep the device at a safe operating temperature. The sixth threshold (nominally 100°C) is used by the system to perform emergency actions such as forcing the system to power down. Support for temperature sensor readings above 95°C does not imply thatthe device may operate properly above 95°C. Side effects may include loss of data integrity.

To ensure proper operation using the temperature sensor, consider the following factors:

- TempGradient is the maximum temperature gradient experienced by the device at the temperature of interest over a range of 2°C.
- ReadInterval is the time period between MR4 reads from the system.
- TempSensorInterval (^{t}TSI) is the maximum delay between internal updates of MR4.
- SysRespDelay is the maximum time between a read of MR4 and the response by the system.

To determine the required frequency of polling MR4, use the maximum TempGradient and the maximum response time of the system using the following equation:

TempGrandient x (ReadInterval + ^{t}TSI + SysRespDelay) ≤ 2°C

Table 172: Temperature Sensor Parameters

Parameter	Symbol	MIN/MAX	Value	Unit	Notes
System Temperature Gradient	TempGradient	MAX	System-dependent	°C/s	
MR4 Read Interval	ReadInterval	MAX	System-dependent	ms	

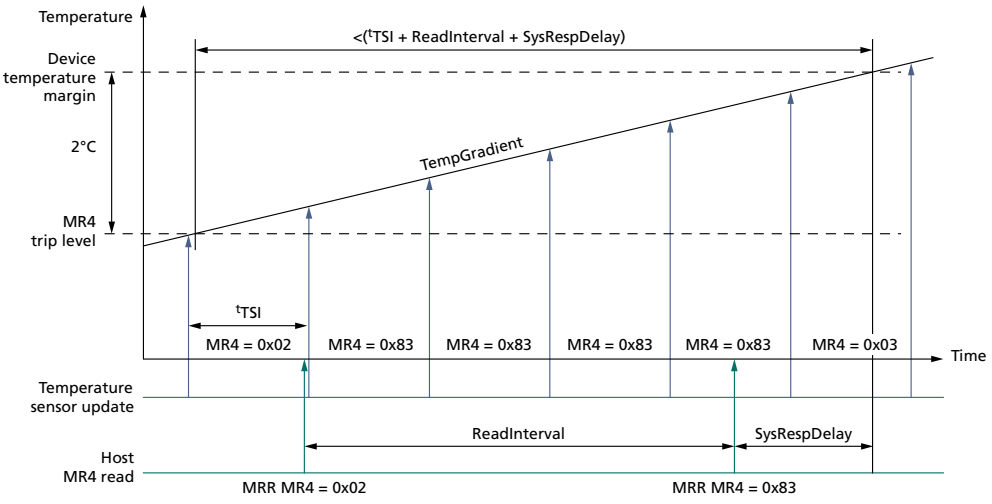
Table 172: Temperature Sensor Parameters (Continued)

Parameter	Symbol	MIN/MAX	Value	Unit	Notes
Temperature Sensor Interval	^{t}TSI	MAX	32	ms	
System Response Delay	SysRespDelay	MAX	System-dependent	ms	
Device Temperature Margin	TempMargin	MAX	2	°C	1
Temperature Sensor Accuracy, second threshold trip point	TempSensorAcc2	MAX	+/-3	°C	1,2
Temperature Sensor Accuracy, fourth threshold trip point	TempSensorAcc4	MAX	+/-3	°C	1,2
Relative Trip Point, second threshold minus first threshold	RelativeTrip2m1	MIN/MAX	MIN 3 / MAX 7	°C	1,3
Relative Trip Point, third threshold minus second threshold	RelativeTrip3m2	MIN/MAX	MIN 3 / MAX 7	°C	1,4
Relative Trip Point, fourth threshold minus third threshold	RelativeTrip4m3	MIN/MAX	MIN 3 / MAX 7	°C	1,4

Notes: 1. Verified by design characterization and may not be subject to production test.
2. Only the minimum (negative side) is specified for the second and fourth thresholds. The device vendor is responsible for guaranteeing correct operation of 1X refresh for MR4 <= 010b and 2X refresh for MR4 <= 100b. (This puts a vendor-specific constraint on the temperature sensor accuracy on the positive side.)
3. The first threshold is defined relative to the second threshold.
4. The third threshold is defined relative to the second and fourth thresholds.

For the table above, if TempGradient is 10°C/s and the SysRespDelay is 1ms: (10°C/s) x (ReadInterval + 32ms + 1ms)≤ 2°C/s. In this case, ReadInterval will not be greater than 68ms.

Figure 65: Temperature Sensor Timing Diagram



Note: 1. MR4 encodings are examples only and assume MR4:OP[4]=0.

Temperature Sensor Usage for 3D Stacked Devices

In the case of 3D stacked (3DS) devices, the refresh rate (MR4) is related to the hottest die in the stack.

Temperature Encoding

The device provides temperature related information to the controller via an encoding on MR4:OP[2:0]. The encodings define the proper refresh rate expected to maintain data integrity.

REFRESH Operation

REFRESH commands are used during normal device operation. The commands are non-persistent; therefore, they must be issued each time a refresh is required. The device requires refresh cycles at an average periodic interval of ^{t}REFI.

Three types of REFRESH operations are supported:

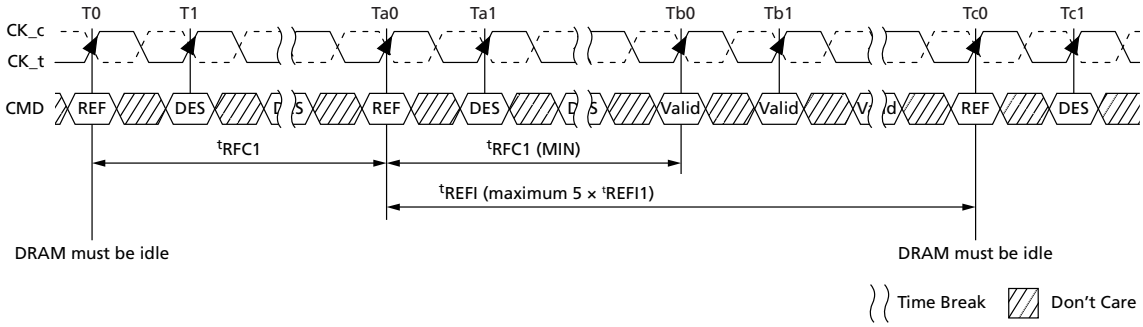
- Normal refresh: Issue the ALL BANK REFRESH (REFab) command in normal refresh mode.
- Fine granularity refresh: Issue the ALL BANK REFRESH (REFab) command in fine granularity refresh mode.
- Same bank refresh: Issue the SAME BANK REFRESH (REFsb) command in fine granularity refresh mode.

This section describes the details of the REFRESH operations, the requirements for each, and the transitions between each type.

For normal REFRESH and fine granularity REFRESH operations, all device banks must be precharged and idle for a minimum of the precharge time (^{t}RP (MIN) before the ALL BANK REFRESH (REFab) command can be applied.

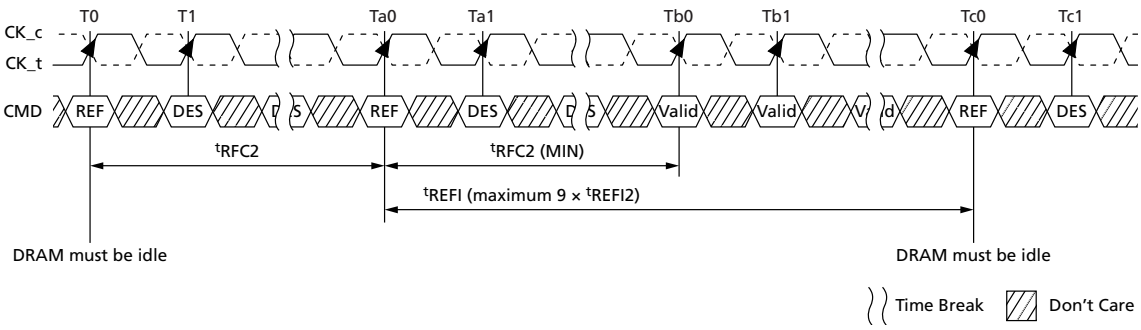
The refresh addressing is generated by the internal refresh controller during the refresh cycle. The external command/address bus (CA[13:0]) is only required to be in a valid state once this cycle has started. When the refresh cycle completes, all device banks will be in the precharged (idle) state. A delay between an issued REFRESH command and the next valid command, except DES, PDE, NOP (PDX) and non-target ODT commands, must be greater than or equal to the minimum refresh cycle time (^{t}RFC (MIN)), as shown in the following figures. Note that the ^{t}RFC timing parameter depends on memory density and the refresh mode setting, which can be set to normal refresh mode or fine granularity refresh mode.

Figure 66: REFRESH Command Timing (Normal Refresh Mode Example)



Notes: 1. Only DES, PDE, NOP (PDX) or non-target ODT commands are allowed after the REF command is issued until ^{t}RFC1 (MIN) expires.
2. Time interval between two REF commands may be extended to a maximum of 5x ^{t}REFI1.

Figure 67: REFRESH Command Timing (Fine Granularity Refresh Mode Example)



Notes: 1. Only DES or non-target ODT commands are allowed after the REF command is issued until ^{t}RFC2 (MIN) expires.
2. Time interval between two REF commands may be extended to a maximum of 9x ^{t}REFI2.

Refresh Modes

The device has two different refresh modes with two different refresh cycle time (^{t}RFC) settings:

- Normal refresh mode
- Fine granularity refresh (FGR) mode

FGR mode provides a shorter refresh cycle time (^{t}RFC2) but also requires ALL BANK REFRESH (REFab) commands to be provided twice as often (^{t}REFI is divided by two; that is, ^{t}REFI2 = ^{t}REFI1/2). The refresh mode setting is programed by the MRW command as shown in the following table. The refresh modes are fixed until changed by MRW command to MR4:OP[4]. On-the-fly refresh mode change is not supported.

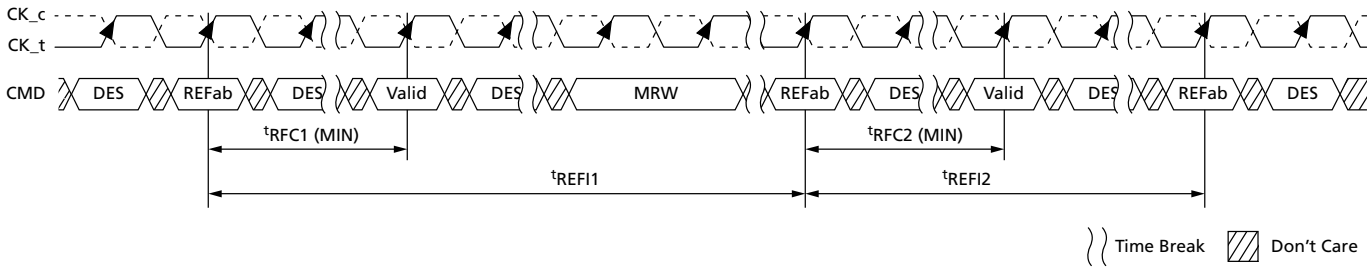
Table 173: Refresh Mode MR Definition

MR4 OP[4]	Refresh Mode (^{t}RFC Setting)
0	Normal refresh mode (^{t}RFC1)
1	Fine granularity refresh mode (^{t}RFC2)

Changing Refresh Mode

When the refresh mode is changed by MRW, the new ^{t}REFI and ^{t}RFC parameters are applied from the moment of the rate change. As shown in the following figure, when an ALL BANK REFRESH command is issued in normal refresh mode, ^{t}RFC1 and ^{t}REFI1 are applied from the time the command (REFab) was issued. And, when an ALL BANK REFRESH command is issued in FGR mode, ^{t}RFC2 and ^{t}REFI2 are satisfied.

Figure 68: Refresh Mode Change Command Timing



Note: 1. Before MRW, the device is in normal refresh mode; after MRW, the device is in FGR mode.

The following conditions must be satisfied before the refresh mode can be changed; otherwise, data retention cannot be guaranteed.

- In normal refresh mode, the REFab command must complete and ^{t}RFC1 must be satisfied before issuing the MRW command to change the refresh mode.
- If performing REFab commands in fine granularity refresh mode, it is recommended that an even number of REFab commands be issued to the device since the last change of the refresh mode with an MRW command before the refresh mode is changed again by another MRW command. If this condition is met, no additional REFRESH commands are required upon the refresh mode change. If this condition is not met, one extra REFab command is required to be issued to the device upon refresh mode change. This extra REFab command is not counted toward the computation of the average refresh interval (^{t}REFI). See the Refresh Mode Change from FGR 2x to Normal 1x Command Timing image below.
- If performing REFsb commands in fine granularity refresh mode, it is recommended that all banks have received an even number of REFsb commands since the last change of the refresh mode with an MRW command before the refresh mode is changed again by another MRW command. If this condition is met, no additional REFRESH commands are required upon the refresh mode change. If this condition is not met, one extra REFab command is required to be issued to the device upon refresh mode change, since an REFab command will reset the internal bank counter. This extra REFab command is not counted toward the computation of the average refresh interval (^{t}REFI). See the 16Gb and Higher Density DRAM Refresh Mode Change from FGR 2x REFsb to Normal 1x Command figure.

Figure 69: Refresh Mode Change from FGR 2x to Normal 1x Command Timing

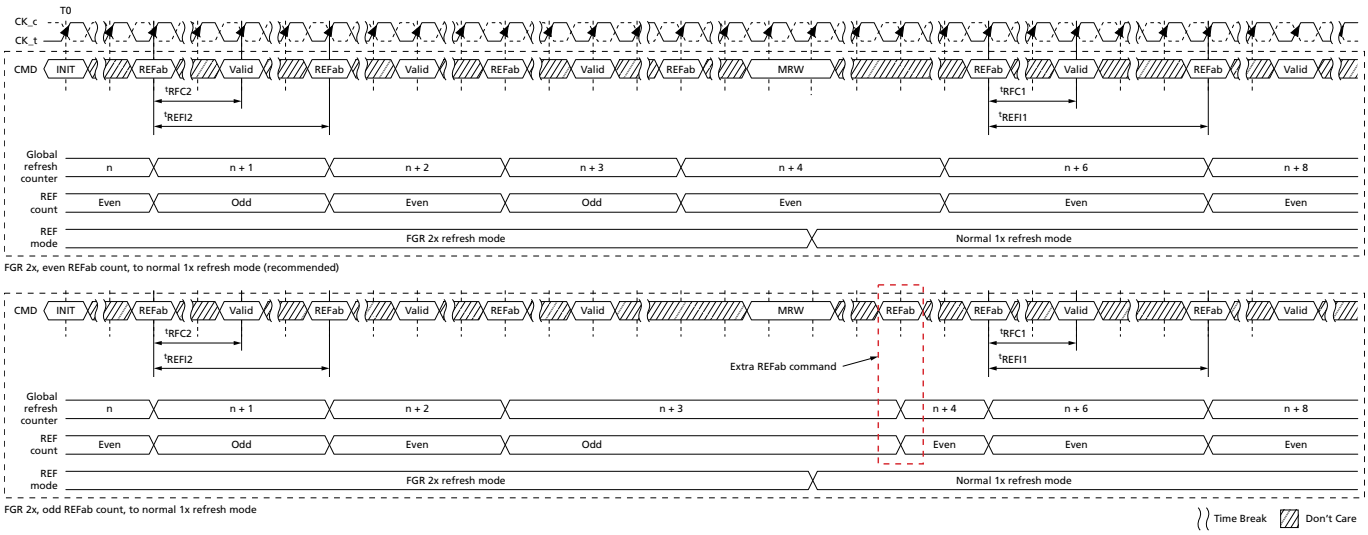
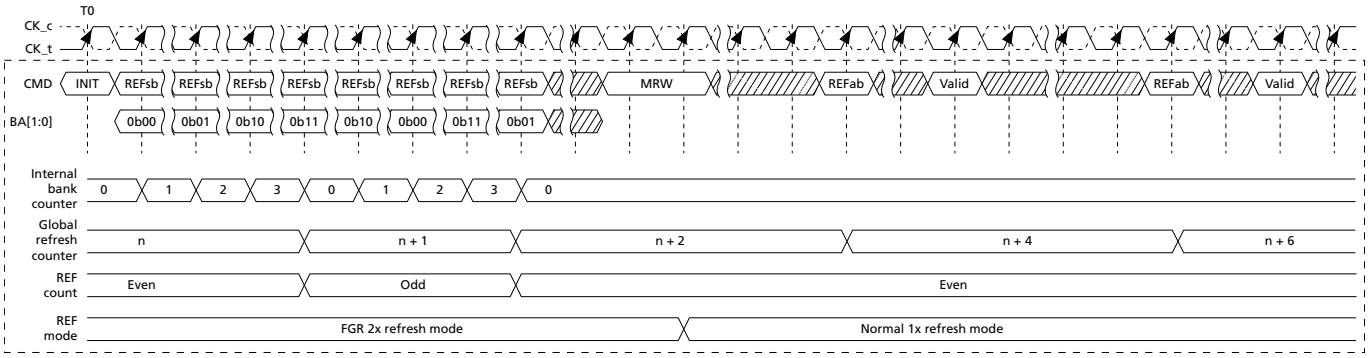
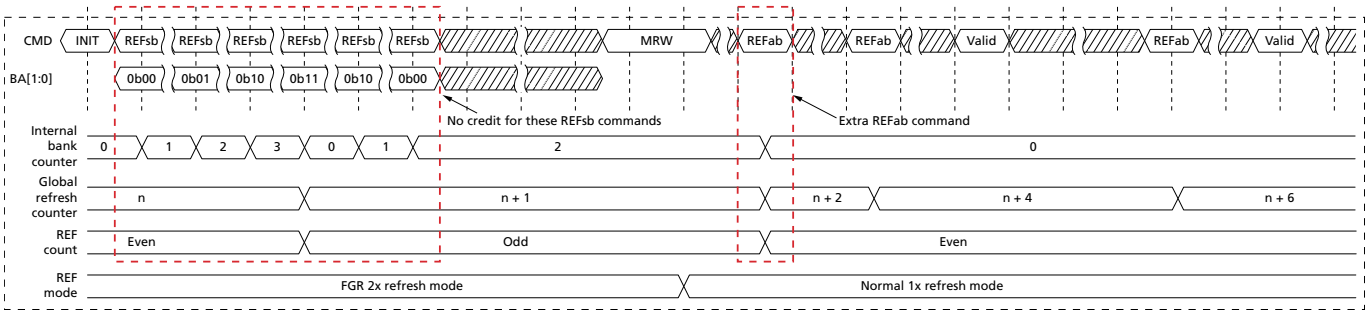


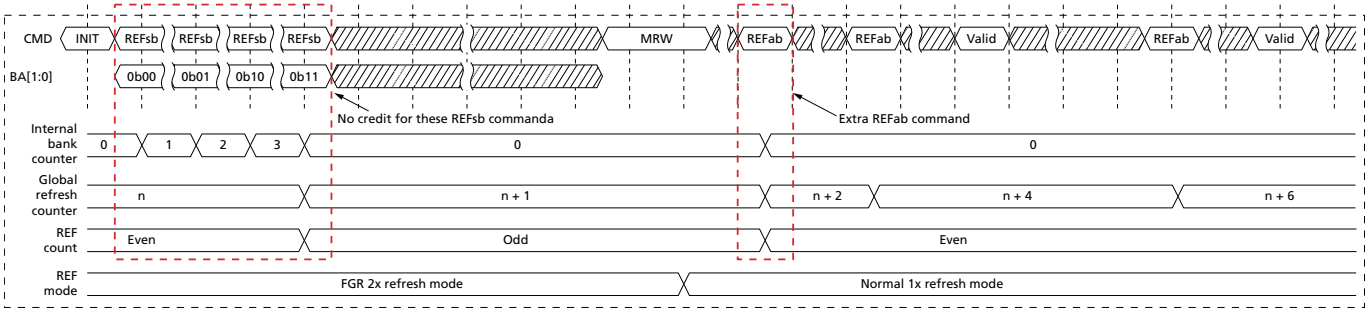
Figure 70: 16Gb and Higher Density DRAM Refresh Mode Change from FGR 2x REFsb to Normal 1x Command Timing



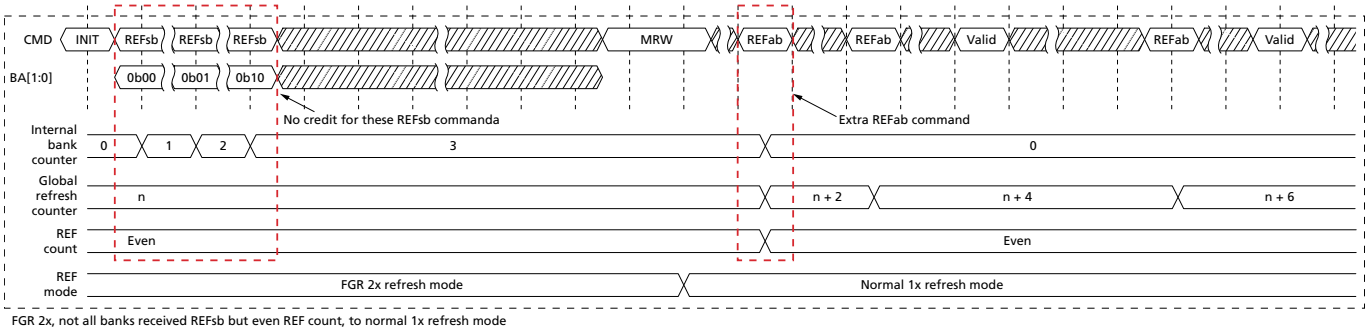
FGR 2x, all banks received REFsb and even REF count, to normal 1x refresh mode (recommended)



FGR 2x, not all banks received REFsb during odd REF count, to normal 1x refresh mode



FGR 2x, all banks received REFsb but odd REF count, to normal 1x refresh mode



FGR 2x, not all banks received REFsb but even REF count, to normal 1x refresh mode

Time Break Don't Care

SAME BANK REFRESH Command

The first SAME BANK REFRESH command (REFsb) applies the refresh process to a specific bank in each bank group (unlike the ALL BANK REFRESH command [REFab], which applies the refresh process to all banks in every bank group). The determination whether a SAME BANK REFRESH or an ALL BANK REFRESH is executed depends on whether a REFsb or REFab command is issued, as shown in the Command Truth Table. The REFsb command is allowed in FGR mode (MR4[4]=1b) only.

Each REFsb command to each bank increments an internal bank counter, and once the bank counter equals the number of available banks in a bank group, it resets and starts over on the next subsequent REFsb.

Each time the internal bank counter resets and starts over on the next subsequent REFsb, the global refresh counter also increments. An REFsb command can be issued to any bank and in any bank order. A subsequent REFsb command issued to the same bank prior to every bank receiving an REFsb command will repeat refreshing the same row, since the device's global refresh counter does not increment until all banks in a bank group receive an REFsb command.

The first REFsb command issued is the *synchronization* REFsb command, and the synchronization count resets the internal bank counter to zero when either (a) every bank has received one REFsb command, (b) RESET is applied, (c) self refresh mode is entered or exited, or (d) REFab is issued. The global refresh counter increments when either an REFab is issued or when all banks have received their one REFsb command and the synchronization count resets to zero. If an REFab command is issued when the bank counter is not zero (that is, in the middle of same bank refreshing), the global refresh counter does not increment until the completion of REFab, effectively losing the credits for any REFsb commands issued prior to the REFab.

Table 174: 16Gb and Higher Density Bank and Refresh Counter Increment Behavior

Count #	Command	BA0	BA1	Refresh Bank #	Internal Bank #	Global Refresh Counter # (Row Address #)
0	RESET, REFab, SRE or SELF REFRESH EXIT (3 x NOP) commands, and in FGR mode (MR4:OP[4]=1)				To 0	-
1	REFsb	0	0	0	0 to 1	*n*
2	REFsb	0	1	1	1 to 2	
3	REFsb	1	0	2	2 to 3	
4	REFsb	1	1	3	3 to 0	
5	REFsb	1	0	2	0 to 1	*n*+1
6	REFsb	0	0	0	1 to 2	
7	REFsb	1	1	3	2 to 3	
8	REFsb	0	1	1	3 to 0	
9	REFsb	0	0	0	0 to 1	*n*+2
10	REFsb	0	1	1	1 to 2	
11	*REFab*	V	V	0-3	To 0	
12	REFsb	1	1	3	0 to 1	*n*+3
13	REFsb	0	1	1	1 to 2	
14	REFsb	0	0	0	2 to 3	
15	REFsb	1	0	2	3 to 0	

Table 174: 16Gb and Higher Density Bank and Refresh Counter Increment Behavior (Continued)

Count #	Command	BA0	BA1	Refresh Bank #	Internal Bank #	Global Refresh Counter # (Row Address #)
16	*REFab*	V	V	0-3	To 0	*n*+4
17	*REFab*	V	V	0-3	To 0	*n*+5
18	*REFab*	V	V	0-3	To 0	*n*+6
19	REFsb	0	0	0	0 to 1	*n*+7
20	*REFab*	V	V	0-3	To 0	
21	REFsb	1	0	2	0 to 1	*n*+8
22	REFsb	0	1	1	1 to 2	
23	REFsb	0	0	0	2 to 3	
24	REFsb	1	1	3	3 to 0	

The REFsb command must not be issued to the device until the following conditions are met:

- ^{t}RFC1 or ^{t}RFC2 has been satisfied after the prior 1x or 2x REF command, respectively
- ^{t}RFCsb has been satisfied after the prior REFsb command
- ^{t}RP has been satisfied after the prior PRECHARGE command to that bank
- ^{t}RRD_L has been satisfied after the prior ACTIVATE command (for example, ^{t}RRD_L has to be met from ACTIVATE of a different bank in the same bank group to the REFsb targeted at the same bank group)

After an REFsb is issued, the target banks (one in each bank group) are inaccessible during the same-bank refresh cycle time (^{t}RFCsb); however, the other banks in each bank group are accessible and can be addressed during this same-bank refresh cycle. When the same-bank refresh cycle completes, the banks refreshed via the REFsb will be in idle state.

After issuing an REFsb command, the following conditions must be met:

- ^{t}RFCsb must be satisfied before issuing an REF command
- ^{t}RFCsb must be satisfied before issuing an ACTIVATE command to the same bank
- ^{t}REFSBRD must be satisfied before issuing an ACTIVATE command to a different bank

Table 175: REFRESH Commands Scheduling Separation Requirements

Symbol	Min Delay From	To	Note
^{t}RFC1	REFab	REFab	1
		ACTIVATE command to any bank	
^{t}RFC2	REFab	REFab	2
		ACTIVATE command to any bank	
		REFsb	
^{t}RFCsb	REFsb	REFab	2
		ACTIVATE command to same bank as REFsb	
		REFsb	
^{t}REFSBRD	REFsb	ACTIVATE command to different bank from REFsb	2

Table 175: REFRESH Commands Scheduling Separation Requirements (Continued)

Symbol	Min Delay From	To	Note
^{t}RRD_L	ACTIVATE	REFsb to different bank from ACTIVATE	2

Notes: 1. MR4:OP[4] set to normal refresh mode.
2. MR4:OP[4] set to FGR mode. REFsb command is valid in FGR mode only.

Postponing REFRESH Command With REFsb

Where *n* is the number of banks in a bank group, a single REFab command can be replaced with *n*REFsb commands for the purpose of scheduling postponed REFRESH commands.

^{t}REFI and ^{t}RFC Parameters

The maximum average refresh interval (^{t}REFI) requirement depends on the refresh mode setting (normal or FGR) and the device's case temperature (T_{case}).

When the refresh mode is set to normal refresh, REFab commands are issued (^{t}RFC1) and T_{case} ≤85°C (the maximum average refresh interval [^{t}REFI1]), is ^{t}REFI. When the refresh mode is set to FGR mode, REFab commands are issued (^{t}RFC2) and T_{case}≤85°C (the maximum average refresh interval [^{t}REFI2]), is ^{t}REFI/2. This same ^{t}REFI/2 interval value is also appropriate if the refresh mode is set to normal refresh mode and REFab commands are issued (^{t}RFC1) but 85°C<T_{case}≤95°C. Finally, if the refresh mode is set to FGR mode, REFab commands are issued (^{t}RFC2) and 85°C<T_{case}≤95°C (the maximum average refresh interval [^{t}REFI2]) is ^{t}REFI/4.

The device includes an optional method for the host to indicate when REFRESH commands are being issued at the 2X (^{t}REFI2) refresh interval rate. The 2X refresh interval rate indicator (MR4:OP[3]) alerts the device if the host supports the refresh interval rate indication as part of the REF command using CA8. If enabled (MR4:OP[3]=1), the host issues 1X REF commands with CA8=H (T_{case}≤85°C), and the host issues 2X REF commands with CA8=L (T_{case} any allowable temperature). MR4:OP[3] is a status read/write (SR/W) MR bit that shows DDR5 support of this optional feature. Reading MR4:OP[3] returns a 1 if the 2X refresh interval rate indicator is supported. A 0 is returned if not supported.

When issuing SAME BANK REFRESH (REFsb) commands, the maximum average refresh interval is further divided down by the number of banks in a bank group, represented by "n" (e.g., 16GB: n=4). Where a REFab command maximum average refresh interval in FGR (^{t}REFI2) is either ^{t}REFI/2 or ^{t}REFI/4 depending on the case temperature range, the REFsb command maximum average refresh interval is either ^{t}REFI/(2*n) or ^{t}REFI/(4*n), respectively.

^{t}REFI is based on the 8192 REFRESH commands that need to be issued within the baseline ^{t}REF =32ms refresh period on the device. ^{t}REFI parameters are shown in the table below.

^{t}REFI and ^{t}RFC Parameters for 3DS Devices

Typical platforms are designed with the assumption that no more than one physical rank is refreshed simultaneously. To limit the maximum refresh current (I_{DD5B1}) for a 3DS stacked device, it is required to stagger the REFRESH commands to each logical rank within a 3DS stack.

The ^{t}RFC time for a single logical rank is defined as ^{t}RFC_slr and is specified as the same value as for a monolithic device of equivalent density. The minimum amount of stagger between REFRESH

commands sent to different logical ranks (^{t}RFC_dlr) or physical ranks (^{t}RFC_dpr) is specified to be approximately ^{t}RFC_slr/3, as shown in the table below.

Table 176: ^{t}REFI Parameters for REFab and REFsb Commands by Device Density (Including 3DS)

Command	Refresh Mode	Parameter	Temperature	Expression	Value	Unit	Note
REFab	Normal	^{t}REFI1	0°C ≤T_{CASE} ≤85°C	^{t}REFI	3.9	µs	1,2,3
			85°C <T_{CASE} ≤95°C	^{t}REFI/2	1.95		
REFab	Fine Granularity	^{t}REFI2	0°C ≤T_{CASE} ≤85°C	^{t}REFI/2	1.95		
			85°C <T_{CASE} ≤95°C	^{t}REFI/4	0.975		
REFsb	Fine Granularity	^{t}REFIsb	0°C ≤T_{CASE} ≤85°C	^{t}REFI/(2*n)	1.95/n		
			85°C <T_{CASE} ≤95°C	^{t}REFI/(4*n)	0.975/n		

Notes: 1. All 3D-stacked (3DS) devices follow the same requirements as the monolithic die, regardless of logical rank.
2. 3DS specification covers up to 16Gb density. Larger densities such as 24Gb or 32Gb may have different ^{t}REFI requirements
3. n is the number of banks in a bank group (for example, 8Gb: n=2; 16Gb: n=4)

Table 177: Refresh Granularity ^{t}RFC1 and ^{t}RFC2 Parameters by Device Density

REFRESH Operation	Parameter	8Gb	16Gb	24Gb	32Gb	Units
Normal	^{t}RFC1,min	195	295	410	410	ns
Fine (FGR mode)	^{t}RFC2,min	130	160	220	220	ns
Same Bank (REFsb)	^{t}RFCsb,min	115	130	190	190	ns

Table 178: 3DS ^{t}RFC Parameters by Logical and Physical Rank Density

REFRESH Operation	Parameter	8Gb	16Gb	24Gb	32Gb	Units	Notes
Normal refresh with 3DS same logical rank	^{t}RFC1_slr,min	^{t}RFC1,min				ns	1
Fine granularity refresh (FGR) mode with 3DS same logical rank	^{t}RFC2_slr,min	^{t}RFC2,min					1
Same Bank (REFsb) with 3DS same logical rank	^{t}RFCsb_slr,min	^{t}RFCsb,min					1
Normal with 3DS different logical rank	^{t}RFC1_dlr,min	^{t}RFC1,min/3					3
Normal refresh with 3DS different physical rank	^{t}RFC1_dpr,min	^{t}RFC1,min/3					2,3
FGR mode with 3DS different logical rank	^{t}RFC2_dlr,min	^{t}RFC2,min/3					3
FGR mode with 3DS different physical rank	^{t}RFC2_dpr,min	^{t}RFC2,min/3					2,3
Same Bank (REFsb) with 3DS different logical rank	^{t}RFCsb_dlr,min	^{t}RFCsb,min/3					

Notes: 1. All 3D-stacked (3DS) devices follow the same requirements as the monolithic die for same logical ranks.
2. Parameter applies to dual-physical rank (36 and 40 placement) 3DS-based DIMMs built with JEDEC PMICXXXX, but may not apply to DIMMs built with higher current capacity PMICs.

3. 3DS ^{t}RFC parameters are to be rounded up to the nearest 1ns after the ^{t}RFC*(min)/3 calculation.

Table 179: Same Bank Refresh Parameters

Refresh Mode	Parameter	8Gb	16Gb	24Gb	32Gb	Units
Same Bank Refresh to ACT delay	^{t}REFSBRD,min	30	30	30	30	ns

Table 180: Same Bank Refresh Parameters for 3DS 2H, 4H

Refresh Mode	Parameter	8Gb	16Gb	24Gb	32Gb	Units
Same Bank Refresh to ACT delay, SLR	^{t}REFSBRD_slr,min	30	30	30	30	ns
Same Bank Refresh to ACT delay, DLR	^{t}REFSBRD_dlr,min	30	30	15	15	

Refresh Operation Scheduling Flexibility

In general, a REFab command (or equivalent number of REFsb commands) needs to be issued to the device regularly every ^{t}REFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided.

In normal refresh mode, a maximum of four REFab commands can be postponed, meaning that at no point in time more than a total of four REFRESH commands are allowed to be postponed. In a case where four REFab commands are postponed in a row, the resulting maximum interval between the surrounding REFab commands is limited to 5 × ^{t}REFI1 (see the Postponing REFRESH Commands Example of Normal Refresh Mode figure below). At any given time, a maximum of five REFab commands can be issued within the 1 x ^{t}REFI1 window.

Self-refresh mode may be entered with a maximum of four REFab commands being postponed. After exiting self-refresh mode with one or more REFab commands postponed, additional REFab commands may be postponed to the extent that the total number of postponed REFab commands (before and after the self-refresh) will never exceed four. During self-refresh mode, the number of postponed REFab commands does not change.

In fine granularity refresh (FGR) mode, the maximum REFab commands that may be postponed is eight, with the resulting maximum interval between the surrounding REFab commands limited to 9 x ^{t}REFI2 (see the Postponing Refresh Commands Example of Fine Granularity Refresh figure below). At any given time, a maximum of nine REFab commands can be issued within 1 x ^{t}REFI2 window. The same maximum count of eight applies to postponed REFab commands around self refresh entry and exit.

Figure 71: Postponing REFRESH Commands Example of Normal Refresh Mode ^{t}REFI1, ^{t}RFC1

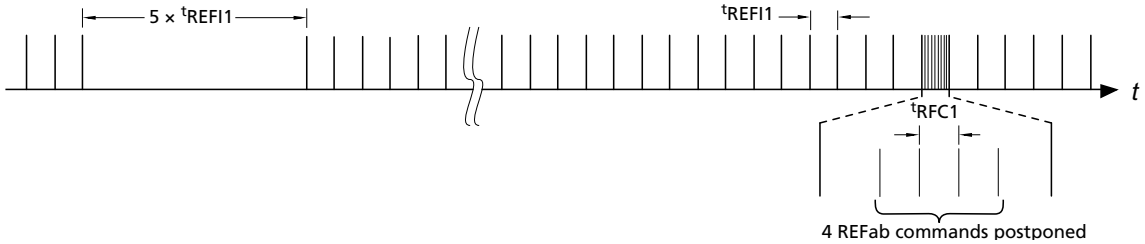
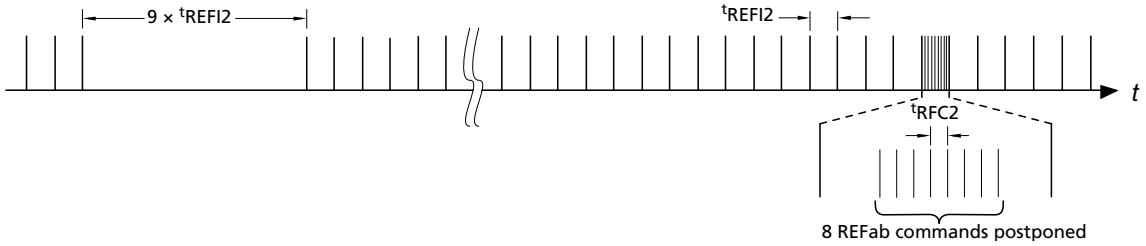


Figure 72: Postponing REFRESH Commands Example of Fine Granularity Refresh Mode ^{t}REFI2, ^{t}RFC2



Module Rank and Channel Limitations for DDR5 DIMMs

To achieve efficient module power supply design for JEDEC-standard DDR5 DIMMs, minimum timings as well as limitations in the number of DRAMs are provided for refresh occurring on a single module. Additionally, since these modules are organized as two independent 36-bit or 40-bit channels (32 bits for non-ECC DIMMs), additional restrictions apply to limit localized power delivery noise on the module.

To provide best performance, the different channels may initiate commands on the same cycle provided the rank-to-rank timings are met, the maximum number of DRAMs in a given activity is not exceeded, and the applicable component timings shown elsewhere in this specification are met. The timing and operational relationships for DDR5 DIMMs are shown below.

Table 181: Module Rank and Channel Timings During REFRESH Operation

DIMM Configuration	Maximum Number of Die in Simultaneous or Overlapping Activity	
	REFRESH (All-bank REFRESH)	
	Die per Physical Rank	Die per DIMM
SR x16	No restriction	
DR x16	No restriction	
SR x8	No restriction	
DR x8	No restriction	
SR x4	No restriction	
DR x4	No restriction	
DR x4 (2H 3DS)	No restriction	40
DR x4 (4H 3DS)	30	40
DR x4 (8H 3DS)	TBD	TBD

Notes: 1. Any combination of commands, with up to the maximum of die per channel and per DIMM, per condition is allowed.
2. REFRESH commands to different channels do not require stagger.
3. ^{t}RFC_dlr must be met for REFRESH commands to different logical ranks within a package rank on the same channel.
4. Any device is considered to be in refresh mode until ^{t}RFC time has been met.
5. Each rank consists of one group of DRAMs making up a 36- or 40-bit channel (32 bits for non-ECC DIMMs).
6. These restrictions only apply to explicit all-banks REFRESH commands (REFab) and not to SELF REFRESH ENTRY or EXIT.
7. Restrictions apply to DIMMs built with JEDEC PMICXXXX, but may not apply to DIMMs built with higher current capacity PMICs.

Self Refresh Entry and Exit

The device can enter self refresh mode anytime in normal refresh and FGR mode without any restriction on the number of REFRESH commands that have been issued during the mode before entering self refresh. However, upon exiting self refresh, extra REFRESH command(s) may be required depending on the condition of the self refresh entry. The conditions and requirements for the extra REFRESH command(s) are defined as follows:

- The normal refresh mode has no special restrictions.
- If performing REFab commands in FGR mode, it is recommended there be an even number of REFab commands before entry into self refresh since the last self refresh exit or MRW command that set the FGR mode. If this condition is met, no additional REFRESH commands are required upon self refresh exit. If this condition is not met, one extra REFab command is required to be issued upon self refresh exit. These extra REFRESH commands are not counted toward the computation of the average refresh interval (^{t}REFI2). See the FGR 2X SREF Command Timing figure below.
- If performing REFsb commands, it is recommended that all banks have received a REFsb command prior to entering self refresh, since entering and exiting self refresh resets the internal bank counter. If this condition is met, no additional REFRESH commands are required upon self refresh exit, and REFsb commands again can be issued to any bank in any bank order. If this condition is not met, one extra REFab command or an extra REFsb command to each bank is required to be issued upon self refresh exit. These extra REFRESH commands are not counted toward the computation of the average refresh interval, ^{t}REFI2 (see the 16Gb and Higher Density Devices with Four Banks per Bank Group example ^{t}REFI2 figure below).

Figure 73: FGR 2X to SREF Command Timing

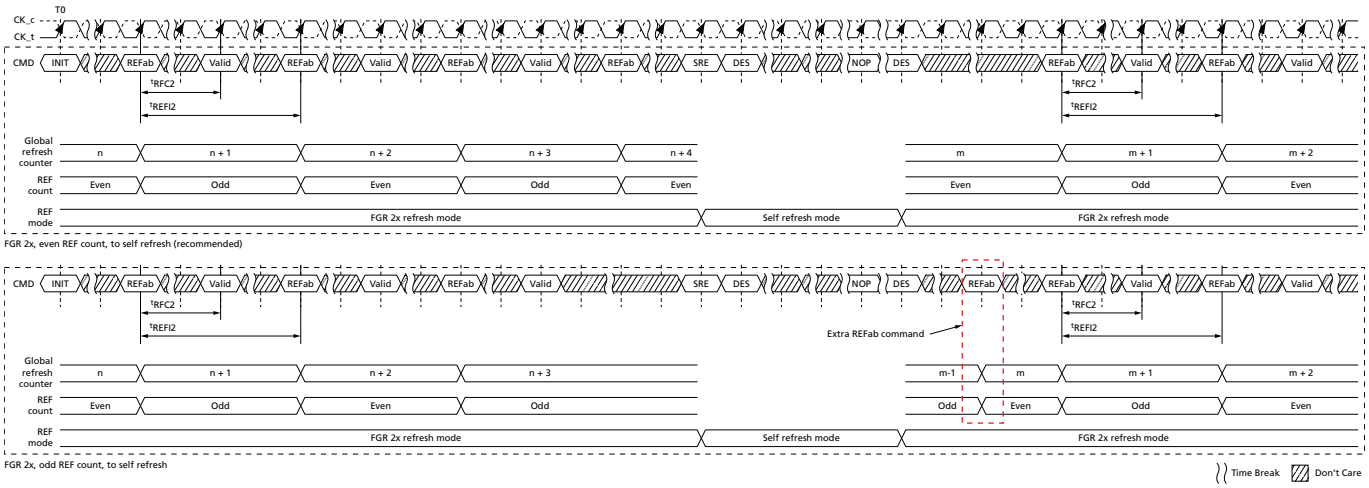
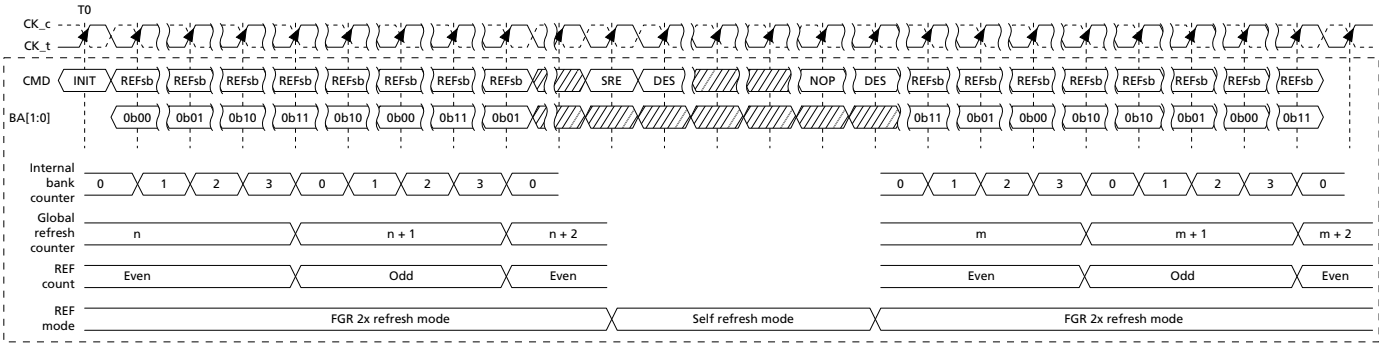
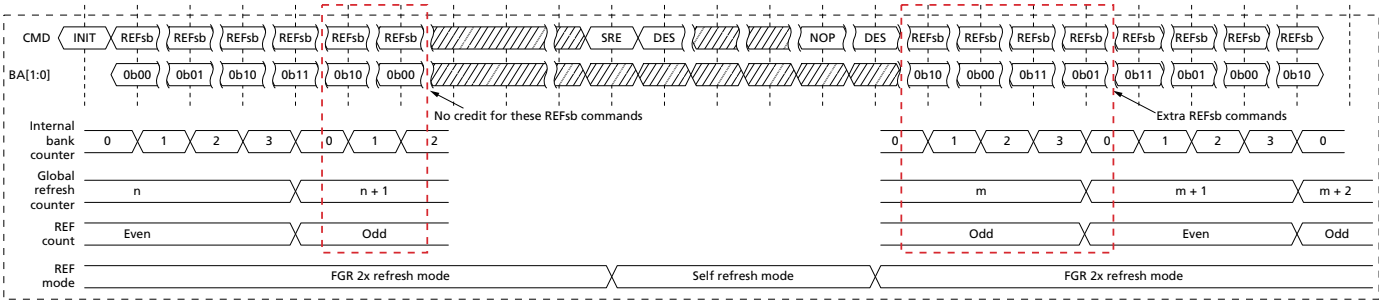


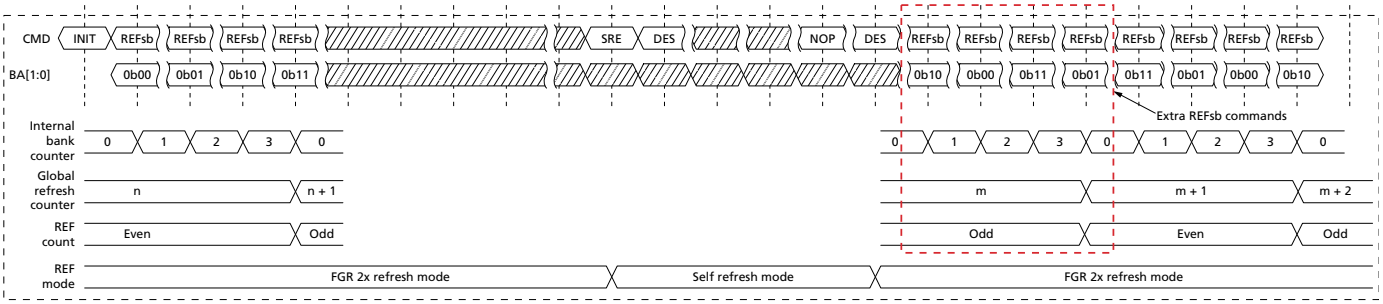
Figure 74: 16Gb and Higher Density FGR 2x REFsb to SREF Command Timing



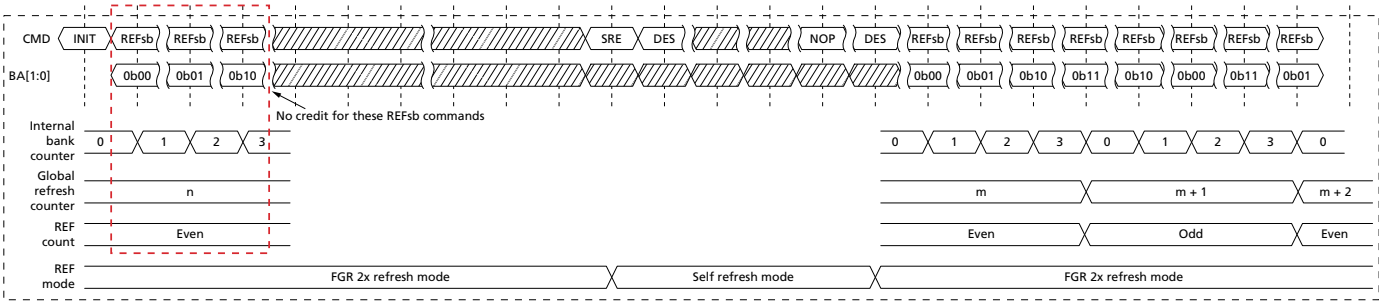
FGR 2x, all banks received REFsb and even REF count, to self refresh (recommended)



FGR 2x, not all banks received REFsb during odd REF count, to self refresh



FGR 2x, all banks received REFsb but odd REF count, to self refresh



FGR 2x, not all banks received REFsb and even REF count, to self refresh

Time Break Don't Care

Self Refresh Operation

Self refresh mode retains data in the device, even if the rest of the system is powered down. When in self refresh mode, the device retains data without external clocking. The device has a built-in timer to accommodate self refresh operation.

While in self refresh mode, the device adjusts and updates its internal average periodic refresh interval as needed, based on its own temperature sensor. The internal average periodic refresh interval adjustment (increasing, decreasing or staying constant) does not require any external control.

SELF REFRESH ENTRY (SRE) is command-based, while the SELF REFRESH EXIT command is defined by the transition of CS_n LOW to HIGH with a defined pulse width ^{t}CSH_SRexit, followed by three or more NOP commands (^{t}CSL_SRexit) to ensure device stability in recognizing exit, as described in detail below. SELF REFRESH EXIT is sometimes referred to as SRX (3 x NOPs).

Before issuing the SRE command, the device must be in an idle state defined as all banks closed (^{t}RP, etc. satisfied), no data bursts in progress, and all timings from previous operations satisfied (^{t}MRD, ^{t}RFC, etc.). A DES command must be registered on the last positive clock edge before issuing the SELF REFRESH ENTRY command. Once the SELF REFRESH ENTRY command is registered, DES commands must also be registered at the next positive clock edge until ^{t}CPDED is satisfied. After ^{t}CPDED is satisfied, CS_n must transition LOW. After CS_n transitions LOW at the end of ^{t}CPDED, CS_n remains LOW until exit. The device may switch to a CMOS-based receiver to save more power, and that transition should coincide with CS_n going LOW.

When CS_n is held LOW, the device automatically disables ODT termination and sets High-Z as the termination state, regardless of R_{TT} configuration for the duration of self refresh mode. Upon exiting self refresh, the device automatically enables ODT termination and sets RTT_PARK (for DQs) asynchronously during ^{t}XS_DLL when RTT_PARK is enabled. CA/CS/CK ODT reverts to its strapped or MR ODT setting state if previously applied. During normal operation (DLL on), the DLL is automatically disabled upon entering self refresh and is automatically enabled (including a DLL Reset) upon exiting self refresh.

When the device enters self refresh mode, all of the external control signals except CS_n and RESET_n are don't care. For proper self refresh operation, all power supply and reference pins (V_{DD}, V_{DDQ}, V_{SS} and V_{PP}) must be at valid levels. The internal V_{REFDQ} and/or V_{REFCA} generator circuitry may remain on or turned off depending on device design. If internal V_{REFDQ} and/or V_{REFCA} circuitry is turned off in self refresh, when the device exits from the self refresh state, it ensures that V_{REFDQ} and/or V_{REFCA} and generator circuitry is powered up and stable within ^{t}XS period. The first WRITE operation or the first write-leveling activity may not occur earlier than ^{t}XS_DLL (or ^{t}XS if the first command does not require a locked DLL) after exit from self refresh mode. The device initiates a minimum of one REFRESH command internally within ^{t}SR period once it enters self refresh mode.

The clock must be valid until ^{t}CKLCS; however, it is not required after ^{t}CKLCS expires (but it should be noted that shortly after ^{t}CPDED, the termination for the clock will be switched off). The clock is internally disabled (inside the device) during the SELF REFRESH operation to save power. The minimum time that the device must remain in self refresh mode is ^{t}CSL. You may change the external clock frequency or halt the external clock ^{t}CKLCS after SRE is registered; however, the clock must be restarted and stable ^{t}CKSRX before the device can exit SELF REFRESH operation.

The procedure for exiting self refresh requires a sequence of events. Because the device switches to a CMOS-based driver to save power, the device triggers self refresh exit upon seeing the CS_n transition from LOW to HIGH, and stays HIGH for ^{t}CSH_SRexit. From the time ^{t}CASRX prior to CS_n transi-

tioning HIGH, the CA bus must be driven HIGH. Once tCSH_SRexit is satisfied, three NOP commands must be issued; otherwise, the device could be put into an unknown state. The clocks must be valid for tCKSRX prior to issuing the NOP command that completes the self refresh exit sequence. Once a self refresh exit is registered, the following timing delays must be satisfied for the subsequent command, depending on if the command requires a locked DLL or not:

Commands that do not require locked DLL:

tXS - ACT, MPC, MRW, PDE, PDX (NOP), PRE(ab,sb,pb), REF(ab,sb), RFM(ab,sb), SRE, SRX (NOP+NOP+NOP), VREFCA, VREFCS, WRP

Commands that require locked DLL:

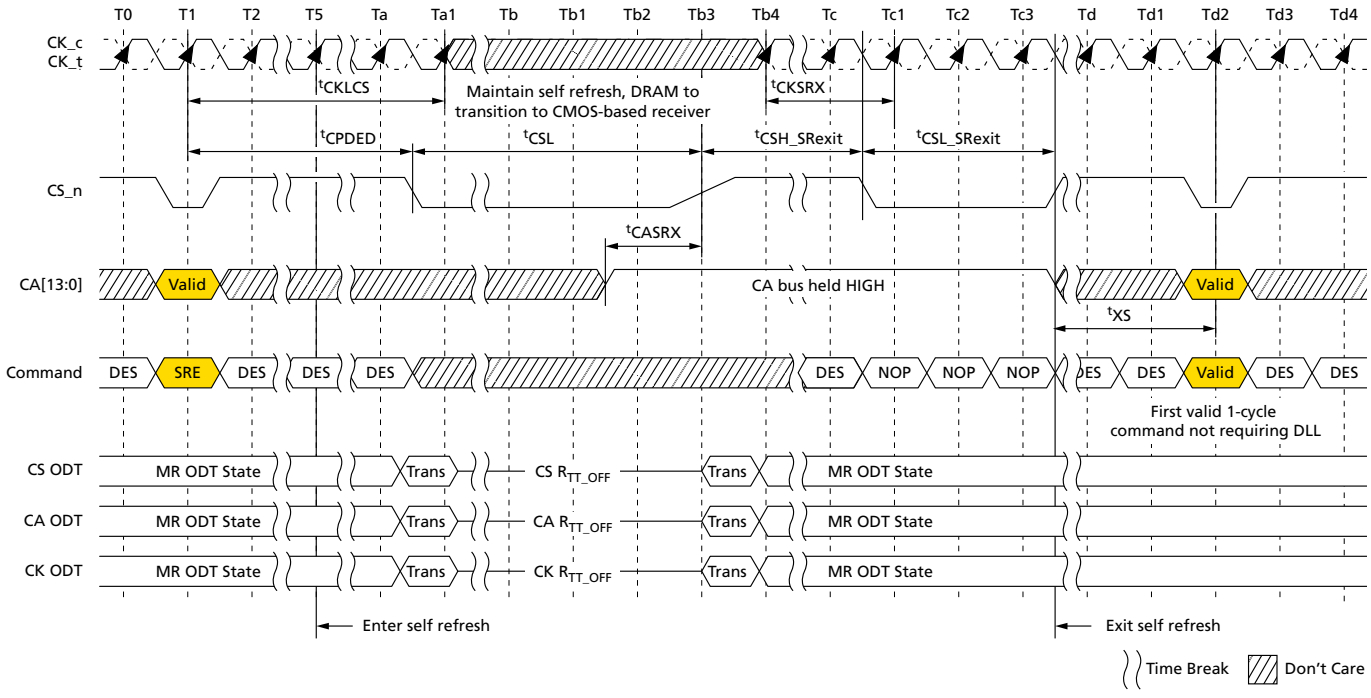
tXS_DLL - MRR, MRR-NT, RD, RD-NT, WR, WR-NT

Depending on the system environment and the amount of time spent in self refresh mode, ZQ calibration commands may be required to compensate for the voltage and temperature drift as described in the ZQ Calibration Commands section. To issue ZQ calibration commands, applicable timing requirements must be satisfied.

Upon exiting self refresh, one additional refresh must be issued in addition to normally scheduled refreshes. This refresh counts toward the maximum number of refreshes which may be postponed. The extra refresh consists of a single REFab command or n*REFsb, where n is the number of banks in a bank group. If self refresh is to be re-entered, and no regularly scheduled periodic refresh commands have been issued, a minimum of one REFab or n*REFsb commands must be issued prior to self refresh re-entry.

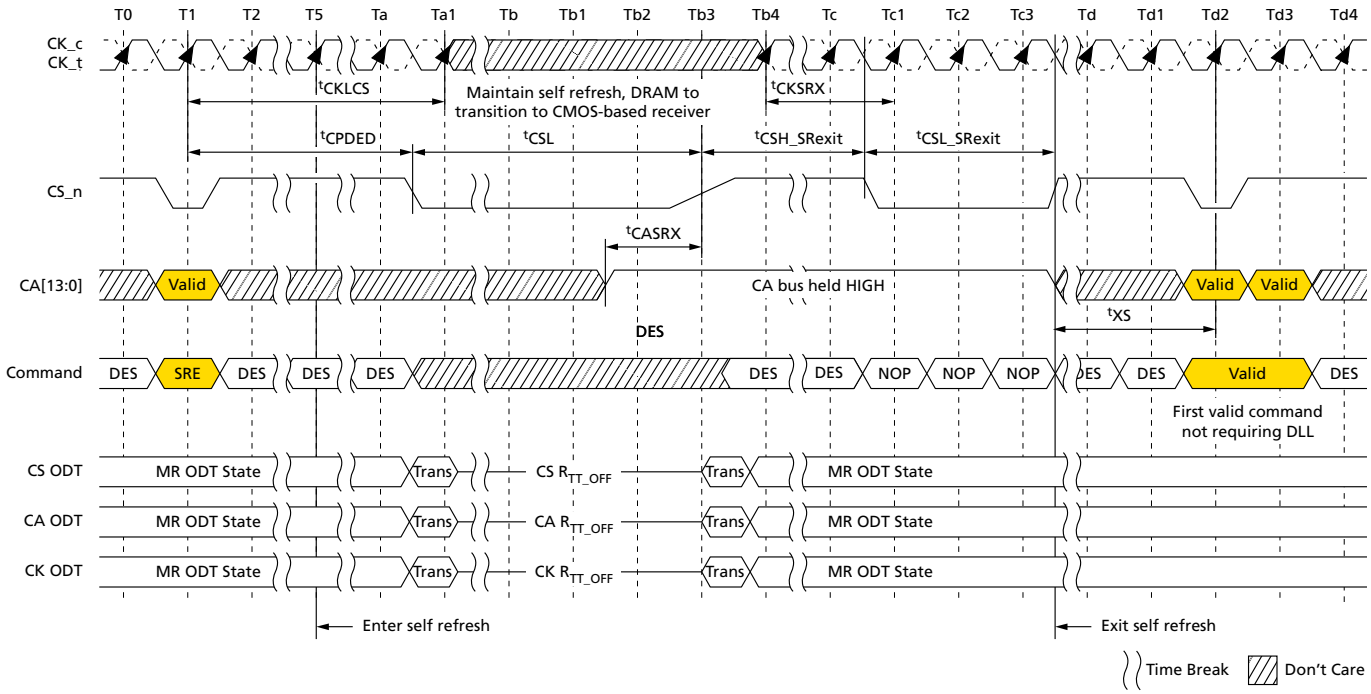
The exit timing from self refresh exit to first valid command not requiring a locked DLL is tXS. The minimum value of tXS is (tRFC1). This delay is to allow for any refreshes started by the device to complete. tRFC1 continues to grow with higher density devices; therefore, tXS will grow as well.

Figure 75: Self Refresh Entry/Exit Timing with One-Cycle Exit Command



Notes: 1. While in 2N mode, ^{t}CSL_SRexit is not statically held LOW (as shown above) because it pulses for each two-cycle period. Refer to the 2N mode section for more details.
2. When ^{t}CSH_SRexit min expires, the CA bus is allowed to transition from all bits HIGH to any valid (V) level. Prior to CS_n being registered LOW at Tc1, the CA bus must transition to NOP conforming to the CAI state of the device and complying with applicable device input timing parameters

Figure 76: Self Refresh Entry/Exit Timing with Two-Cycle Exit Command



Notes: 1. While in 2N mode, ^{t}CSL_SRexit is not statically held LOW (as shown above) because it pulses for each two-cycle period. Refer to the 2N mode section for more details.
2. When ^{t}CSH_SRexit min expires, the CA bus is allowed to transition from all bits HIGH to any valid (V) level. Prior to CS_n being registered LOW at Tc1, the CA bus must transition to NOP conforming to the CAI state of the device and complying with applicable device input timing parameters

Partial Array Self Refresh (PASR)

DDR5 devices may contain an optional feature that disables refresh to selected segments in each bank when in self-refresh mode. The feature allows for lower self refresh power if portions of the devices are not required to retain data. Each bank is divided into six or eight segments based on the three highest row address bits supported by the device's density. Non-binary density devices are divided into six segments because the 110 and 111 encodings of the partial array self refresh (PASR) segment row bits are not used. Binary densities are divided into eight segments.

MR60 provides the segment mask for all banks, with one bit per segment. A 0 (default) in the bit position provides normal REFRESH operation for the segment, while a 1 masks that segment. Masked segments are **not** refreshed during self refresh. Note this affects self refresh only. All segments are refreshed by a REFRESH command when out of self-refresh mode.

Segments that are masked are not guaranteed to retain their data if self refresh is entered. If automatic ECS (MR14 OP[7] = 0b) or automatic ECS in self-refresh (MR15 OP[3] = 1b) is enabled, ECS scrubbing still occurs in unmasked segments while in self refresh; however, the DRAM is not required to execute the ECS on the masked segments. ECS transparency may not produce accurate results if any mask bit is set. Additionally, upon exit of self refresh with masked segments, the masked segments will need to be initialized with known data and the ECS counters will need to be reset if accurate ECS data is required during the next scrub through the full array.

MR19:OP[7] bit indicates whether the device supports PASR. 0 = not supported; 1 = supported

Table 182: MR60 PASR Segment Definition

Segment (PASR Row Bits)	Type	Operand	Data	Note
Segment 0 (000)	W	OP0	0 = Normal, 1 = Masked	
Segment 1 (001)	W	OP1	0 = Normal, 1 = Masked	
Segment 2 (010)	W	OP2	0 = Normal, 1 = Masked	
Segment 3 (011)	W	OP3	0 = Normal, 1 = Masked	
Segment 4 (100)	W	OP4	0 = Normal, 1 = Masked	
Segment 5 (101)	W	OP5	0 = Normal, 1 = Masked	
Segment 6 (110)	W	OP6	0 = Normal, 1 = Masked	Must be 0 for 24Gb devices
Segment 7 (111)	W	OP7	0 = Normal, 1 = Masked	Must be 0 for 24Gb devices

Table 183: PASR Segment Row Address Bits

DRAM Density	PASR Row Bits	Segments
8Gb	R15:13	8
16Gb	R15:13	8
24Gb	R16:14	6
32Gb	R16:14	8
64Gb	R17:15	8

Input Clock Frequency Change

Once initialized, the device requires the clock to be stable during almost all states of normal operation. Once the clock frequency has been set and is in the stable state, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and spread spectrum clocking (SSC) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under self refresh with frequency change mode. Outside of self refresh with frequency change mode, it is illegal to change the clock frequency.

Prior to entering self refresh with frequency change mode, the host must program ^{t}CCD_L/^{t}DLLK/^{t}CCD_L/^{t}CCD_L_WR/^{t}CCD_L_WR2/^{t}DLLK via MR13:OP[3:0] to the desired target frequency and configure VREFCA, VREFCS, RTT_CK, RTT_CS and RTT_CA if needed

Once the device has been successfully placed into self refresh with frequency change mode and ^{t}CKLCS has been satisfied, the state of the clock becomes a don't care. Once in the don't care state, changing the clock frequency is permissible, provided the new clock frequency is stable prior to ^{t}CKSRX. During ^{t}CSL_FreqChg and prior to exiting self refresh, the device will automatically apply the changes to ^{t}CCD_L/^{t}DLLK/^{t}CCD_L/^{t}CCD_L_WR/^{t}CCD_L_WR2/^{t}DLLK, VREFCA, VREFCS, RTT_CK, RTT_CS and RTT_CA. Upon entering and exiting self refresh mode when changing the clock frequency, the self refresh entry and exit specifications must still be met as outlined in Self Refresh Operation.

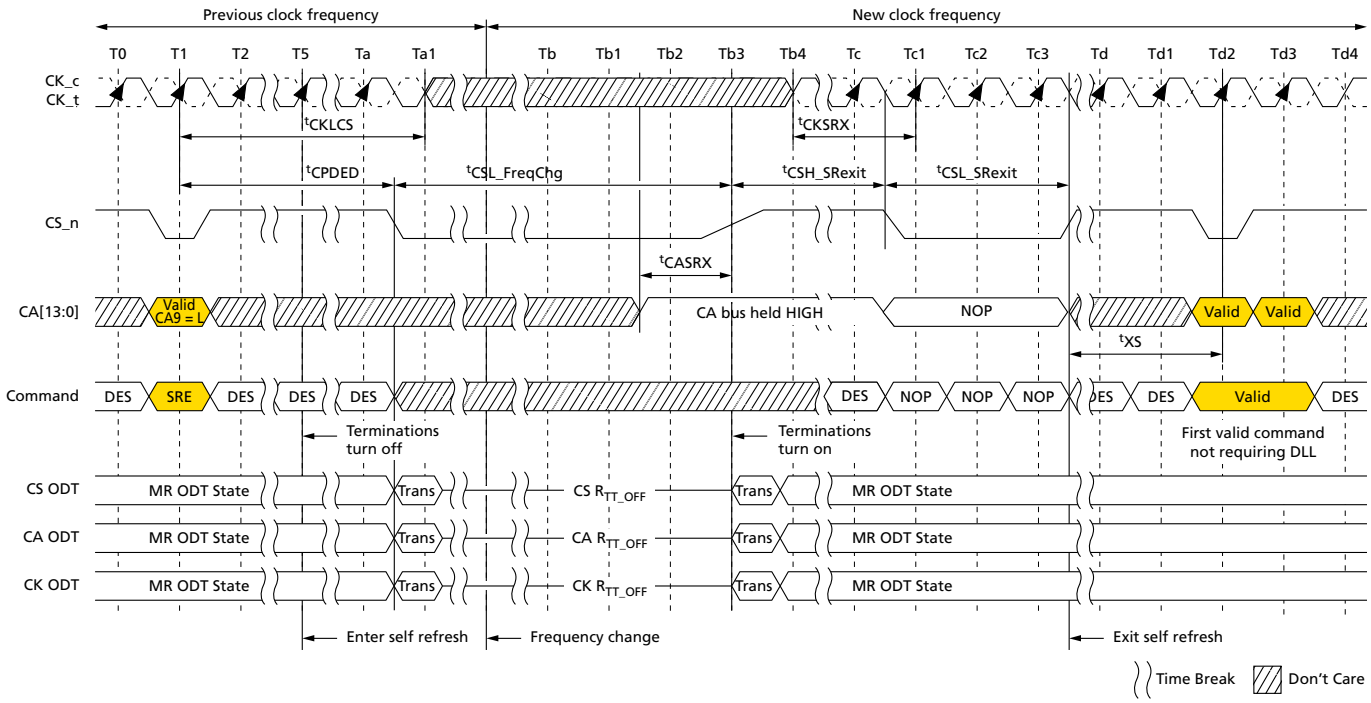
For the new clock frequency, mode registers may need to be configured (to program the appropriate CL, preambles, write leveling internal cycle alignment, etc) prior to normal operation. The device input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade.

Input Clock Frequency Change Steps

The following steps must be taken to execute a frequency change in the DDR5 device:

1. Prior to the SRE command, there are several modes that either must be or can be optionally configured:
   a) The host must program ^{t}CCD_L/^{t}DLLK/^{t}CCD_L/^{t}CCD_L_WR/^{t}CCD_L_WR2/^{t}DLLK via MPC (see the MPC Op-Codes Table) to the desired target frequency. During this stage, these values are set but not enabled.
   b) The host can optionally configure the appropriate CS/CA/CK ODT settings via MPC commands if new values are needed for the new target clock frequency. During this stage, these values are set but not enabled.
   c) The host can optionally configure the VREFCA and/or VREFCS via their corresponding commands. During this stage, these values are set but not enabled.
2. Host sends the SELF REFRESH ENTRY WITH FREQUENCY CHANGE (SREF) command.
3. After ^{t}CPDED, host transition CS_n LOW to signal to the device to turn off the terminations.
4. After ^{t}CKLCS, the clock can be turned off.
5. Device enters self refresh.
6. Changing the clock frequency is permissible, provided the new clock frequency is stable prior to ^{t}CKLSRX.
7. Exiting self refresh with frequency change follows the same process as normal self refresh exit.
8. After^{t}XS, mode register changes that are needed for the new frequency can be configured, and any other commands not requiring a DLL may be issued.
9. After ^{t}XS_DLL, normal operation resumes and all commands are legal.

Figure 77: Frequency Change During Self Refresh



Notes: 1. While in 2N mode, tCSL_SRext will not be statically held LOW (as shown), as it will pulse for each 2-cycle period. Refer to the 2N mode section for more details.

2. If no V_{REFCS} or V_{REFCA} changes are required by the new frequency, the normal tCSL can be used.
3. The figure shows a valid 2-cycle command after tXS for simplicity. 1-cycle valid command is also legal.
4. When tCSH_SRexit (MIN) expires, the CA bus is allowed to transition from all bits HIGH to any valid (V) level. Prior to CS_n being registered LOW at TC1, the CA bus must transition to NOP conforming to the CAI state of the device and complying with applicable device input timing parameters.

Power-Down Mode

Power-down mode does not use CKE to control entry and exit. Instead, power-down mode entry/exit uses the POWER DOWN ENTRY (PDE)/POWER DOWN EXIT (PDX) command, triggered by CS_n. Once in power-down mode, CS_n acts effectively like historic CKE, and the device uses the CS_n transition from HIGH to LOW with a NOP command as the decode for exiting power-down mode; this is referred to as a POWER DOWN EXIT command, or PDX (NOP). In PDE mode, CS_n should be sampled on every edge.

POWER-DOWN ENTRY and POWER-DOWN EXIT Commands

Power-down mode is entered when the POWER-DOWN ENTRY (PDE) command is registered. Unlike self refresh mode, CS_n is NOT held LOW constantly while in power-down. Timing is shown below with details for entry and exit of power-down.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. Device design provides AC/DC timing and voltage specifications, along with proper DLL operation, as long as the controller complies with DRAM specifications.

During power-down, if all banks are closed after any in-progress commands are completed, the device will be in precharge power-down mode. If any bank is open after in-progress commands are completed, the device will be in active power-down mode.

Entering power-down deactivates the input and output buffers, excluding CK_t, CK_c, CS_n, RESET_n. If CA11 = L during the PDE command, CA1 and CA4 will also be excluded, allowing the appropriate NT ODT command to be passed through and decoded by the non-target device while the target device remains in power-down (device will monitor commands that use NT ODT via CA1 and CA4 and will not exit power-down if a valid NT ODT command is registered).

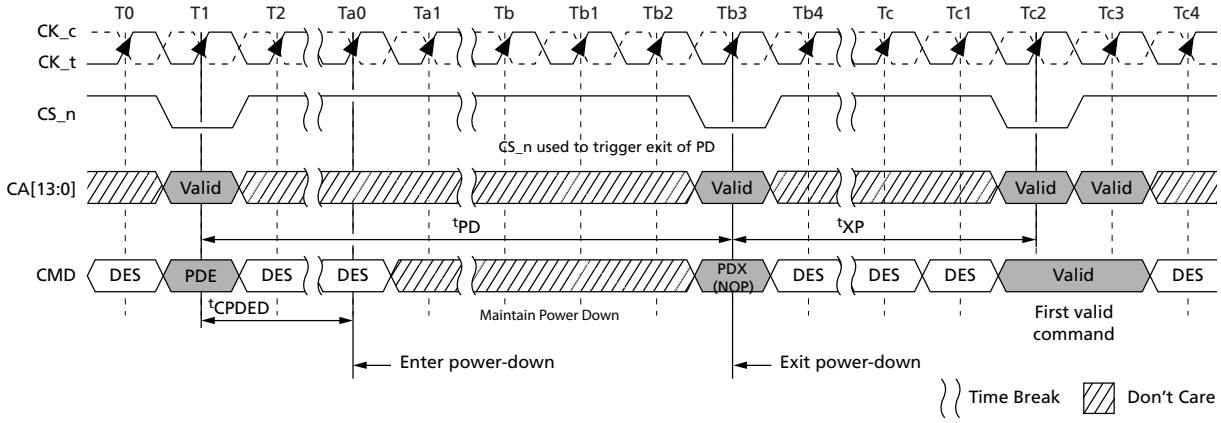
If CA11 = H during the PDE command, only the NOP command qualified by CS_n is legal during power-down. If CA11 = L during the PDE command, only NT ODT commands and NOP commands, qualified by CS_n, are legal during power-down. Refer to the command truth table for more information.

MRR NT ODT commands during power-down are not supported with OTF burst modes in MR0:OP[1:0].

When power-down is entered with ODT control enabled (CA11 = L), the device will continue to accept NT termination commands throughout the power-down process, including entry and exit. Upon entry, during the ^{t}CPDED period, the device will be switching from decoding all CA bus command bits to only decoding CA1 and CA4. During this time, all CA command bits must be valid when CS is asserted with a complete READ or WRITE command, because the device may still be decoding the full command.

Following ^{t}CPDED, only CA1 and CA4 need be valid because the device will be ignoring the others. Following the PDX (NOP) command to exit power-down mode, all CA command bits also must be valid for NT termination commands, because the device will be transitioning to decoding all bits. It is only the time between ^{t}CPDED completion and $^{t}XP_{start}$ that CA[13:5], [3:2], and [0] need not be valid.

Figure 78: Power-Down Entry and Exit Mode



Notes: 1. There is no specific PDX command. In the case of systems with register using CAI, the encoding out of the register may be inverted from a NOP-defined command.
2. Image shows a valid 2-cycle command after ^{t}XP for simplicity. 1-cycle valid commands are also legal.

3. CS_n is held HIGH, not toggled, during power-down (Ta to Tb2), except NON-TARGET ODT command when PDE with CA11=L is asserted.

Table 184: Power-Down Entry Definitions

Device Status	DLL	Power-Down Exit	Relevant Parameters
Active (single bank or more open)	On	Fast	^{t}XP to any valid parameter
Precharged (all banks precharged)	On	Fast	^{t}XP to any valid parameter

The DLL is kept enabled during precharge power-down or active power-down. (If RESET_n goes LOW during power-down, the device will move out of power-down mode and into reset state.) Power-down duration is limited by ^{t}PD(MAX) of the device.

In the following table, the inclusion of Write-NT, Read-NT, and NOP reflects the subset of input signals used for decoding commands while in power-down mode with ODT enabled. These are the same input states detailed in the Command Truth Table. Note that Write-NT and Read-NT are two-cycle commands, requiring CS to be LOW for both cycles. NOP is the only single-cycle command allowed while in power-down mode.

Table 185: Valid Command During Power-Down with ODT Enabled

CA1	CA4	Command	Operation When Device is in Power-Down
L	L	WRITE	Device will enable ODT_WR_NOM
L	H	READ	Device will enable ODT_WR_NOM
H	L	ILLEGAL	Illegal. CS will NOT be asserted to a powered down device with this CA1/CA4 combination
H	H	PDX (NOP)	Exit power-down

Notes: 1. MRR NT ODT commands during power down are not supported with burst-on-the-fly (OTF) modes in MR0 OP[1:0].

Maximum Power Saving Mode

Maximum power saving mode (MPSM) provides a way for the device to be in a low power state while also sharing its input signals with other devices that are active. MPSM is different in DDR5 than DDR4 because DDR5 lacks the CKE signal that DDR4 devices use to exit MPSM.

There are three MPSM states:

- Maximum power saving mode idle (MPSM idle)
- Maximum power saving mode power down (MPSM power down)
- Maximum power saving mode deep power down (MPSM deep power down)

These modes enable low power operation by causing the device to ignore most commands, while at the same time providing proper ODT on both CA and IO signals and a means for the device to be brought into an active state through exiting MPSM by issuing a MRW command.

MPSM is enabled by setting MR2:OP[3] = 1 using an MRW command, at which time the device enters MPSM idle. Alternatively, when MPSM for device 15 is enabled by setting the device 15 MPSM enable bit (MR2:OP[5]) to 1 using an MRW command, and the device's PDA enumerate ID (MR1:OP[3:0]) are equal to 15, the device enters MPSM idle.

Setting the device 15 MSPM enable bit to 1 must be done after PDA device enumeration is complete. Once the device is placed into MPSM idle, it can stay in that state indefinitely, or it can subsequently be placed in either MPSM power down or MPSM deep power down.

Data retention is not guaranteed when the device is in any MPSM state. Mode register status and soft PPR information is preserved.

Figure 79: Maximum Power Saving Mode State Diagram

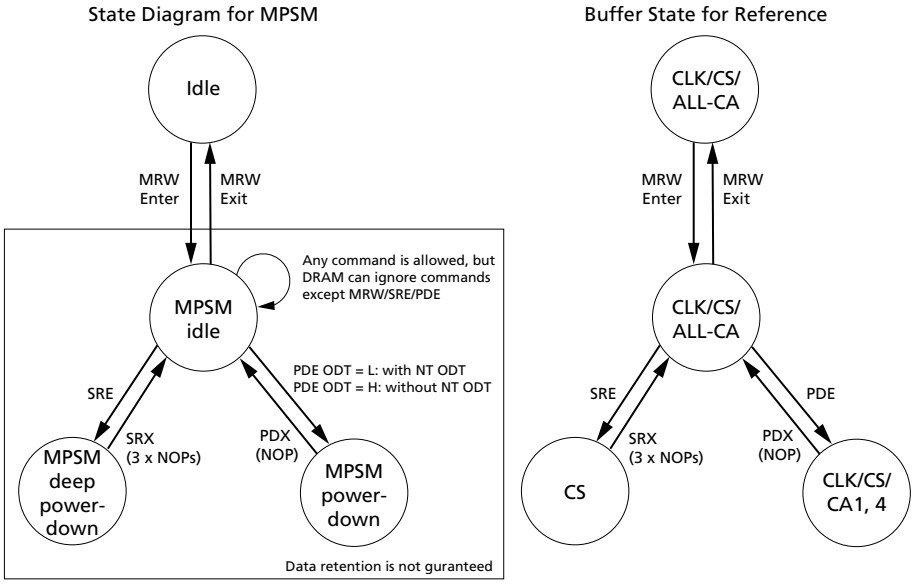


Table 186: MPSM Configuration Options

MPSM MR2:OP[3]	Device 15 MPSM MR2:OP[5]	PDA Enumeration ID MR1:OP[3:0]	Action
1	X	X	Enter MPSM on MRW
X	1	1111	Enter MPSM on MRW
0	0	X	Exit MPSM on MRW
0	X	Not equal to 1111	Exit MPSM on MRW

MPSM Idle State

When the device is in MPSM idle, it ignores all types of commands except MRW, NT ODT, POWER DOWN ENTRY (PDE) and SELF REFRESH ENTRY (SRE); these commands are executed normally. The device does not respond to any other command except these four command types. The DLL status is the same as in the normal idle state. The device continues to drive CA ODT as programmed. Normal command timing parameters are applied in this state, except that ^{t}REFI does not need to be satisfied because the REFRESH command does not need to be issued in this state.

MPSM Power Down State

MPSM power down state is entered by issuing the PDE command from MPSM idle. In this state, the device responds to the NT ODT command normally as it does in the precharged power down state. DLL status is the same as in the normal precharged power down state. When the PDX (NOP) command is issued to exit power down mode, the device returns to MPSM idle after ^{t}XP. Normal power down command timings are applied in this state, except the ^{t}REFI requirement.

MPSM Deep Power Down State

MPSM deep power down (DPD) state is entered from MPSM idle with the SRE command, and exited to MPSM idle with the 3 x NOPs used for the SELF REFRESH EXIT (SRX) command. Input signal requirements in this state are the same as those in self refresh mode. The device does not execute any internal REFRESH operations in this state. Normal SELF REFRESH command timings are applied in this state. When the SRX command is issued, the device returns to the MPSM idle state after ^{t}XS. ^{t}XS_DLL must be met prior to issuing any commands that require a locked DLL. Normal SELF REFRESH command timings are applied in this state.

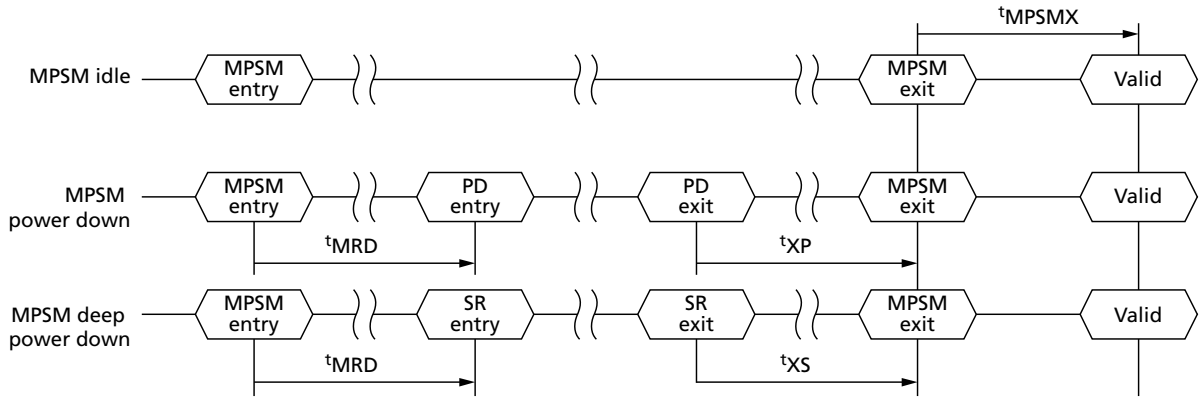
MPSM Command Timings

The device exits from MPSM idle by programming the MPSM enable (MR2:OP[3]) bit to 0 using the MRW command. MPSM exit to the first valid command delay is ^{t}MPSMX.

Table 187: MPSM Timing Parameters

Symbol	Description	MIN	MAX	Unit
^{t}MPSMX	MPSM exit to first valid command delay	^{t}MRD	-	ns

Figure 80: MPSM Exit Timings



Connectivity Test Mode

Connectivity test (CT) mode speeds up testing of electrical continuity of pin interconnection on the PC boards between the memory devices and the memory controller on the SoC.

Designed to work seamlessly with any boundary scan devices, CT mode is required for all devices independent of density and interface width. This applies to x4, x8, and x16 interface widths. Contrary to other conventional shift register-based test modes, where test patterns are shifted in and out of the devices serially in each clock, CT mode in DDR5 allows test patterns to be entered in parallel into the test input pins, and the test results are extracted in parallel from the test output pins of the device at the same time, significantly enhancing connectivity check speed.

Prior to entering CT mode, RESET_n is registered HIGH. CT mode is enabled by asserting the test enable (TEN) pin. Once in CT mode by asserting the TEN pin, the device effectively appears as an asynchronous device to the external controlling agent; after the input test pattern is applied, the connectivity test results are available for extraction in parallel at the test output pins after a fixed propagation delay. During CT mode, CA ODT is set to the default reset value. The device must be reset after exiting CT mode.

Pin Mapping

Only digital pins can be tested via CT mode. For the purpose of connectivity check, all pins that are used for the digital logic in the device are classified as one of the following types:

- **Test Enable (TEN) pin**: When asserted HIGH, this pin causes the device to enter CT mode. In this mode, the normal memory function inside the device is bypassed and the IO pins appear as a set of test input and output pins to the external controlling agent. The TEN pin is dedicated to the connectivity check function and is not used during normal memory operation.
- **Chip Select (CS_n) pin**: When asserted LOW, this pin enables the test output pins in the device. When de-asserted, the output pins in the device are HIGH-Z. The CS_n pin serves as the CS_n pin in CT mode.
- **Test Input:** This group of pins used during normal operation are designated as test input pins; these pins are used to enter the test pattern in CT mode. Most test input pins are input pins during normal operation. The ALERT_n pin is the only output pin that is used as a test input during CT mode. The CK_t and CK_c pins are single-ended test input pins during CT mode.
- **Test Output:**This group of pins used during normal operation are designated test output pins; these pins are used for extraction of the connectivity test results in CT mode.
- **Reset:** Fixed high level for RESET_n is required during CT mode (same as normal function).

Table 188: Pin Classification in CT Mode

Pin Type in CT Mode		Pin Names During Normal Memory Operation
Test Enable		TEN
Chip Select		CS_n
Test Inputs	A	CA[13:0]
	B	CK_t, CK_c
	C	ALERT_n
Test Outputs		DQL[7:0], DQU[7:0], DQSU_t, DQSU_c, DQSL_t, DQSL_c, DML_n, DMU_n, DM_n/TDQS_t, TDQS_c
Reset		Reset_n

Notes: 1. Test outputs may contain the upper and lower label identification used with x16 devices. In the case of x4/x8 devices, the lower identification may be removed.
2. CAI and MIR input levels do not affect test output values.

Table 189: Signal Description

Symbol	Type	Function
TEN	Input	Connectivity test mode is active when TEN is HIGH and inactive when TEN is LOW. TEN must be LOW during normal operation TEN is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DDQ}.

Logic Equations

MTx is an internal signal to be used to generate the signal to drive the output signals. These internal signals are the same across all interface widths and densities.

Table 190: Min Term Equations

Min Term	Intermediate Logic Nodes
MT0	XOR(CA[0,1,2,3,8,9,10,11])
MT1	XOR(CA[0,4,5,6,8,12,13], ALERT_n)
MT2	XOR(CA[1,4,9,12], CK_t, CK_c)
MT3	XOR(CA[2,5,7,10,13], CK_t)
MT4	XOR(CA[3,6,7,11], CK_c, ALERT_n)
MT0_B	!(MT0)
MT1_B	!(MT1)
MT2_B	!(MT2)
MT3_B	!(MT3)
MT4_B	!(MT4)

Table 191: Output Equations per Interface Width

Output	x16	x8	x4
DQL0	MT0	MT0	MT0
DQL1	MT1	MT1	MT1
DQL2	MT2	MT2	MT2
DQL3	MT3	MT3	MT3
DQL4	MT0_B	MT0_B	
DQL5	MT1_B	MT1_B	
DQL6	MT2_B	MT2_B	
DQL7	MT3_B	MT3_B	
DML	MT4	MT4	
TDQS_c		MT4_B	
DQSL_t	MT4	MT4	MT4
DQSL_c	MT4_B	MT4_B	MT4_B
DQU0	MT0		
DQU1	MT1		
DQU2	MT2		
DQU3	MT3		
DQU4	MT0_B		
DQU5	MT1_B		
DQU6	MT2_B		
DQU7	MT3_B		
DMU	MT4		

Table 191: Output Equations per Interface Width (Continued)

Output	x16	x8	x4
DQSU_t	MT4		
DQSU_c	MT4_B		

Notes: 1. Test outputs may contain the x16 upper "U" and lower "L" label identification. In the case of x4 and x8 devices, the lower "L" identification would not be present.

Input Levels and Timing Requirement

Input levels during CT Mode are defined in the CT Mode Input Requirements for TEN, CS_n and Test Inputs Table.

RESET_n input level in C: CMOS DC high above 70% V_{DDQ}.

Prior to the assertion of the TEN pin, all voltage supplies must be valid and stable.

Upon assertion of the TEN pin, the CK_t and CK_c signals are ignored and the device enters CT mode after time ^{t}CT_Enable. In CT mode, no refresh activities in the memory arrays—initiated either externally (i.e., auto-refresh) or internally (i.e., self refresh)—are maintained.

The TEN pin may be asserted after the device completes power-on, after RESET_n has deasserted, the wait time after the RESET_n de-assertion has elapsed, and prior to starting the clock (CK_t, CK_c).

The TEN pin may be de-asserted at any time in CT mode. Upon exiting CT mode, the device states are unknown and the integrity of the original content of the memory array is not guaranteed; therefore, the reset initialization sequence is required. All output signals at the test output pins are stable within ^{t}CT_valid after the test inputs have been applied to the test input pins with TEN input and CS_n input maintained HIGH and LOW, respectively.

Figure 81: CT Mode Timing Diagram

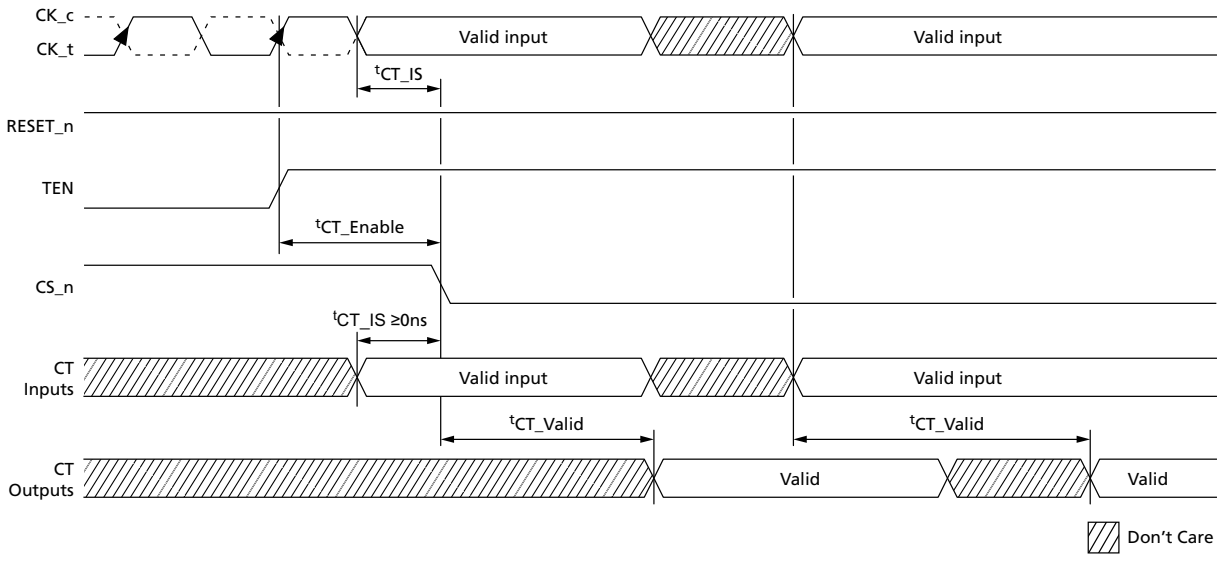


Table 192: CT Mode AC Parameters

Symbol	MIN	MAX	Unit
^{t}CT_IS	0	–	ns

Table 192: CT Mode AC Parameters (Continued)

Symbol	MIN	MAX	Unit
^{t}CT_Enable	200	–	ns
^{t}CT_Valid	–	200	ns

Input Levels

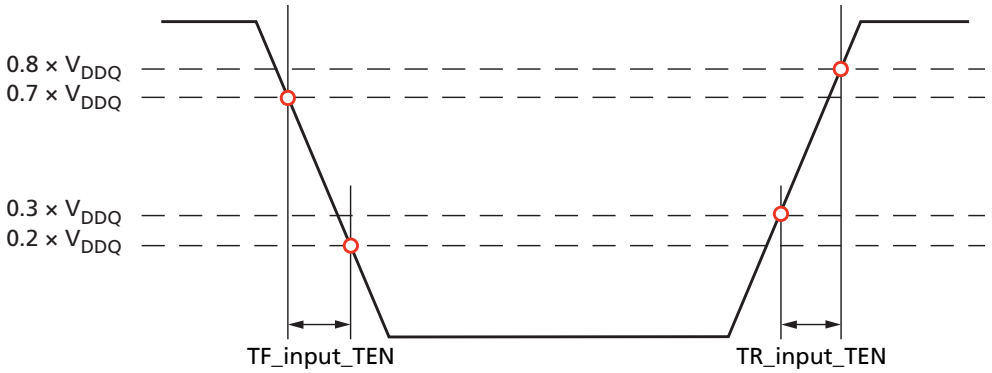
The following input parameters are applied to input signals during CT mode.

Table 193: CT Mode Input Requirements for TEN, CS_n and Test Inputs

Parameter	Symbol	MIN	MAX	Unit	Notes
TEN, CS_N, Test pins AC input high voltage	VIH(AC)_CT	0.8 x V_{DDQ}	V_{DDQ}	V	1
TEN, CS_N, Test pins DC input high voltage	VIH(DC)_CT	0.7 x V_{DDQ}	V_{DDQ}	V	
TEN, CS_N, Test pins DC input low voltage	VIL(DC)_CT	V_{SS}	0.3 x V_{DDQ}	V	
TEN, CS_N, Test pins AC input low voltage	VIL(AC)_CT	V_{SS}	0.2 x V_{DDQ}	V	2
TEN, CS_N, Test pins input signal falling time	TF_input_CT	–	10	ns	
TEN, CS_N, Test pins input signal rising time	TR_input_CT	–	10	ns	

Notes: 1. Overshoot may occur. It should be limited by the absolute maximum DC ratings.
2. Undershoot may occur. It should be limited by the absolute maximum DC ratings.

Figure 82: CT Mode Input Slew Rate Definition



CMOS Rail-to-Rail Input Levels for RESET_n

Table 194: CMOS Rail-to-Rail Input Levels for RESET_n

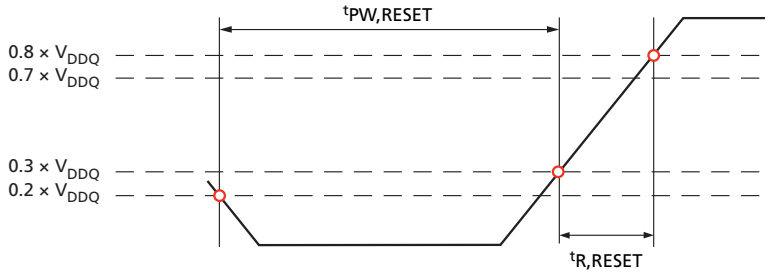
Parameter	Symbol	MIN	MAX	Unit	Notes
AC input high voltage	$V_{IH,AC,RESET}$	0.8 x V_{DDQ}	V_{DDQ}	V	6
DC input high voltage	$V_{IH,DC,RESET}$	0.7 x V_{DDQ}	V_{DDQ}	V	2
DC input low voltage	$V_{IH,DC,RESET}$	V_{SS}	0.3 * V_{DDQ}	V	1
AC input low voltage	$V_{IH,AC,RESET}$	V_{SS}	0.2 * V_{DDQ}	V	7
Rise time	^{t}R,RESET	–	1.0	µs	4

Table 194: CMOS Rail-to-Rail Input Levels for RESET_n (Continued)

Parameter	Symbol	MIN	MAX	Unit	Notes
RESET_n pulse width	$^{t}PW,RESET$	1.0	–	µs	3,5

Notes: 1. After RESET_n is registered LOW, RESET_n level is maintained below $V_{IL,DC,RESET}$ during $^{t}PW\_RESET$; otherwise, the device may not be reset.
2. Once RESET_n is registered HIGH, RESET_n level must be maintained above $V_{IH,DC,RESET}$; otherwise, device operation is not guaranteed until it is reset asserting RESET_n signal LOW.
3. RESET is destructive to data contents.
4. This definition only applies to the reset procedure at power stable.
5. Overshoot may occur; it should be limited by the absolute maximum DC ratings.
6. Undershoot may occur; it should be limited by the absolute maximum DC ratings.

Figure 83: RESET_n Input Slew Rate Definition



Package Output Driver Test Mode

This optional mode enables characterization of the device package by allowing the host to individually turn on the output driver of a single bit of the device, while all other bits remain terminated. To use this test mode, the host sets MR61:OP[4:0] to select the target DM or DQ output driver. The host also sets the target driver to use the pull-up output driver Impedance of 34 ohms (MR5:OP[2:1] = 00b), while the termination for all the other DMs and DQs are defined by MR34:[2:0] (RTT_PARK). Note that all the supportability of DM termination is decided by MR5:OP[5].

This is a test mode only. Normal functionality is not assumed while in this mode or after enabling this mode unless the device is reset. Enter this mode by programming any value in MR61 other than 0. It is only exited via a RESET to the device. Because this is an optional function, the discovery bit is located in MR5:OP[3].

A reset of the device is required after exiting the package output driver test mode.

Even though only five bits of the mode register are needed, the entire mode register is blocked out to isolate it from normal operating modes.

Table 195: MR5 Register (for reference only - see Mode Register Section for details)

MR Address	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
5	Valid	Valid	DM Enable	Valid	PODTM Support	Valid	Valid	Valid

Notes: 1. OP[7:0] can be programmed with either 0 or 1 appropriate to the other bits controlled by MR5.

Table 196: MR61 Register (for reference only - see Mode Register Section for details)

MR Address	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
61	RSVD			Package Output Driver Test Mode				

ZQ Calibration Commands

MPC commands are used to perform ZQ calibration, which calibrates the output driver termination impedance across process, temperature, and voltage. ZQ calibration occurs in the background of device operation.

ZQCAL START (ZQCST) OP[7:0] = 0000 0101b initiates the device's calibration procedure and ZQCAL LATCH (ZQCLH) OP[7:0] = 0000 0100b captures the result and loads it into the device drivers.

A ZQCAL START MPC command may be issued anytime the device is in a state in which it can receive valid commands. Two timing parameters are associated with ZQ Calibration: ^{t}ZQCAL and ^{t}ZQLAT. ^{t}ZQCAL is the time from when the ZQCAL START MPC command is sent to when the host can send the ZQCAL LATCH MPC command. ^{t}ZQLAT is the time from when the ZQCAL LATCH MPC command is sent by the host to when the CA bus (and subsequently the DQ bus) can be used for normal operation. A ZQCAL LATCH MPC command may be issued anytime outside of power-down after ^{t}ZQCAL has expired and all DQ bus operations have completed.

The CA bus must maintain a deselect (CS_n = HIGH) state during ^{t}ZQLAT to allow CA ODT calibration settings to be updated. After a ZQCAL START MPC command has been issued, neither another ZQCAL START nor a ZQCAL LATCH MPC command is allowed until ^{t}ZQCAL finishes.

Table 197: ZQ Calibration Timing Parameters

Parameter	Symbol	Min	Units
ZQ calibration time	^{t}ZQCAL	1	µs
ZQ calibration latch time	^{t}ZQLAT	max(30ns, 8CK)	ns

ZQ External Resistor, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240 ohm ±1% tolerance external resistor must be connected between ZQ and V_{SS}.

If the system configuration has more than one rank, and if the ZQ pins of both ranks are attached to a single resistor, the device controller must ensure that the ZQ calibrations for each rank do not overlap.

The total capacitive loading on the ZQ pin must not exceed the max external loading of 25pf, with the addition of the device ZQ pincap (5pf) for a total capacitive loading of 30pf.

Per-DRAM Addressability

Per-DRAM addressability (PDA) enables programming of a given device in a rank. For example, it can program different ODT or V_{ref} values on each device on a given rank. Per-DRAM addressability applies to MRW, MPC, VREFCA and VREFCS commands. Some per-DRAM settings are required prior to training the CA and CS timings and the DQ write timings. The MPC, VREFCA, and VREFCS command timings with extended setup/hold and multicycle CS assertion may be used for PDA commands if the CA and CS timings have not yet been trained.

DDR5 introduces a CA interface-only method for per-DRAM addressability by having a unique PDA enumerate ID programmable in each device in a rank and the ability to set a PDA select ID in the commands.

The unique PDA enumerate ID requires the use of the DQ0 signals of each device in the rank (DQL0 in the x16 configuration), and a PDA enumerate programming mode available through the MPC commands. The PDA enumerate ID and PDA select ID are 4-bit fields. Once the PDA enumerate ID is

programmed into a device, subsequent commands targeted to that device will not use the DQ0/DQL0 signal (legacy PDA method) to select the device for the commands. Instead, when the PDA select ID (MR1:OP[7:4]) is the same as the PDA enumerate ID (MR1:OP[3:0]), or when the PDA select ID is set to the all-DRAM code of 1111b, the device can be written with an MPC, MRW, VREFCA or VREFCS command. A few MPC commands do not use the PDA select ID to determine if the command is applied; among these are the MPC opcodes to set the PDA enumerate ID and the opcode to set the PDA select ID. During the reset procedure, the receive FIFO must be initialized with all 1s to ensure the PDA enumerate flow does not program an enumerate ID when the strobes are not toggling.

Table 198: Commands Supporting/Not Supporting PDA Select ID Usage

Command	Op-code	Uses PDA Select ID to Determine When to Execute Command	Note
MRW	All	Yes	
VREFCA	All	Yes	
VREFCS	All	Yes	
MPC	(Group A and B) RTT_CA	Yes	
MPC	(Group A and B) RTT_CS	Yes	
MPC	(Group A and B) RTT_CK	Yes	
MPC	Set RTT_PARK	Yes	
MPC	Set DQS_RTT_PARK	Yes	
MPC	Apply VREFCA, VREFCS, and RTT_CA/CS/CK	No	
MPC	Enter PDA enumerate programming mode	No	
MPC	Exit PDA enumerate programming mode	No	
MPC	PDA enumerate ID	No	1
MPC	PDA select ID	No	
MPC	All other MPC opcodes	No	

Notes: 1. The PDA enumerate ID op-code is the only MPC command that utilizes the PDA enumerate ID programming mode.

Table 199: PDA Mode Register Fields

MR Address	Operating Mode	Description
MR1:OP[3:0]	PDA enumerate ID[3:0]	This is a read-only MR field, which is only programmed through an MPC command with the PDA enumerate ID opcode. xxxxb encoding is set with MPC with the PDA enumerate ID opcode. This can only be set when PDA enumerate programming mode is enabled and the associated DQ0/DQL0 is asserted LOW. The PDA enumerate ID opcode includes four bits for this encoding. Default setting is 1111b.
MR1:OP[7:4]	PDA select ID[3:0]	This is a read-only MR field, which is only programmed through an MPC command with the PDA select ID opcode. xxxxb encoding is set with MPC with the PDA select ID opcode. The PDA select ID opcode includes four bits for this encoding. 1111b = all devices execute MRW, MPC, VREFCS, and VREFCA. For all other encodings, devices execute MRW, MPC, VREFCS, and VREFCA only if PDA select ID[3:0] = PDA enumerate ID[3:0], with some exceptions for specific MPC commands that execute regardless of PDA select ID. Default setting is 1111b.

PDA Enumerate ID Programming

1. PDA enumerate programming mode is enabled by sending one or more MPC command cycles with OP[7:0]=0000 1011b. Data mask and PDA enumerate are not supported for use at the same time. Either data mask is disabled or DM_n driven HIGH while PDA enumerate programming mode is enabled.
2. In the PDA enumerate programming mode, only the MPC command with PDA enumerate ID op-code is qualified with DQ0 for x4/x8 and DQL0 for x16. The device captures DQ0 for x4/x8 using DQS_c and DQS_t, and DQL0 for x16 by using DQSL_c and DQSL_t (as shown in the figure below) when DQ is driven LOW after the PDA enumerate ID opcode is set via the MPC command, and DQS starts toggling after ^{t}PDA_DQS_DELAY (MIN) but prior to ^{t}PDA_DQS_DELAY (MAX), and DQ is held until after DQS stops toggling.
   An alternate method is shown in the Self-Refresh Entry/Exit Timing with 2-Cycle Exit Command figure, where DQ is driven LOW and DQS toggles continuously starting prior to the PDA enumerate ID opcode being set via the MPC command, and remains toggling until ^{t}PDA_DQS_Delay (MAX) is satisfied and the MPC command with exit PDA enumerate programming mode opcode has finished.
   If the value on DQ0/DQL0 is LOW, the device executes the MPC command to set the PDA enumerate ID. If the signal on DQ0/DQSL0 is HIGH, the device ignores the MPC command. The controller may choose to drive all the DQ bits. Only the PDA enumerate ID opcode with MPC command are supported during the enter/exit PDA enumerate programming mode. The exit PDA enumerate program mode opcode with MPC command does not require a DQ qualification (DQ0/DQL0 will be ignored).
3. For the "don't enumerate" case where a device is to ignore the MPC command with PDA enumerate ID opcode, the DQS_t/DQS_c and DQ signals (DQSL_t/DQSL_c and DQL/DQU for x16) may be HIGH (either driven or due to RTT_PARK termination) prior to sending the enter PDA enumerate program mode op-code via MPC command. After entering PDA enumerate programming mode, the DQ and DQS signals must remain HIGH until exiting PDA enumerate programming mode. Holding the signals HIGH will ensure this device is not programmed with a PDA enumerate ID, other than the default setting of 0xFh. See the timing diagram showing the “don’t enumerate” case.

Table 200: PDA Enumerate Results

DQS_t/c for x4/x8 (DQSL_t/c for x16)	DQ0 for x4/x8 (DQL0 for x16)	PDA Enumerate Result	Notes
Toggling	LOW	Enumerate	
Toggling	HIGH	Don't Enumerate	
HIGH	LOW	Unknown	1
HIGH	HIGH	Don't Enumerate	2
Differentially LOW	Valid	Don't Enumerate	3

Notes: 1. DQS_t/c are differential signals and small amounts of noise could appear as toggling, resulting in an unknown state for the PDA enumerate result.
2. The expected usage case where the DQS signals are HIGH is to have the DQ signals HIGH as well.
3. Differentially LOW is defined as DQS_t/DQSL_t = LOW and DQS_c/LDQS_c = HIGH.

4. A minimum of one complete BL16 set of strobe edges (8 rising edges and 8 falling edges) must be sent by the host within the ^{t}PDA_DQS_DELAY (MIN)/(MAX) range after the MPC command. The DQ value is captured during any strobe edge during the valid LOW duration of the target DQ. Valid LOW time is defined as the time between ^{t}PDA_S and ^{t}PDA_H. If the device captures a 0 on DQ0/DQL0 at any strobe edge in the strobe sequence, the MPC command initiated PDA enumerate

ID is executed. Because the write timings for the DQ bus have not been trained, the host must ensure a minimum of 16 strobe edges occur after a period of ^{t}PDA_DQS_Delay (MIN) after the associated MPC command. The BC8 OTF mode register setting in the device is ignored while in PDA enumerate programming mode. The DQS assumes preamble/postamble requirements.

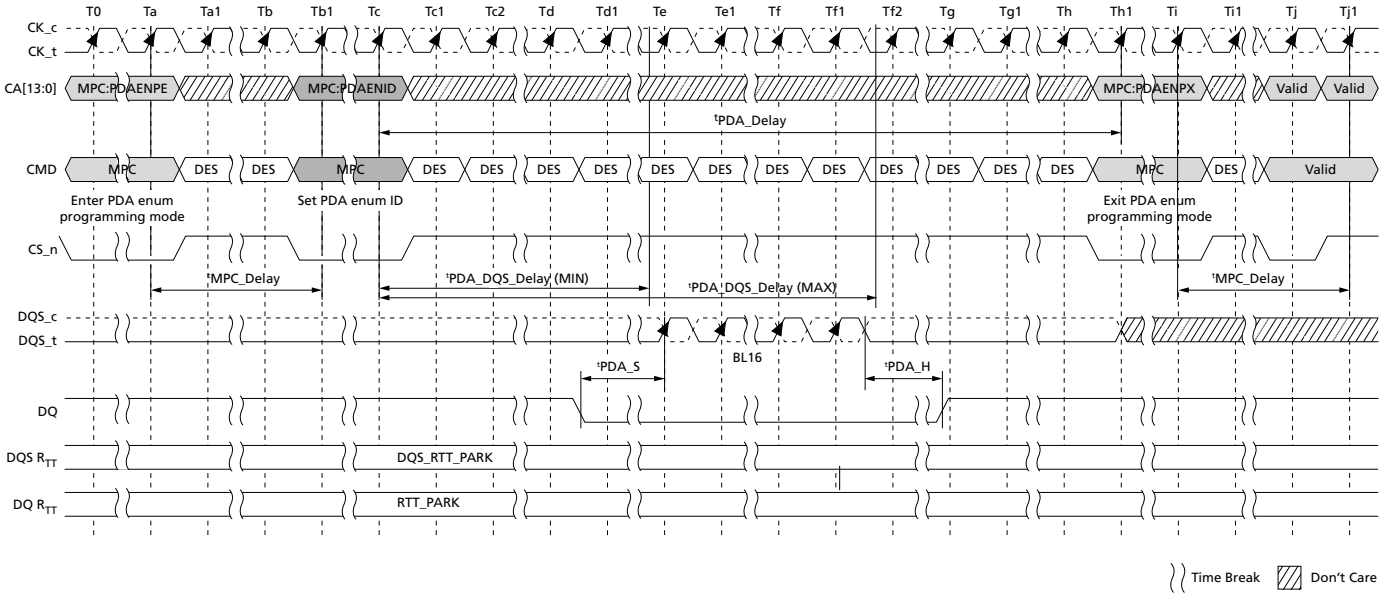
5. Prior to when the MPC command with enter PDA enumerate programming mode opcode is sent by the host, the host must drive DQS_t and DQS_c differentially LOW, other than when the burst of 16 strobe edges is sent in association with the PDA enumerate ID MPC command. The host must also include preamble and postamble DQS_t/DQS_c toggles during the qualification of the PDA command. Once PDA enumerate programming mode is enabled in the DRAM device, the host memory controller waits ^{t}MPC_Delay to the time the first PDA enumerate ID MPC command is issued.
6. In the PDA enumerate programming mode, only MPC commands to PDA enumerate ID opcode and exit PDA enumerate program mode opcode are allowed.
7. In the PDA enumerate programming mode, the default (or previously programmed) RTT_PARK value is applied to the DQ signals.
8. The cycle time for the MPC command with PDA enumerate ID opcode is defined as ^{t}PDA_Delay. This time is longer than the normal ^{t}MPC_Delay and must be met to provide time to latch the asserted DQ and complete the WRITE operation to the PDA enumerate ID mode register (MR1:OP[3:0]), prior to executing the next MPC command with PDA enumerate ID opcode (shown in figure below).
9. To remove the device from PDA enumerate programming mode, send an MPC command with exit PDA enumerate programming mode opcode (PDAENPX), OP[7:0]=0000 1010b. The MPC command with exit PDA enumerate programming mode opcode is never qualified by the DQ settings and is applied to all devices in the rank.
10. During the PDA enumerate ID programming mode, only one MPC command with PDA enumerate ID opcode is allowed to each device. Once the PDA enumerate ID is programmed, any change for the PDA enumerate ID requires the device to re-enter into PDA enumerate ID programming mode.

As an example, the following sequence programs the PDA enumerate ID per device:

1. Send MPC command with **enter PDA enumerate programming mode** opcode, OP[7:0]=0000 1011b.
2. For (i = 0, i < MAX_DRAMS, i++), send MPC command with PDA enumerate ID opcode with **i** in the lower four bits of the opcode (4-bit value), with device **i**'s DQ signals LOW.
3. Send MPC command with **exit PDA enumerate programming mode** opcode, OP[7:0]=0000 1010b.

The following figure shows a timing diagram for setting the PDA enumerate ID value for one device. In this case, only one device is programmed prior to exiting PDA enumerate programming mode, but many devices may be programmed prior to exiting this mode.

Figure 84: PDA Enumerate Programming Mode Entry, PDA Enumerate ID Programming, PDA Enumerate Programming Mode Exit



Notes: 1. The diagram assumes preamble/postamble requirements for DQS.
2. The second MPC command at Tb1 is assuming a multi-cycle command, and the timings are adjusted to visually show separation between spacing timings such as ^{t}MPC_Delay (which start at the end of a command cycle and end at the beginning of the next) and other timings such as ^{t}PDA_DELAY.

Figure 85: PDA Enumerate Programming Mode Entry with Continuous DQS Toggling

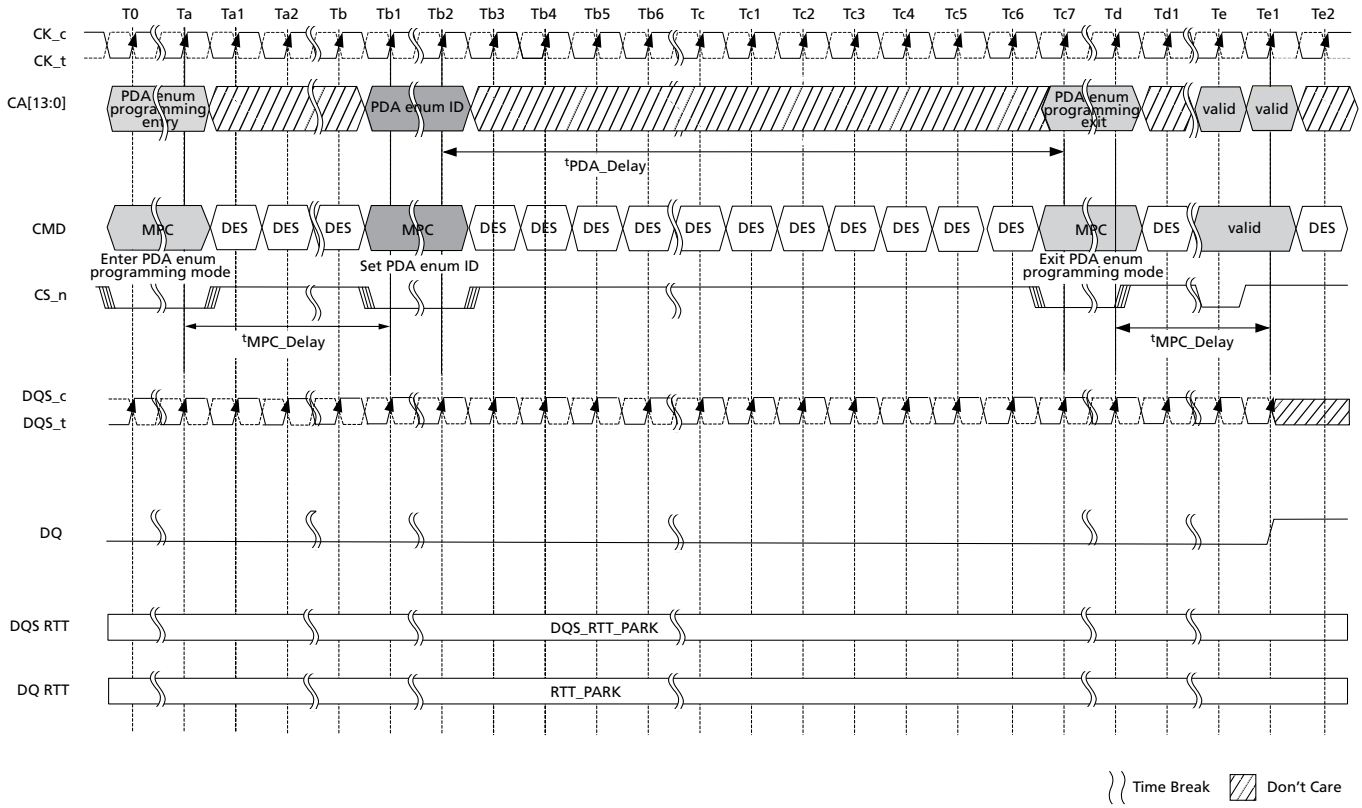
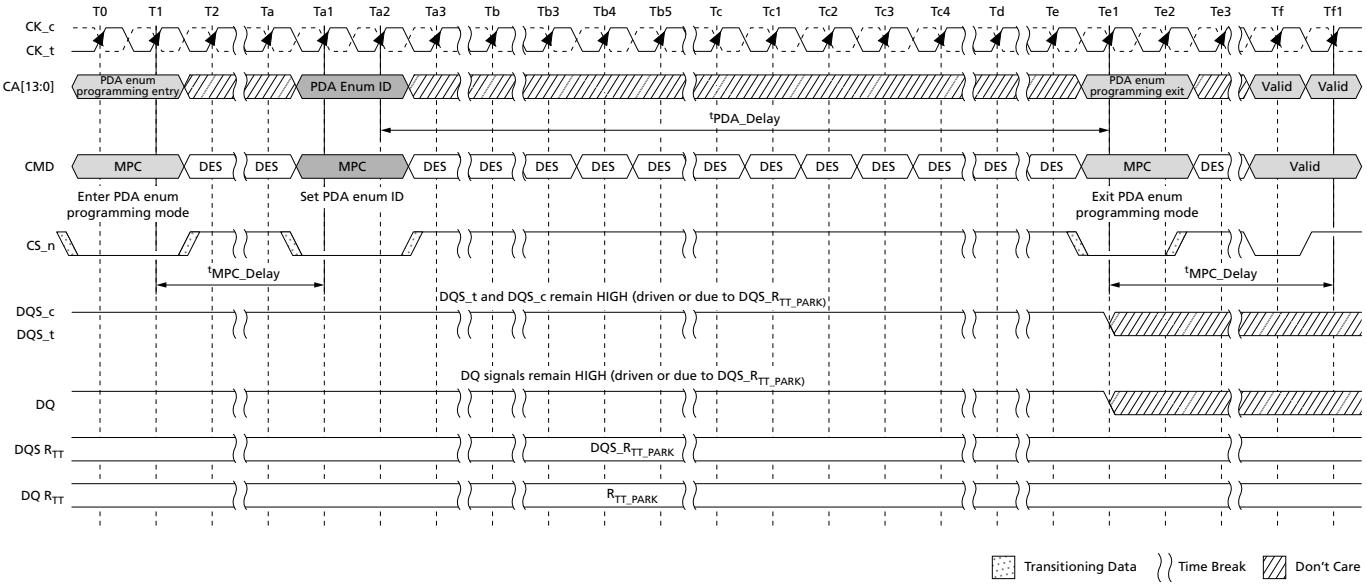


Figure 86: Don't Enumerate Case



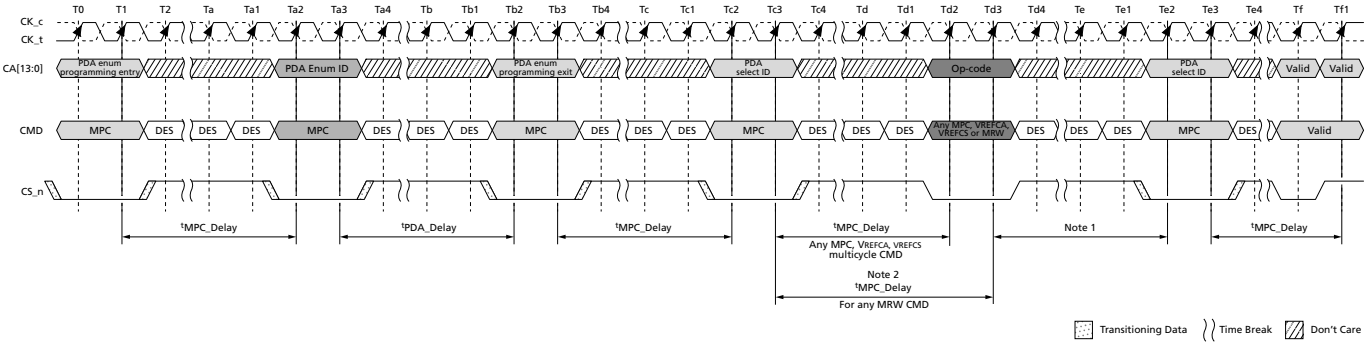
PDA Select ID Operation

Once the PDA enumerate IDs have been programmed in all devices, the execution of future MPC/MRW/VREFCA/VREFCS commands depends on the value of the PDA select ID and the type of MPC command. If PDA select ID = 1111b, all devices execute the command. For all MRW, VREFCA and VREFCS commands, and some of the MPC commands (RTT_CA/CS/CK and RTT_PARK opcodes), the PDA select ID is compared to the PDA enumerate ID to determine if the device executes the commands. For all other MPC commands (that is, not the RTT_CA/CS/CK and RTT_PARK opcodes), the device executes the command regardless of the PDA select ID value.

As an example, the following sequence could be used to program unique MR fields per device:

1. Send MPC with PDA select ID opcode, with encoding 0000 included in the opcode.
2. Send MRWs for field settings specific to device 0000. This can be any number of MRWs.
3. Send MPC with PDA select ID opcode, with encoding 0001 included in the opcode.
4. Send MRWs for field settings specific to device 0001. This can be any number of MRWs.
5. Repeat for any number of devices.
6. Send MPC with PDA select ID opcode, with encoding 1111 included in the opcode to enable all devices to execute all MRW, VREFCS, VREFCA, and MPC commands.

Figure 87: Multicycle MPC Command Sequencing with PDA Enumerate and PDA Select ID



Notes: 1. Commands used such as VREFCA, VREFCS, or MRW have different command spacing requirements. Refer to the command sections for details.
2. Any multicycle MPC, VREFCA or VREFCS command spacing is measured from the last valid command cycle to the first following valid command cycle, while standard command spacing goes from the last valid command cycle to the last valid command cycle. See MRW command period diagrams for details.

CS Training Mode

CS Training Mode (CSTM) facilitates the loopback of a sampled sequence of the CS_n signal.

In this mode, the CK is running and the CA signals are held in a NOP command encoding state. Once this mode is enabled and the devices are selected to actively sample and drive feedback, the device samples the CS_n signal on the rising edge of CK. Every set of four CK rising edge samples is included in a logical computation to determine the CSTM output result that is sent back to the host on the DQ bus. Once sampling begins, the device must maintain the consecutive grouping of the samples every 4^{t}CK. When the CS_n Sample[0] and Sample[2] result in a logic 0 and the CS_n Sample[1] and Sample[3] result in a logic 1, the device drives a 0 on all DQ signals. There is no requirement to drive any strobes, and the output signal could transition as often as every 4^{t}CK.

Entry and Exit

CSTM is enabled when the host sends the MPC command with enter CS training mode opcode (CSTMN) (OP[7:0] = 0000 0001B). Since CS training must occur prior to establishing alignment between CK and CS_n signals, the MPC command extends beyond multiple ^{t}CK cycles, during which the CS_n signal is asserted. This avoids causing the device to latch invalid commands, as might happen when the CS_n-to-CK setup time is not met. In this mode, commands are actively processed. The only commands that should be sent by the host memory controller while CSTM is enabled are the NOP command and the MPC command with exit CS training mode opcode (CSTMX), OP[7:0] = 0000 0000B. Any other command may produce unreliable results.

Once enabled, the device begins sampling on every rising CK edge, with the four sample groups looping consecutively. Depending on the value of the samples, the DQ signals are driven HIGH or LOW. Prior to entering CSTM, DQ signals are not driven by the device and are terminated according to the default RTT_PARK setting. Once enabled, the DQ signal begins driving the output values based on the CSTM samples. Once the DQ signals are driven by the device, RTT_PARK termination is no longer applied, similar to a READ operation.

To exit CSTM, a MPC command with exit CS training mode opcode (CSTMX) must be sent. Since the timing relationship between CS_n and CK is understood when exiting CSTM, the host can either send a multi-cycle CS_n assertion during the MPC command or a single ^{t}CK assertion.

Operation

In CSTM, the CS_n values are sampled on all CK rising edges. Each group of four consecutive samples is evaluated in pairs, and then the two pairs are combined with a logical OR prior to sending to the DQ output. The samples evaluation to determine the output is as follows:

Table 201: Sample Evaluation for Intermediate Output [0]

Intermediate Output[0]	CS_n Sample[0]	CS_n Sample[1]
1	0	0
0	0	1
1	1	0
1	1	1

Table 202: Sample Evaluation for Intermediate Output [1]

Intermediate Output[1]	CS_n Sample[2]	CS_n Sample[3]
1	0	0
0	0	1
1	1	0
1	1	1

Table 203: Sample Evaluation for Final CSTM Output

CSTM Output[1]	Intermediate Output[0]	Intermediate Output[1]
0	0	0
1	0	1
1	1	1

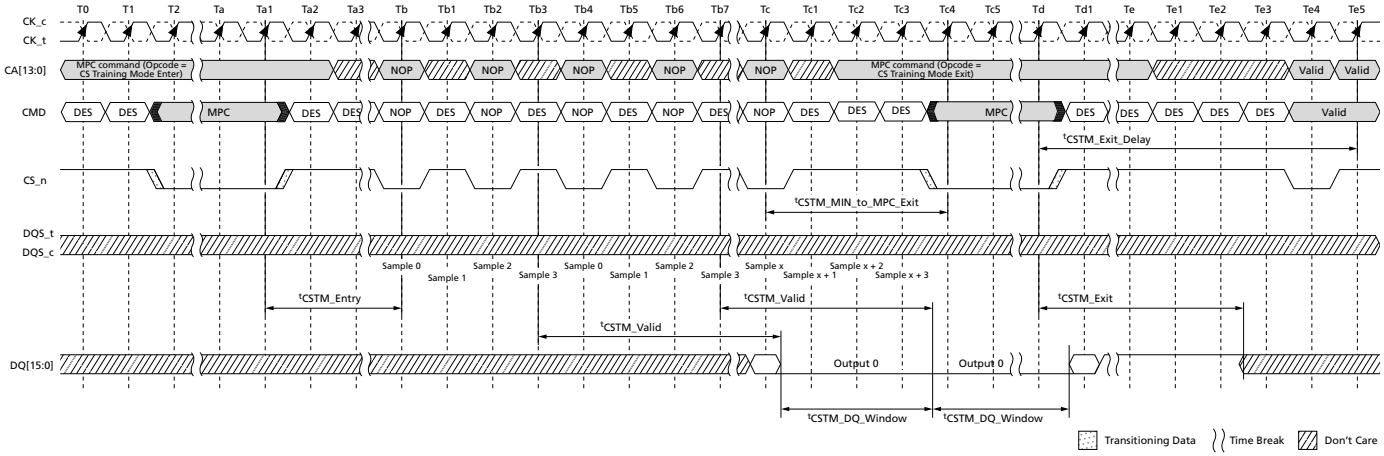
Table 203: Sample Evaluation for Final CSTM Output (Continued)

CSTM Output[1]	Intermediate Output[0]	Intermediate Output[1]
1	1	0

Notes: 1. When there is no change on the CSTM output from previous evaluation, DQ will continue to drive the same value continuously with no switching on the bus.

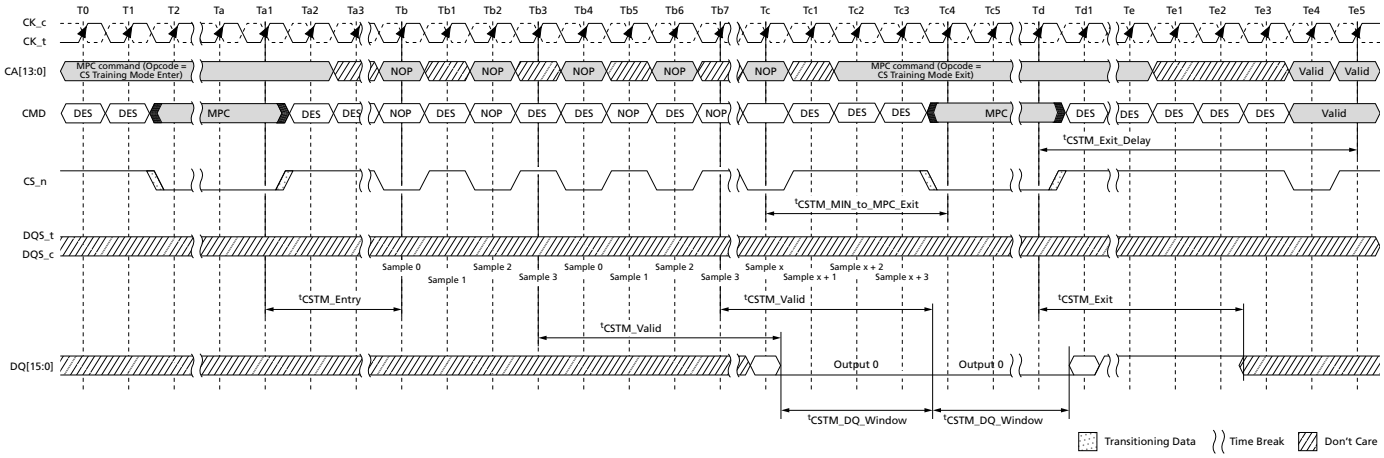
During CSTM, CA ODT is enabled as with a functional operation. The V_{refCS} is set according to the functional setting (using the VREFCS command). The delay from when the CS signals are sampled during the fourth CK rising edge (Sample[3]), to when the output of the sample evaluation is driven to a stable value on the DQ pins, is specified as ^{t}CSTM_Valid, as shown in the following figure. The details of the ^{t}CSTM_entry, ^{t}CSTM_exit, and ^{t}CSTM_DQ_Window are also illustrated.

Figure 88: Timing Diagram for CSTM with Consecutive Output Samples = 0



The following figure illustrates an example where the DQ output switches from a logic 0 to a logic 1, demonstrating the minimum ^{t}CSTM_DQ_Window.

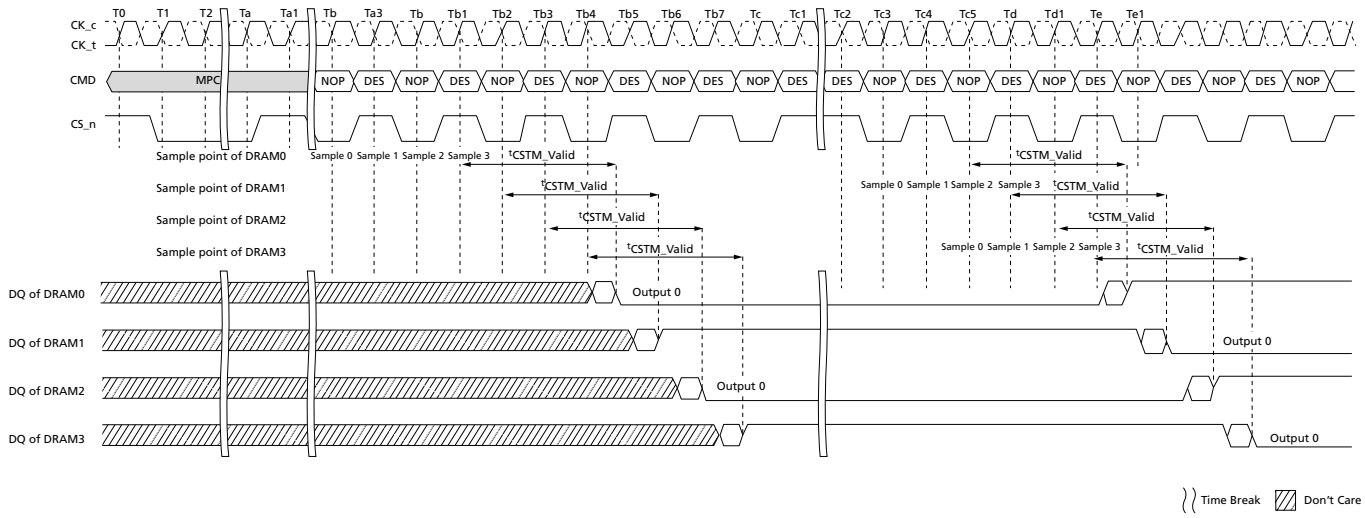
Figure 89: Timing Diagram for CSTM with Consecutive Output Sample Toggle



Notes: 1. See MPC Command for details on setup, hold and command register time.
2. The CA bus must meet setup and hold times on any clock where it is possible that CS_n might be sampled LOW while in CS training mode.

When the host trains CS_n timing for the device by using CSTM, CS_n sampling timing for each DRAM could be different from each other because the variation of internal timing is different for each DRAM. Therefore, even though the CS setup/hold time is appropriate for each DRAM, 4^{t}CK CS_n sampling window, which may have different starting points, could appear differently as shown in the following figure. The host should train CS_n timing based on asserting every edge of CS_n to cover multiple devices without exiting CSTM.

Figure 90: Timing Diagram for CSTM with Multiple DRAMs Output Sample Toggle



Note: 1. See MPC Command for details on setup, hold and command register time.

Output Signals

The following table shows which signals transmit the output of the CSTM loopback sample evaluation. These values are driven asynchronously, but may switch as often as every 4^{t}CK.

Table 204: CS Sampled Output per Interface Width

Output	x16	x8	x4
DQ0	CSTM Output	CSTM Output	CSTM Output
DQ1	CSTM Output	CSTM Output	CSTM Output
DQ2	CSTM Output	CSTM Output	CSTM Output
DQ3	CSTM Output	CSTM Output	CSTM Output
DQ4	CSTM Output	CSTM Output	
DQ5	CSTM Output	CSTM Output	
DQ6	CSTM Output	CSTM Output	
DQ7	CSTM Output	CSTM Output	
DML			
TDQS_c			
DQSL_t			
DQSL_c			
DQ8	CSTM Output		

Table 204: CS Sampled Output per Interface Width (Continued)

Output	x16	x8	x4
DQ9	CSTM Output		
DQ10	CSTM Output		
DQ11	CSTM Output		
DQ12	CSTM Output		
DQ13	CSTM Output		
DQ14	CSTM Output		
DQ15	CSTM Output		
DMU			
DQSU_t			
DQSU_c			

CA Training Mode

CA Training Mode (CATM) is a method to facilitate the loopback of a logical combination of sampled CA[13:0] signals.

In this mode, the CK is running and CS_n qualifies when the CK samples the CA signals. A loopback equation that includes all of the CA signals results in an output value that is sent asynchronously on the DQ signals back to the host memory controller. The host timings between CS_n, CK, and CA[13:0] signals can then be optimized for proper alignment. In this mode, no functional commands are executed in the device. The functional command interface is restored only after exiting this mode, which requires a CS_n assertion of two or more consecutive ^{t}CK. Prior to entering CATM, the CS_n signal must be aligned to the CK to meet the CS_n-to-CK timing specifications. This assumes CS training has been completed to determine the correct CS_n timings on the host, so the timing window for the CS to be met to ensure enough setup or hold timing margin prior to entering command/address training mode. Chip select training, through CSTM, can be used to accomplish this.

Entry and Exit

CATM is entered by sending an MPC command with enter CA training mode op-code (OP[7:0] = 0000 0011b). Once this MPC command executes, no other commands are interpreted by the device. Only the sampling of the CA signals, evaluation of the XOR result, and loopback to the DQs occurs. While in CATM, the CS_n signal asserts only for a single ^{t}CK at a time. The maximum sampling rate on the CA signals is every 4^{t}CK. CATM is disabled by asserting CS_n for two or more cycles up to eight cycles in a row while sending a NOP command on the CA bus.

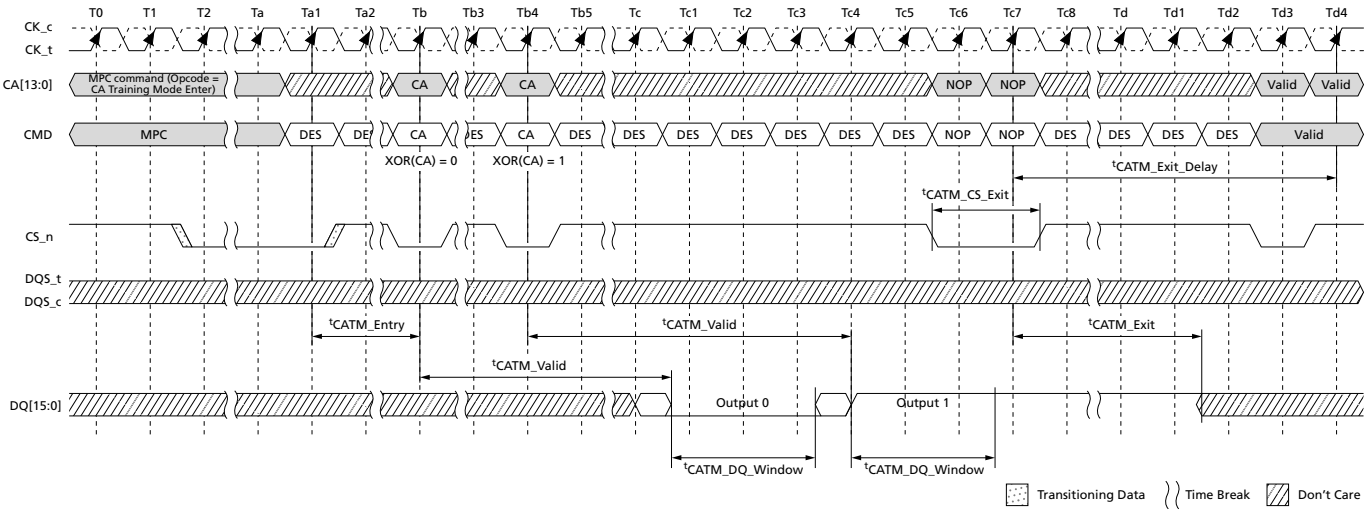
Operation

In CATM, the CA values are sampled in the same way as with functional operation, where the CS_n qualifies which cycle the sampling occurs and the sample is captured by the rising CK edge. Unlike functional operation, there is no concept of multiple cycle commands in CATM. Sampling of the CA signals occurs only when CS_n is asserted LOW. Once the CA signals are sampled, the values are XOR'd to produce an output value. This output value is driven on all the DQ pins, as a pseudo-static value. These output values are held until the next sample is captured on the CA bus, according to the CS_n assertion.

During CATM, the CA ODT is enabled as with a functional operation. The V_{refCA} is set according to the functional setting (through the VREFCA command). The timing requirements for the CA bus (CK_t, CK_c, and CS_n) are the same as with a functional operation.

The delay from when the CA signals are sampled during the CS_n assertion and when the output of the XOR computation is driven on the DQ pins is specified as ^{t}CATM_Valid, as shown in the following figure. CS_n may be asserted every 4^{t}CK, and thus, the CA XOR output may transition every 4^{t}CK. The following figure demonstrates an example where two CS_n assertions occur within 4^{t}CK. The device exits CATM when CS_n is asserted for two or more consecutive cycles, but limited to eight cycles.

Figure 91: CA Training Mode



CA Loopback Equation

CATM output is computed based on the CS_n assertion and the values of the CA inputs. The following table clarifies the output computation.

Table 205: CATM Output

CS_n	CATM Output	Notes
0	XOR(CA[13:0])	1
1	Hold previous value	

Notes: 1. The XOR function occurs after mirroring/inversion recovery, and only includes signals supported on the device (that is, may not include CA[13], depending on density (including stacking). If CA[13] is not needed for the device's density, the logical value is considered 0 for the XOR computation, though as indicated in the pin description table for MIR, the ball location associated with CA13's logical input (which switches with CA12) will be connected to V_{DDQ}.

Output Equations

The following table shows which signals transmit the output of the CATM loopback equation. These values are driven asynchronously as pseudo-static values, updating with a new output at a time ^{t}CAT-M_Valid after each CS_n assertion.

Table 206: Output Equations per Interface Width

Output	x16	x8	x4
DQ0	CATM Output	CATM Output	CATM Output
DQ1	CATM Output	CATM Output	CATM Output
DQ2	CATM Output	CATM Output	CATM Output
DQ3	CATM Output	CATM Output	CATM Output
DQ4	CATM Output	CATM Output	
DQ5	CATM Output	CATM Output	
DQ6	CATM Output	CATM Output	
DQ7	CATM Output	CATM Output	
DML			
TDQS_c			
DQSL_t			
DQSL_c			
DQ8	CATM Output		
DQ9	CATM Output		
DQ10	CATM Output		
DQ11	CATM Output		
DQ12	CATM Output		
DQ13	CATM Output		
DQ14	CATM Output		
DQ15	CATM Output		
DMU			
DQSU_t			
DQSU_c			

VREFCS Command

The V_{REFCS} voltage level should be set, if needed, prior to training the CS_n and CA bus timings relative to CK. The device supports a single UI command, VREFCS, specifically for setting the internal V_{REFCS} voltage level. This avoids any timing and/or default V_{REFCS} setting issues when sending a 2UI MRW command, by enabling the host to extend the setup and hold time for the CA signals. The VREFCS command also supports multiple cycles of CS_n assertion. The multiple cycles of CS_n assertion ensure the DRAM captures the VREFCS command during at least one rising edge of the differential CK (CK_t - CK_c).

NOTE: The operation, functionality and timings for VREFCS are effectively the same as VREFCA with the exception of the command name, and the fact that it modifies the internal reference voltage level of the chip select (CS_n) pin vs. the CA pins.

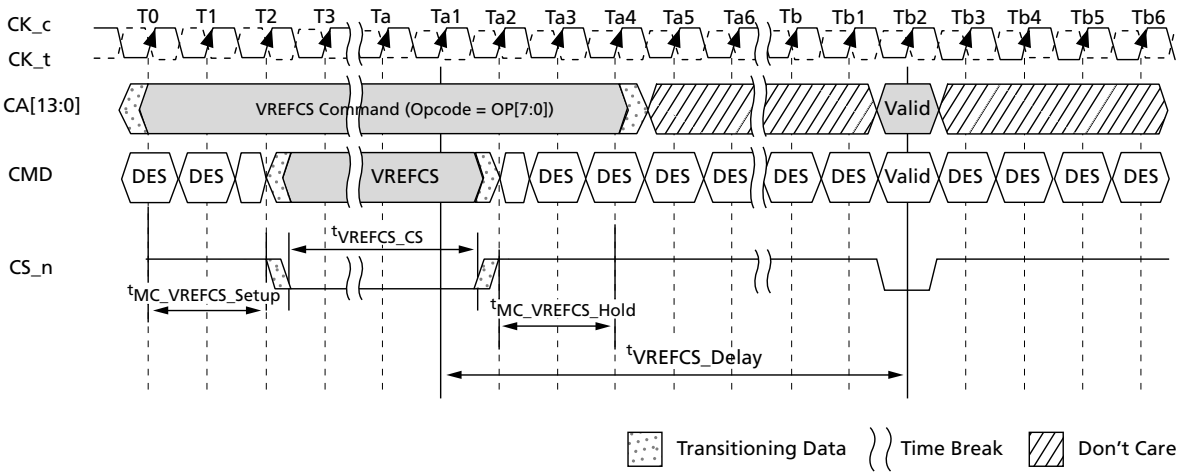
VREFCS Command Timing

The following diagram illustrates a timing sequence example for the VREFCS command that occurs prior to CS and CA training. The command is sampled on every rising edge of CK.

The host must ensure that the CA signals are valid during the entire CS_n assertion time. The timing of the CS_n assertion may not satisfy the setup/hold requirements around all CK transitions, but it will satisfy the setup/hold requirements relative to at least one rising edge of CK.

There is no separate mode that enables the multicycle CS_n assertion. This timing relationship can always be used by the host to send the VREFCS commands even after training has been completed for the interface. To latch the VREFCS command in cases where the alignment between CS_n, CA, and CK may be unknown, the CA inputs must reach the proper command state at least three cycles prior to CS_n transitioning from HIGH to LOW, CS_n must remain LOW for ^{t}VREFCS_CS, and CA must remain in the proper command state for at least three cycles after CS_n transitions from LOW to HIGH.

Figure 92: VREFCS Command Timing



The following table lists the timing parameters for the VREFCS command.

Table 207: AC Parameters for VREFCS Command

Symbol	Description	MIN	MAX	Unit	Note
^{t}VREFCS_DELAY	VREFCS command to any other valid command delay	^{t}MRD	-	nCK	
^{t}VREFCS_CS	Time CS_n is held low to register VREFCS command	3.5	8	nCK	1, 2

Notes: 1. Multiple cycles are used to avoid metastability of CS_n.
2. At the end of CSTM, it is assumed that the host should be able to place the CS_n appropriately and the VREFCS command could be issued as a single-cycle command.

VREFCA Command

The V_{REFCA} voltage level must be set prior to training the CS_n and CA bus timings relative to CK. The device supports a single UI command, VREFCA, specifically for setting the internal V_{REFCA} voltage

level. This avoids any timing and/or default V_{REFCA} setting issues when sending a 2UI MRW command, by enabling the host to extend the setup and hold time for the CA signals. The VREFCA command also supports multiple cycles of CS_n assertion. The multiple cycles of CS_n assertion ensures the device captures the VREFCA command during at least one rising edge of the differential CK (CK_t - CK_c).

VREFCA Command Timing

The figure below illustrates a timing sequence example for the VREFCA command that occurs prior to CS and CA training. The command is sampled on every rising edge of CK.

The host must ensure that the CA signals are valid during the entire CS_n assertion time. The timing of the CS_n assertion may not satisfy the setup/hold requirements around all CK transitions, but it will satisfy the setup/hold requirements relative to at least one rising edge of CK.

There is no separate mode that enables the multicycle CS_n assertion. This timing relationship can always be used by the host to send the VREFCA commands even after training has been completed for the interface. To latch the VREFCA command in cases where the alignment between CS_n, CA, and CK may be unknown, the CA inputs must reach the proper command state at least three cycles prior to CS_n transitioning from HIGH to LOW, CS_n must remain LOW for ^{t}VREFCA_CS, and CA must remain in the proper command state for at least three cycles after CS_n transitions from LOW to HIGH.

Figure 93: VREFCA Command Timing

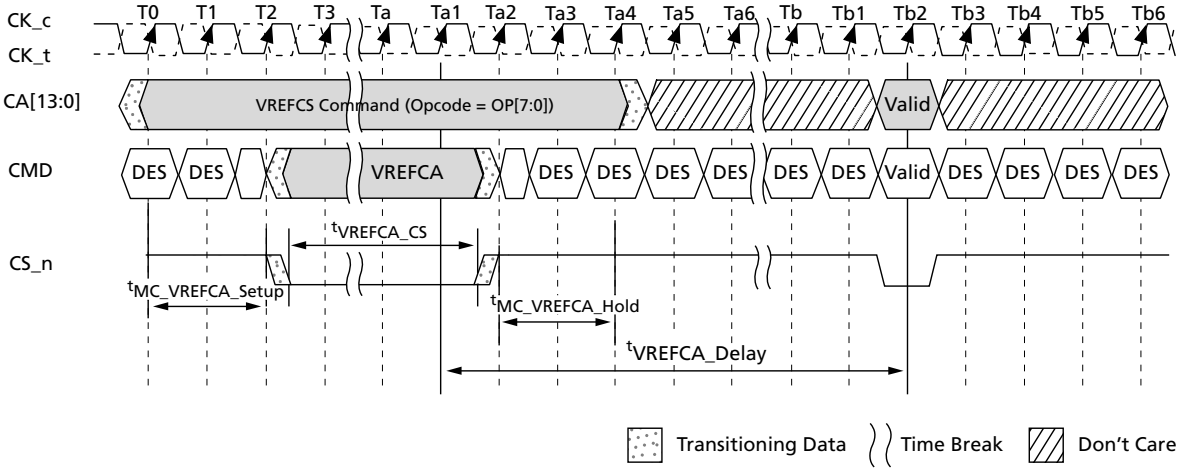


Table 208: AC Parameters for VREFCA Command

Symbol	Description	Min	Max	Unit	Note
^{t}VREFCA_DELAY	VREFCA command to any other valid command delay	^{t}MRD	-	nCK	
^{t}VREFCA_CS	Time CS_n is held low to register VREFCA command	3.5	8	nCK	1, 2

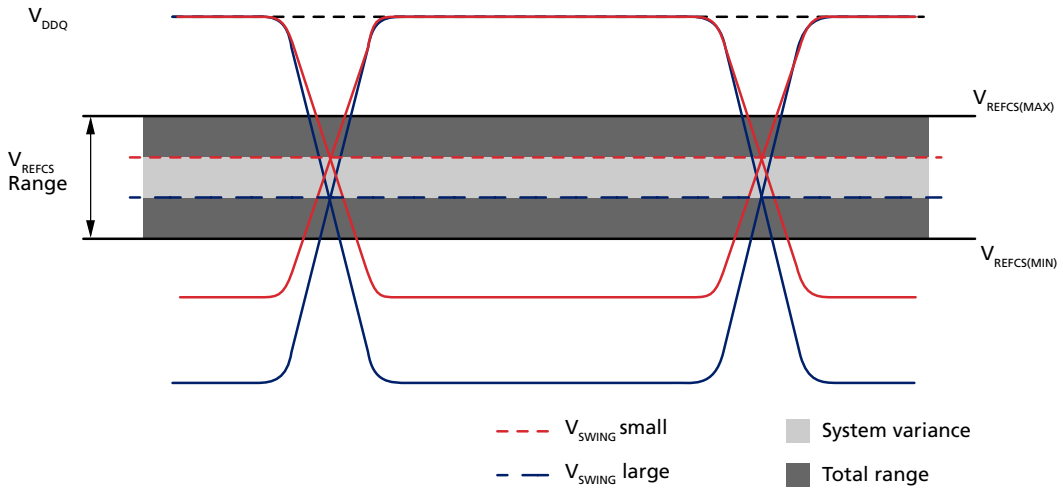
Notes: 1. Multiple cycles are used to avoid metastability of CS_n.
2. At the end of CSTM, it is assumed that the host should be able to place the CS_n appropriately and the VREFCA command could be issued as a single-cycle command.

V_{REFCS} Training

The internal V_{REFCS} specification parameters include operating voltage range, step size, step tolerance, step time, and valid voltage levels.

The operating voltage range specifies the minimum required V_{REFCS} setting ranges. These minimum setting ranges are defined by $V_{REFCS(MIN)}$ to $V_{REFCS(MAX)}$ as depicted in the following figure.

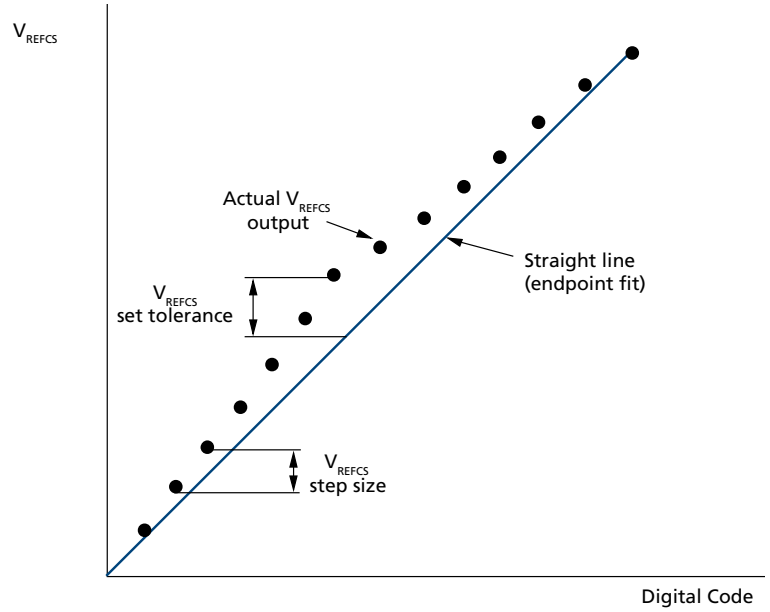
Figure 94: V_{REFCS} Operating Ranges



The step size is defined as the size between adjacent steps. For a given design, the DRAM V_{REFCS} step sizes must be within the specified range.

The set tolerance is the variation in the V_{REFCS} voltage levels from the ideal settings. This accounts for accumulated error over multiple steps. There are two ranges for set tolerance uncertainty. The range of set tolerance uncertainty is a function of number of steps *n*. The set tolerance is measured with respect to the ideal line, which is based on the two endpoints, $V_{REFCS(MIN)}$/$V_{REFCS(MAX)}$, for the specified ranges.

Figure 95: V_{REFCS} Set Tolerance and Step Size Example – MAX Case



The increment/decrement step times are defined by V_{REFCS_time}, which is defined from t0 tot1 (shown below), where t1 is referenced to when the V_{REFCS} voltage is at the final DC level within the V_{REFCS} valid tolerance ($V_{REFCS\_val\_tol}$).

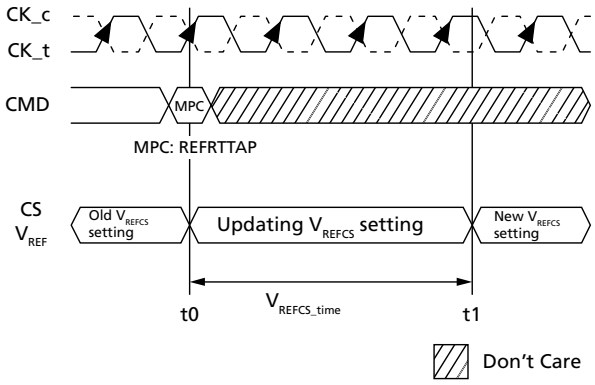
The V_{REFCS} valid level is defined by the valid tolerances to qualify the step time t1, as shown in the following figures. This parameter is used to ensure an adequate RC time constant behavior of the voltage level change after any V_{REFCS} increment or decrement adjustment, and are only applicable for DRAM component-level validation/characterization.

V_{REFCS} time is the time including up to $V_{REFCS,\ min}$ to $V_{REFCS,\ max}$ or $V_{REFCS,\ max}$ to $V_{REFCS,\ min}$ change in V_{REFCS} voltage.

t0 is referenced to MPC APPLY VREFCS and RTT_CA/CS/CK commands.

t1 is referenced to $V_{REFCS\_val\_tol}$.

Figure 96: V_{REFCS_time} Timing



A VREFCS command is used to store the V_{REF} values into the V_{REFCS} mode register (MR12). This mode register is only programmed via the command but is readable via a normal MRR.

Table 209: V_{REFCS} Mode Register

MR Address	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR12	Valid	V_{REFCS} calibration value						

Figure 97: V_{REFCS} Step, Single Step Size Increment Example

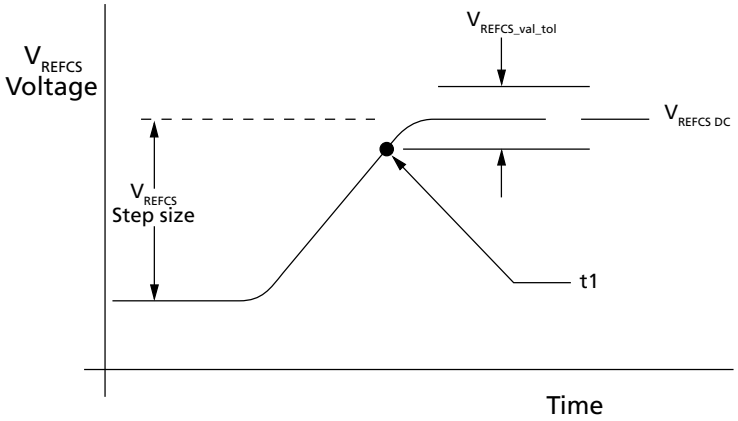


Figure 98: V_{REFCS} Step, Single Step Size Decrement Example

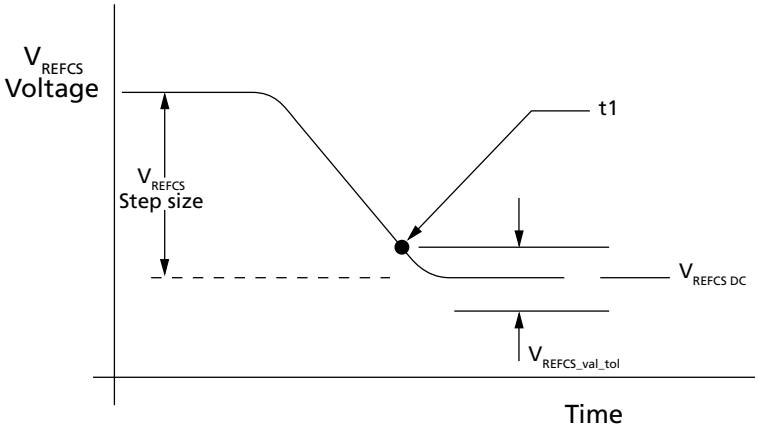


Figure 99: V_{REFCS} Full Step from $V_{REFCS(MIN)}$ to $V_{REFCS(MAX)}$ Example

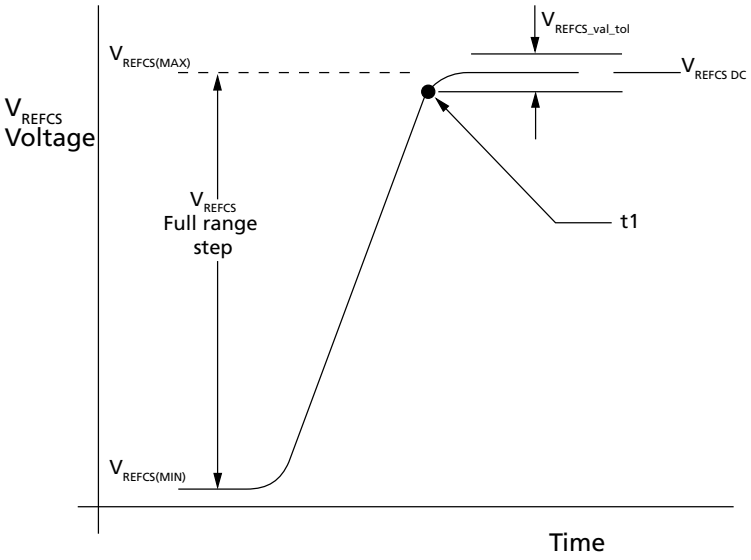


Figure 100: V_{REFCS} Full Step from $V_{REFCS(MIN)}$ to $V_{REFCS(MAX)}$ Example

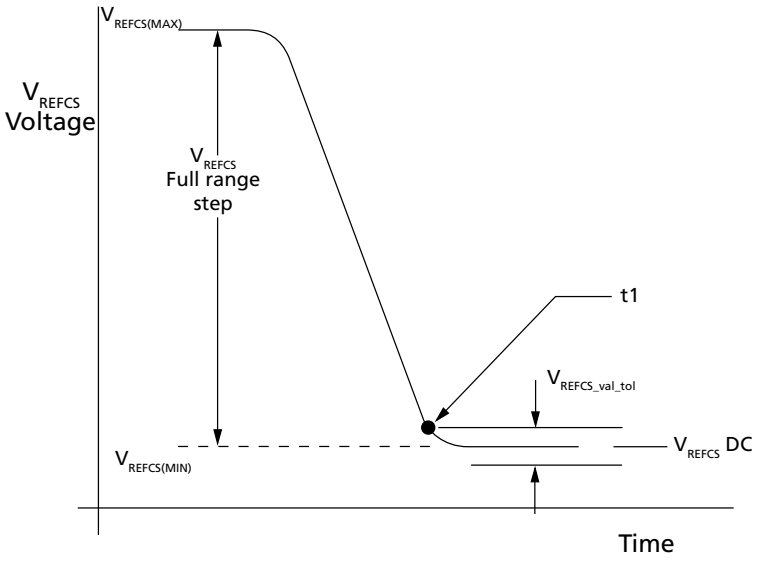


Table 210: Internal V_{REFCS} Specifications

Parameter	Symbol	MIN	TYP	MAX	Unit	Notes
$V_{REFCS(MAX)}$ operating point	$V_{REFCS(MAX)}$	97.5%	–	–	V_{DDQ}	1
$V_{REFCS(MIN)}$ operating point	$V_{REFCS(MIN)}$	–	–	45%	V_{DDQ}	1
V_{REFCS} step size	V_{REFCS_step}	0.41%	0.50%	0.59%	V_{DDQ}	2
V_{REFCS} set tolerance	$V_{REFCS\_set\_tol}$	–1.625%	0.00%	1.625%	V_{DDQ}	3, 4, 6
		–0.15%	0.00%	0.15%	V_{DDQ}	3, 5, 7
V_{REFCS} step time	V_{REFCS_time}	–	–	300	ns	8
V_{REFCS} valid tolerance	$V_{REFCS\_val\_tol}$	–0.15%	0.00%	0.15%	V_{DDQ}	9

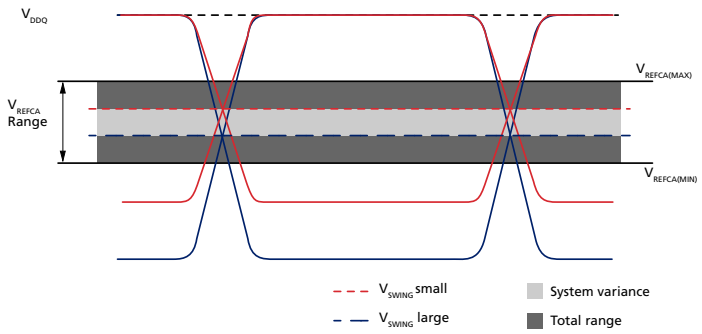
Notes: 1. V_{REFCS} DC voltage reference to V_{DDQ_DC}.
2. V_{REFCS} step size increment/decrement range. V_{REFCS} at DC level.
3. $V_{REFCS\_new\text{-}setting} = V_{REFCS\_old\text{-}setting}$+/- n * V_{REFCS_step}; n = number of steps; if increment use +; if decrement use -.
4. The minimum value of V_{REFCS} setting tolerance = $V_{REFCS\_new\text{-}setting}$ - 1.625% * V_{DDQ}. The maximum value of V_{REFCS} setting tolerance = $V_{REFCS\_new\text{-}setting}$ + 1.625% * V_{DDQ} for n>4.
5. The minimum value of V_{REFCS} setting tolerance = $V_{REFCS\_new\text{-}setting}$ - 0.15% * V_{DDQ}. The maximum value of V_{REFCS} setting tolerance = $V_{REFCS\_new\text{-}setting}$ + 0.15% * V_{DDQ} for n<=4.
6. Measured by recording the minimum and maximum values of the V_{REFCS} output over the range, drawing a straight line between those points and comparing all other V_{REFCS} output settings to that line.
7. Measured by recording the minimum and maximum values of the V_{REFCS} output across four consecutive steps (n = 4), drawing a straight line between those points and comparing all other V_{REFCS} output settings to that line.
8. Time from MPC command with Apply VREFCS and RTT_CA/CS/CK opcodes to increment or decrement.
9. Only applicable for DRAM component-level test/characterization purpose. Not applicable for normal mode of operation. V_{REFCS} valid is to qualify the step times which will be characterized at the component level.

V_{REFCA} Training

The internal V_{REFCA} specification parameters include operating voltage range, step size, step tolerance, step time, and valid voltage levels.

The operating voltage range specifies the minimum required V_{REFCA} setting range. These minimum setting ranges are defined by $V_{REFCA,min}$ to $V_{REFCA,max}$, as depicted in the following figure.

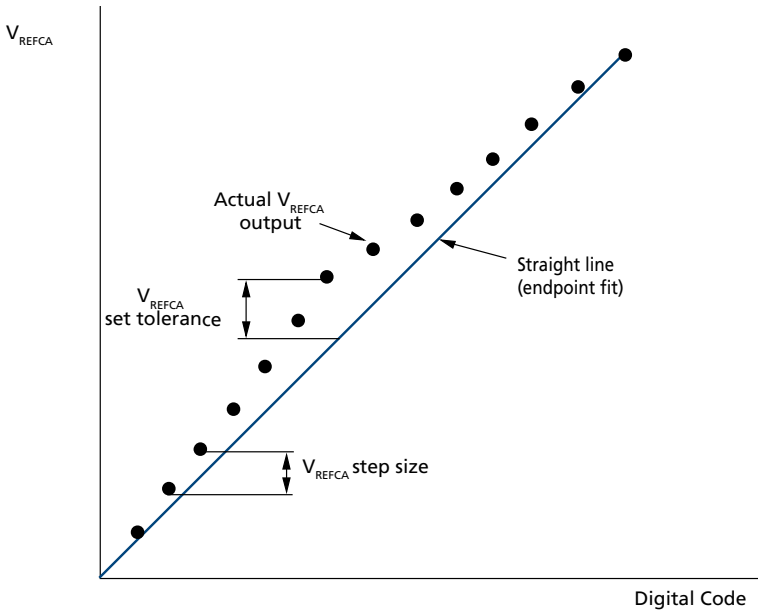
Figure 101: V_{REFCA} Operating Ranges



The step size is defined as the size between adjacent steps. For a given design, the DRAM V_{REFCA} step size must be within the specified range.

The set tolerance is the variation in the V_{REFCA} voltage levels from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for set tolerance uncertainty. The range of set tolerance uncertainty is a function of number of steps *n*. The set tolerance is measured with respect to the ideal line, which is based on the two endpoints, $V_{REFCA,min}$ and $V_{REFCA,max}$, for the specified ranges.

Figure 102: V_{REFCA} Set Tolerance and Step Size Example – MAX Case



The increment/decrement step times are defined by $V_{REFCA,time}$, which are defined from t0 tot1 (shown below), where t1 is referenced to when the VREFCA voltage is at the final DC level within the VREFCA valid tolerance ($V_{REFCA\_val\_tol}$).

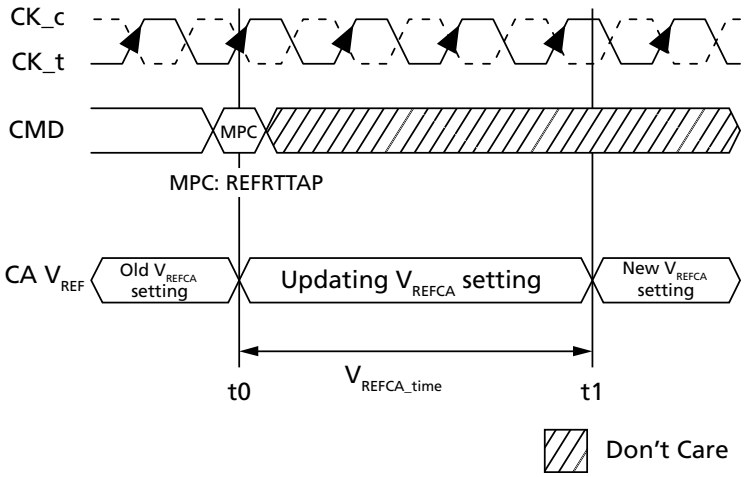
The valid level is defined by the valid tolerances to qualify the step timet1, as shown in the following figures. This parameter is used to ensure an adequate RC time constant behavior of the voltage level change after any V_{REFCA} increment or decrement adjustment, and are only applicable for DRAM component-level validation/characterization.

V_{REFCA} time is the time including up to $V_{REFCA,min}$ to $V_{REFCA,max}$ or $V_{REFCA,max}$ to $V_{REFCA,min}$ change in V_{REFCA} voltage.

t0 is referenced to MPC APPLY VREFCA and RTT_CA/CS/CK commands.

t1 is referenced to $V_{REFCA\_val\_tol}$.

Figure 103: V_{REFCA_time} Timing



A VREFCA command is used to store the V_{REF} value into the V_{REFCA} mode register, MR11. This mode register is only programmed via the command but is readable via a normal MRR.

Table 211: V_{REFCA} Mode Register

MR Address	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR11	Valid	V_{REFCA} calibration value						

Figure 104: V_{REFCA} Step, Single Step Size Increment Example

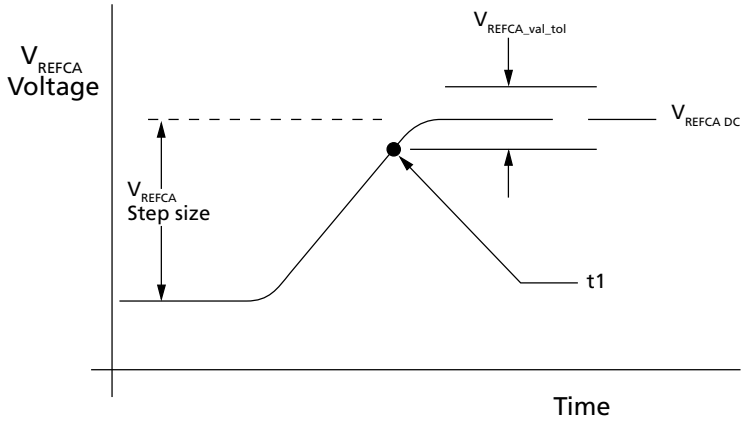


Figure 105: V_{REFCA} Step, Single Step Size Decrement Example

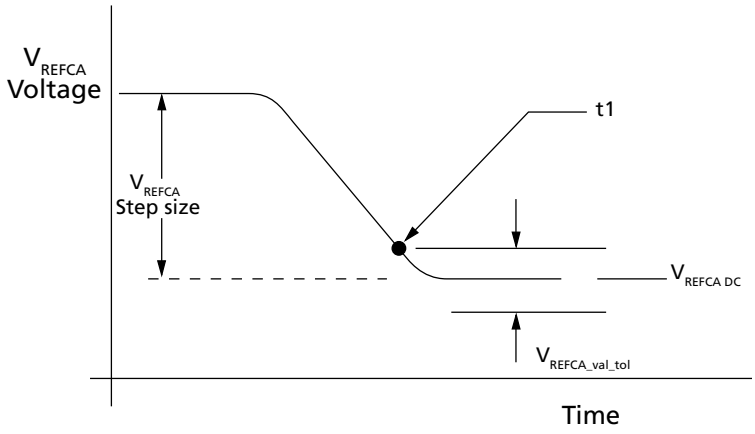


Figure 106: V_{REFCA} Full Step from $V_{REFCA(MIN)}$ to $V_{REFCA(MAX)}$ Example

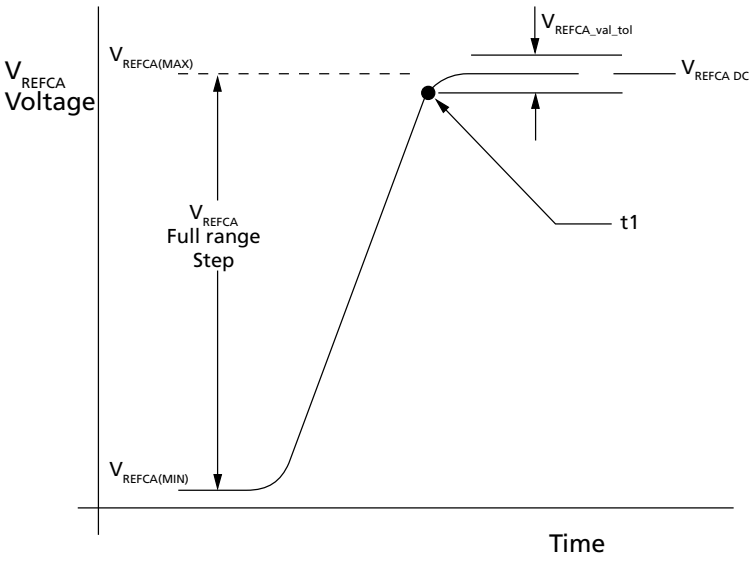


Figure 107: V_{REFCA} Full Step from $V_{REFCA(MIN)}$ to $V_{REFCA(MAX)}$ Example

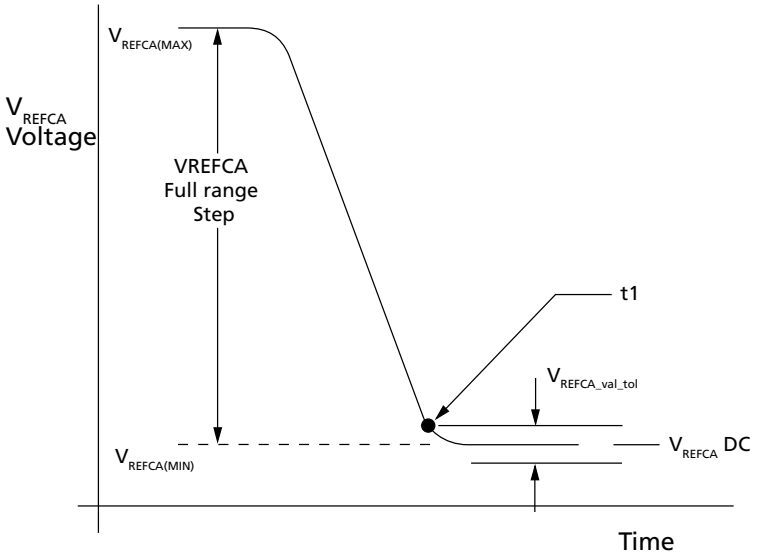


Table 212: Internal V_{REFCA} Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
$V_{REFCA,max}$ operating point	$V_{REFCA,max}$	97.5%	–	–	V_{DDQ}	1
$V_{REFCA,min}$ operating point	$V_{REFCA,min}$	–	–	45%	V_{DDQ}	1
V_{REFCA} step size	$V_{REFCA,step}$	0.41%	0.50%	0.59%	V_{DDQ}	2
V_{REFCA} set tolerance	$V_{REFCA\_set\_tol}$	–1.625%	0.00%	1.625%	V_{DDQ}	3, 4, 6
		–0.15%	0.00%	0.15%	V_{DDQ}	3, 5, 7
V_{REFCA} step time	V_{REFCA_time}	–	–	300	ns	8
V_{REFCA} valid tolerance	$V_{REFCA\_val\_tol}$	–0.15%	0.00%	0.15%	V_{DDQ}	9

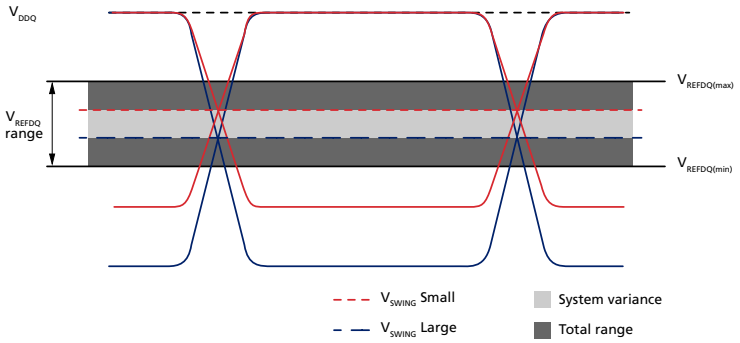
Notes: 1. V_{REFCA} DC voltage reference to TBD.
2. V_{REFCA} step size increment/decrement range. V_{REFCA} at DC level.
3. $V_{REFCA\_new\text{-}setting} = V_{REFCA\_old\text{-}setting} + n * V_{REFCA\_step}$; n = number of steps; if increment use +; if decrement use -.
4. The minimum value of V_{REFCA} setting tolerance = $V_{REFCA\_new\text{-}setting}$ - 1.625% * TBD. The maximum value of V_{REFCA} setting tolerance = $V_{REFCA\_new\text{-}setting}$ + 1.625% * TBD for n>4.
5. The minimum value of V_{REFCA} setting tolerance = $V_{REFCA\_new\text{-}setting}$ -0.15% * TBD. The maximum value of V_{REFCA} setting tolerance = $V_{REFCA\_new\text{-}setting}$ + 0.15% * TBD for n<=4.
6. Measured by recording the minimum and maximum values of the V_{REFCA} output over the range, drawing a straight line between those points and comparing all other V_{REFCA} output settings to that line.
7. Measured by recording the minimum and maximum values of the V_{REFCA} output across four consecutive steps (n = 4), drawing a straight line between those points and comparing all other V_{REFCA} output settings to that line.
8. Time from MPC command with Apply VrefCA and RTT_CA/CS/CK opcode to increment or decrement and voltage settling to within $V_{REFCA\_val\_tol}$ of the target level.
9. Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. V_{REFCA} valid is to qualify the step times which will be characterized at the component level.

V_{REFDQ} Training

The internal V_{REFDQ} specification parameters are operating voltage range, V_{REFDQ} step size, V_{REFDQ} step tolerance, V_{REFDQ} step time, and V_{REF} full step time, and V_{REFDQ} valid voltage level.

The voltage operating range specifies the minimum required V_{REFDQ} setting range. The minimum range is defined by $V_{REFDQ,max}$ and $V_{REFDQ,min}$.

Figure 108: V_{REFDQ} Operating Range – $V_{REFDQ,min}$ $V_{REFDQ,max}$

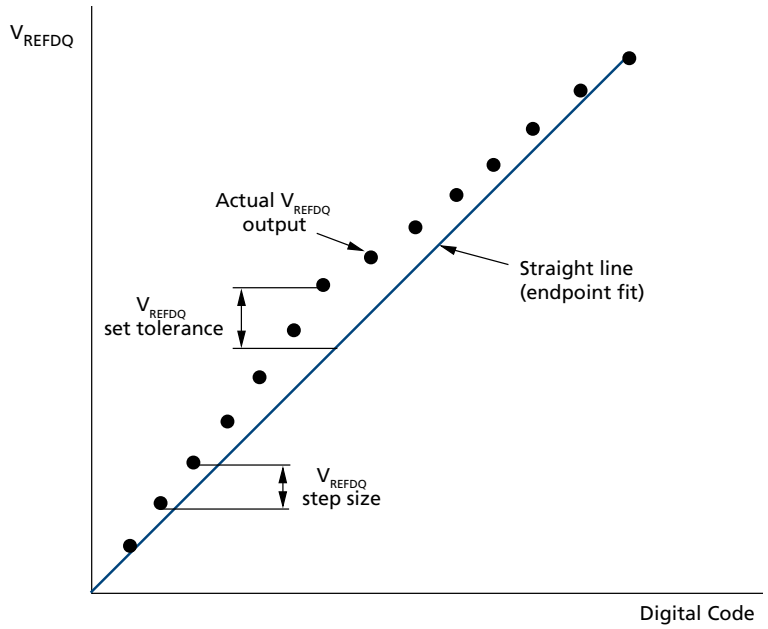


The V_{REFDQ} step size (V_{REFDQ_step}) is defined as the step size between adjacent steps. For a given design, the V_{REFDQ} step size must be within the range specified.

The V_{REFDQ} set tolerance ($V_{REFDQ\_set\_tol}$) is the variation in the V_{REFDQ} voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for V_{REFDQ} set tolerance uncertainty. The range of V_{REFDQ} set tolerance uncertainty is a function of number of steps *n*.

The V_{REFDQ} set tolerance is measured with respect to the ideal line, which is based on the two endpoints, with the endpoints at MIN and MAX V_{REFDQ} values for a specified range.

Figure 109: V_{REFDQ} Set Tolerance and Step Size – MAX Case



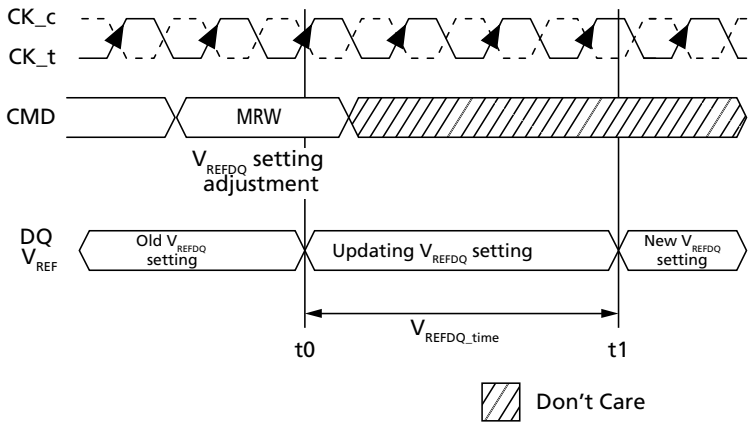
The V_{REFDQ} increment/decrement step times are defined by V_{REFDQ_time}. V_{REFDQ_time}, which is defined from t0 to t1 (shown below), where t0 is at the MRW to MR10 (to adjust V_{REFDQ}) and t1 is where the V_{REFDQ}voltage is at the final DC level (defined by $V_{REFDQ\_new\text{-}setting}$) within the valid tolerance ($V_{REFDQ\_val\_tol}$).

The V_{REFDQ} valid level is defined by $V_{REFDQ\_val\_tol}$ to qualify the step time t1, as shown in the following figures. This parameter is used to ensure an adequate RC time constant behavior of the voltage level change after any V_{REFDQ} increment or decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

t0 - is referenced to the MRW command which updates the V_{REFDQ} values.

t1 - is referenced to the $V_{REFDQ\_va\_tol}$

Figure 110: V_{REFDQ_time}Timing



Notes: 1. The minimum time required between two MRW commands which update V_{REFDQ} settings is V_{REFDQ_time}.
2. An MRW command is used to store the global V_{REFDQ} values into the V_{REFDQ} bits of MR10.
3. Additional per-pin V_{REFDQ} trims are available for programming in MR118, MR126, MR134, ... MR254, OP[7:4], up to a maximum of ±3 V_{REFDQ} steps. The combined global and per-pin V_{REFDQ} settings never exceed the available V_{REFDQ} range from 35.0% to 97.5%.

Figure 111: V_{REFDQ} Step, Single Step Size Increment Example

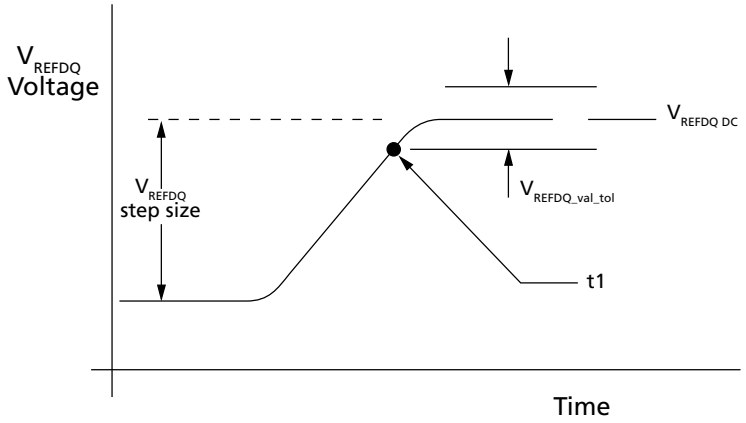


Figure 112: V_{REFDQ} Step, Single Step Size Decrement Example

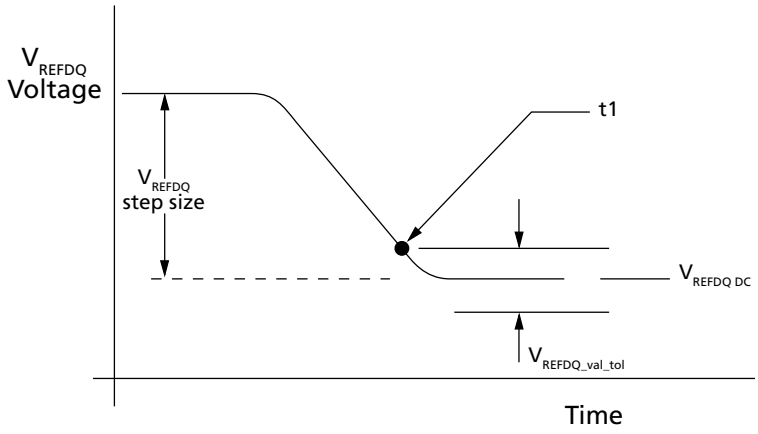


Figure 113: V_{REFDQ} Full Step from $V_{REFDQ(MIN)}$ to $V_{REFDQ(MAX)}$ Example

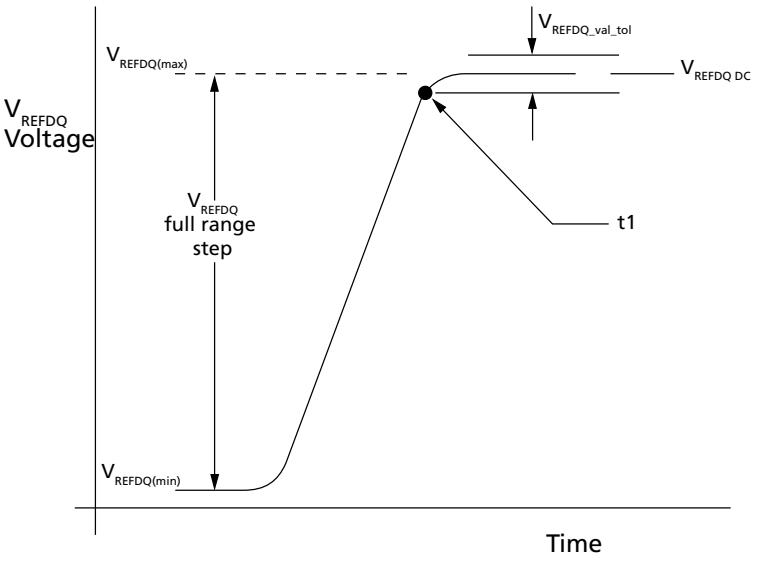


Figure 114: V_{REFDQ} Full Step from $V_{REFDQ(MAX)}$ to $V_{REFDQ(MIN)}$ Example

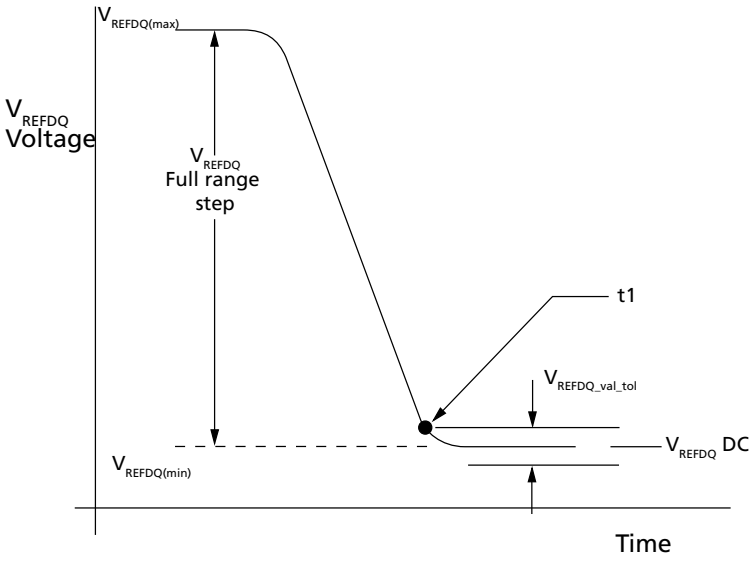


Table 213: Internal V_{REFDQ} Specifications

Parameter	Symbol	MIN	TYP	MAX	Unit	Notes
$V_{REFDQ,max}$ operating point	$V_{REFDQ,max}$	97.5%	–	–	V_{DDQ}	1
$V_{REFDQ,min}$ operating point	$V_{REFDQ,min}$	–	–	45%	V_{DDQ}	1
V_{REFDQ} step size	V_{REFDQ_step}	0.41%	0.50%	0.59%	V_{DDQ}	2
V_{REFDQ} set tolerance	$V_{REFDQ\_set\_tol}$	–1.625%	0.00%	1.625%	V_{DDQ}	3, 4, 6
		–0.15%	0.00%	0.15%	V_{DDQ}	3, 5, 7
V_{REFDQ} step time	V_{REFDQ_time}	–	–	150	ns	8, 10
		–	–	500		
V_{REFDQ} valid tolerance	$V_{REFDQ\_val\_tol}$	–0.15%	0.00%	0.15%	V_{DDQ}	9

Notes:
1. V_{REFDQ} DC voltage referenced to $V_{DDQ(DC)}$.
2. V_{REFDQ} step size increment/decrement range: V_{REFDQ} at DC level.
3. $V_{REFDQ\ (new)} = V_{REFDQ\ (old)} + n * V_{REFDQ\_step}$; n = number of step; if increment, use +; if decrement, use –.
4. The minimum value of V_{REFDQ} setting tolerance = $V_{REFDQ\ (new)}$ - 1.625% * V_{DDQ}. The maximum value of V_{REFDQ} setting tolerance = $V_{REFDQ\ (new)}$ + 1.625% * V_{DDQ} for n > 4.
5. The minimum value of V_{REF} setting tolerance = $V_{REFDQ\ (new)}$ - 0.15% * V_{DDQ}. The maximum value of V_{REFDQ} setting tolerance = $V_{REFDQ\ (new)}$ +0.15% * V_{DDQ} for n < 4.
6. Measured by recording the minimum and maximum values of the V_{REFDQ} output over the range, drawing a straight line between those points and comparing all other V_{REFDQ} output settings to that line.
7. Measured by recording the minimum and maximum values of the V_{REFDQ} output across four consecutive steps (n = 4), drawing a straight line between those points and comparing all other V_{REFDQ} output settings to that line.
8. Time from MRW command updating V_{REFDQ} command to increment or decrement and voltage settling to within $V_{REFDQ\_val\_tol}$ of the target level.
9. Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. V_{REFDQ} valid is to qualify the step times which will be characterized at the component level.
10. The maximum value of V_{REFDQ} step time = 150ns for n<16 and 500ns for n≥16, where n = number of steps.

Write Leveling Training Mode

The DDR5 memory modules use a fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology benefits include reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the memory controller to set the timings of the WRITE DQS signaling according to the write latency timing specification at the device. Therefore, the device supports a write leveling feature that allows the controller to compensate for channel skew. Write leveling training also allows for an unmatched path between CK and DQS within the DRAM, supporting an internal write leveling training flow to account for the difference in internal delays.

The device also provide a programmable timing in its write logic, controlled by the write leveling internal cycle alignment (WICA) mode register (MR3), which provides a means for improved performance of the device receivers. The proper setting of this register shall be determined by the memory controller, either as described in the sections that follow, or by another means derived through engineering analysis. This delay setting is specific to each device, its write preamble setting, and the operating frequency being used. Once the proper delay settings have been determined for a given device byte, write preamble setting and operating frequency, these settings may be restored to the device after reset, power cycle, or return to a previously used operating frequency.

The memory controller can use the write leveling feature and feedback from the device to adjust the controller's differential DQS (DQS_t, DQS_c) output delay to align to the phase and cycle that corresponds to the CAS write latency (CWL) delay after the WRITE command. The memory controller involved in the leveling must have an adjustable delay setting on the DQS to align the rising edge of differential DQS with the timing at the receiver that is the pin-level write latency (external write leveling training), and to align DQS with the internal DRAM write latency timing point (write leveling internal cycle alignment training). The internal DRAM write latency timing point may be skewed from the pin-level write latency timing point. The host will minimize this skew (^{t}DQSoffset) through the write leveling training flow.

Because the system and DIMM delays vary, the device supports the ability for the host to align the DQS timings with a pin-level write latency differential CK (CK_t-CK_c) edge. This alignment is referred to as external write leveling. Once the DQS host timings are aligned at the DRAM write latency timing, the internal DRAM timings are optimized for lowest power and internal delay. This is accomplished when the host enables the internal write timing setting in MR2. To compensate for the difference in delay, the host will execute an internal write leveling training sequence, which includes sweeping the write leveling internal cycle (WICA) settings in MR3 (write leveling internal cycle alignment operation) and then finalizing the differential DQS phase and offset (write leveling internal phase alignment and final host DQS timing operation).

During write leveling training (both external and internal), the DQS pattern includes the full programmed write preamble and only the first toggle of the normal data burst sequence. The device samples the internal write leveling pulse relative to the first DQS toggle of the data burst sequence (last rising differential DQS edge sent by the host) and asynchronously feeds back the result of this sample on the DQ bus, transitioning between ^{t}WLO MIN and ^{t}WLO MAX. If the DQ bus output is LOW at ^{t}WLO MAX, the internal write leveling pulse signal is sampled while it is deasserted (LOW). Likewise, if the DQ burst output is HIGH at ^{t}WLO MAX, the internal write leveling pulse signal is sampled while it is asserted (HIGH).

The sampled feedback state remains on the DQ bus until a subsequent write leveling sample changes the state, or until write leveling training is exited.

The internal write leveling pulse is generated in response to a WRITE command, and held statically LOW otherwise. To perform the write leveling training, the controller repeatedly sends a WRITE

command, delays DQS, and monitors the DQ feedback after ^{t}WLO MAX until a transition from 0 to 1 is detected, indicating alignment with the internal write leveling pulse.

During internal write leveling training flows, the host will apply an offset to the starting point or the final setting of the DQS signals. The offsets are referred to as WL_ADJ_start and WL_ADJ_end. This will minimize the ^{t}DQSoffset variation across different DRAM devices. The WL_ADJ_start and WL_ADJ_end values depend on the ^{t}WPRE setting.

When external and internal write leveling training flows are complete and the final WL_ADJ_end offset has been applied to the DQS timings, DQS is phase-aligned and cycle-aligned for write operations. During the training sequence, the DRAM in write leveling training mode will apply ODT to the strobes in the same way as for functional operation.

All non-target ranks (which will not be in write leveling training mode) will apply ODT as defined for functional operation. Prior to executing the write leveling training flow, ^{t}WPRE value must be configured to the functional operation setting.

Note: DQS ODT is based on a DQS PARK mode and is not enabled and disabled with DQ ODT timings.

Write Leveling Mode Registers

The MR fields for write leveling training, internal write timing, and write leveling internal cycle alignment are part of MR2 and MR3.

To enter write leveling training mode, the controller programs MR2:OP[1] = 1. To exit the write leveling training mode, program MR2:OP[1] = 0. Write leveling internal cycle alignment offers two nibbles to control the upper and lower DQ bytes. The lower byte write leveling internal cycle alignment is intended for x4, x8, and x16 configurations, while the upper byte is only for x16 configurations.

The internal write timing, once enabled (MR2:OP[7]=1), remains enabled through the internal write leveling training flow and for functional operation. The host is responsible for incrementing the write leveling internal cycle alignment setting until the internal write leveling pulse is pulled early enough to align with the differential DQS signal which was previously aligned with the pin-level write latency timing. The write leveling internal cycle alignment setting only applies when the internal write timing is enabled.

Only BL16 mode is supported in write leveling training mode.

External Write Leveling Training Operation

When write leveling mode is enabled (MR2:OP[1]=1) and the internal write timing is disabled (MR2:OP[7]=0), the device will have an internal write leveling pulse that indicates how the DQS signals align to match the pin-level write latency timings. The rising edge of the internal write leveling pulse will align to the rising edge of the differntial CK signal that coincides with CAS write latency (CWL), as shown in the following diagrams.

The differntial DQS signals driven by the controller during leveling mode must be terminated by the DRAM devices based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

All data bits carry the leveling feedback to the controller across the DRAM configurations x4, x8, and x16. On a x16 device, both byte lanes are leveled independently. Therefore, a separate feedback mechanism shall be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS (diff_UDQS) to internal write leveling pulse relationship, whereas the lower data bits would indicate the lower diff_DQS (diff_LDQS) to internal write leveling pulse relationship. When training a x16 device, the data bits of a byte remain in the don't care statue until its applicable DQS

signals are toggled. Once the DQS signals are toggled, the DQs follow the behavior previously described.

The following diagram shows the timing sequence to enter write leveling training mode, how the operation works during write leveling training mode (with internal write timing disabled), and the timing sequence to exit write leveling training mode. An MRW command is sent to enable write leveling training mode. Prior to sending the MRW command to enable write leveling training mode, the host memory controller must drive the DQS signals differentially LOW. After ^{t}WLPEN time, the controller can send a WRITE command, followed by strobe pulses. The DQS signals always drive differentially LOW, except during the preamble and burst strobe sequence. There is no restriction as to how early the strobe pulses are sent, so long as they are no earlier than CWL/2 after the WRITE command. The device samples the internal write leveling pulse relative to the first DQS toggle of the data burst sequence and asynchronously feeds back the result of this sample on the DQ bus, transitioning between ^{t}WLOmin and ^{t}WLOmax.

While in write leveling training mode, the host controller may send ACT and PRE commands. The DRAM will ignore these commands, and the addresses associated with these ACT and the WRITE commands may be any value. The following timing diagrams demonstrate the timing requirements associated with write leveling training mode entry, the internal write leveling pulse alignment during external write leveling training, and the DQ sample feedback timing.

Figure 115: Write Leveling Training Mode (External Training, 2N Mode, 0 Sample)

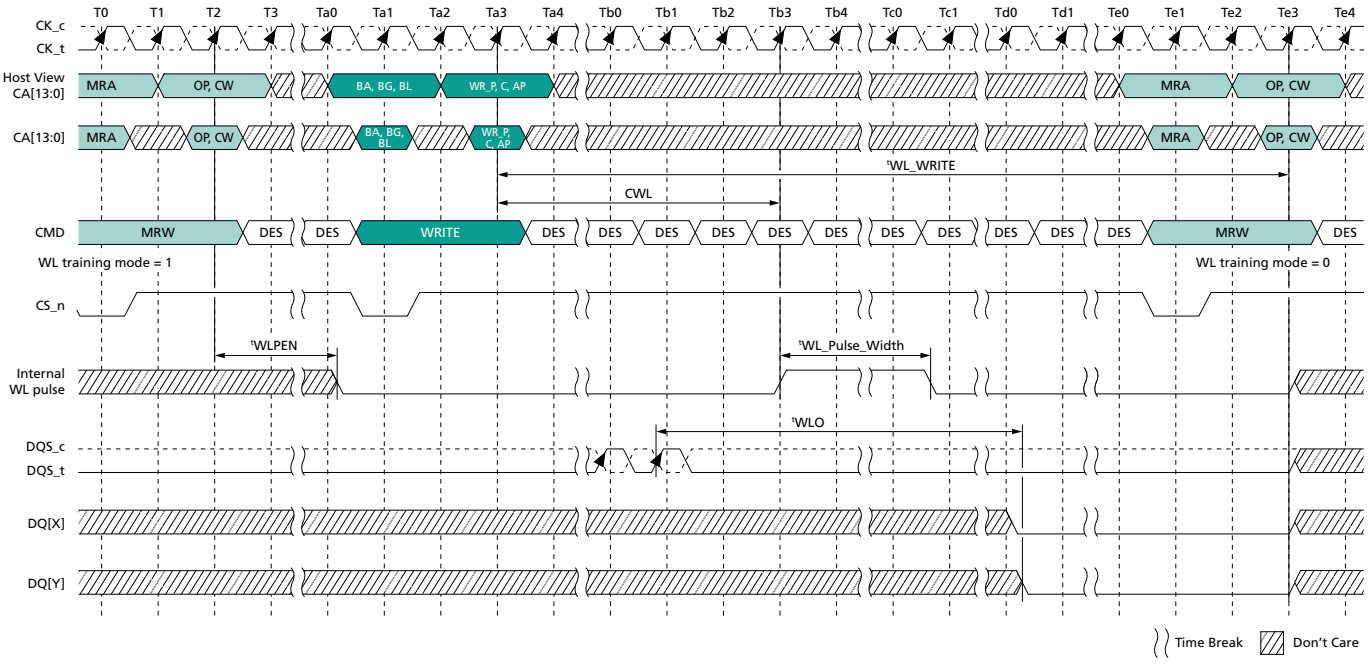


Figure 116: Write Leveling Training Mode (External Training, 1N Mode, 0 Sample)

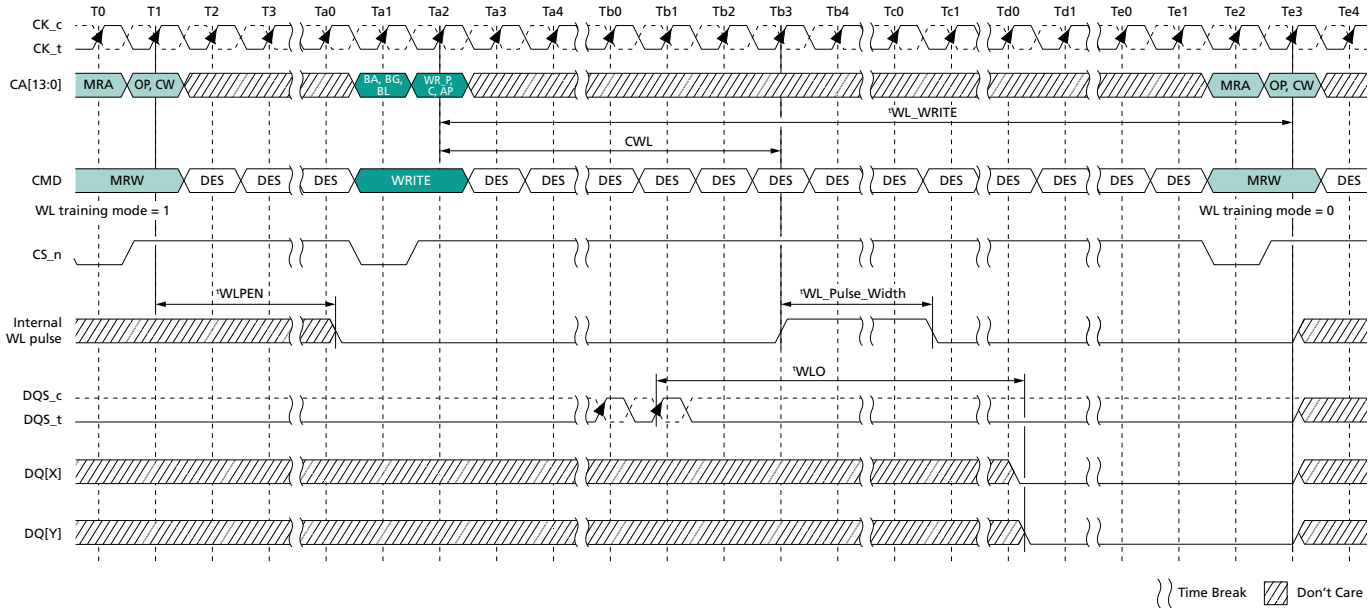


Figure 117: Write Leveling Training Mode (External Training, 2N Mode, 1 Sample)

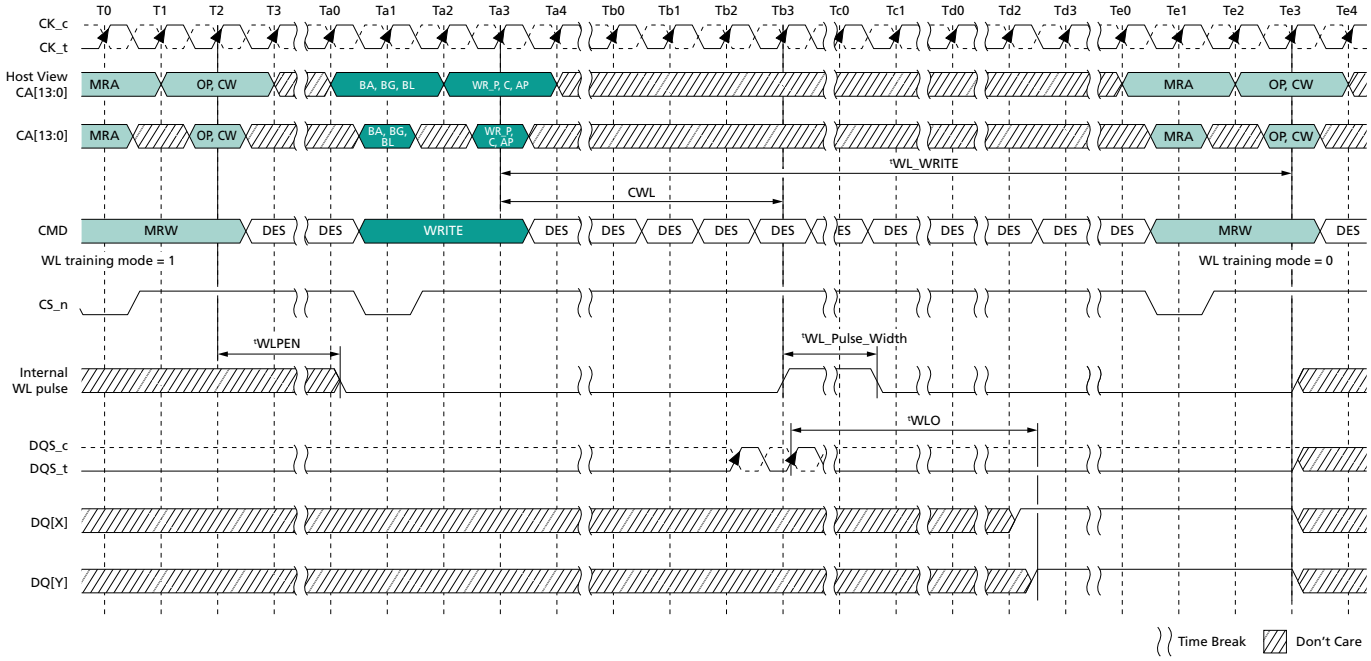
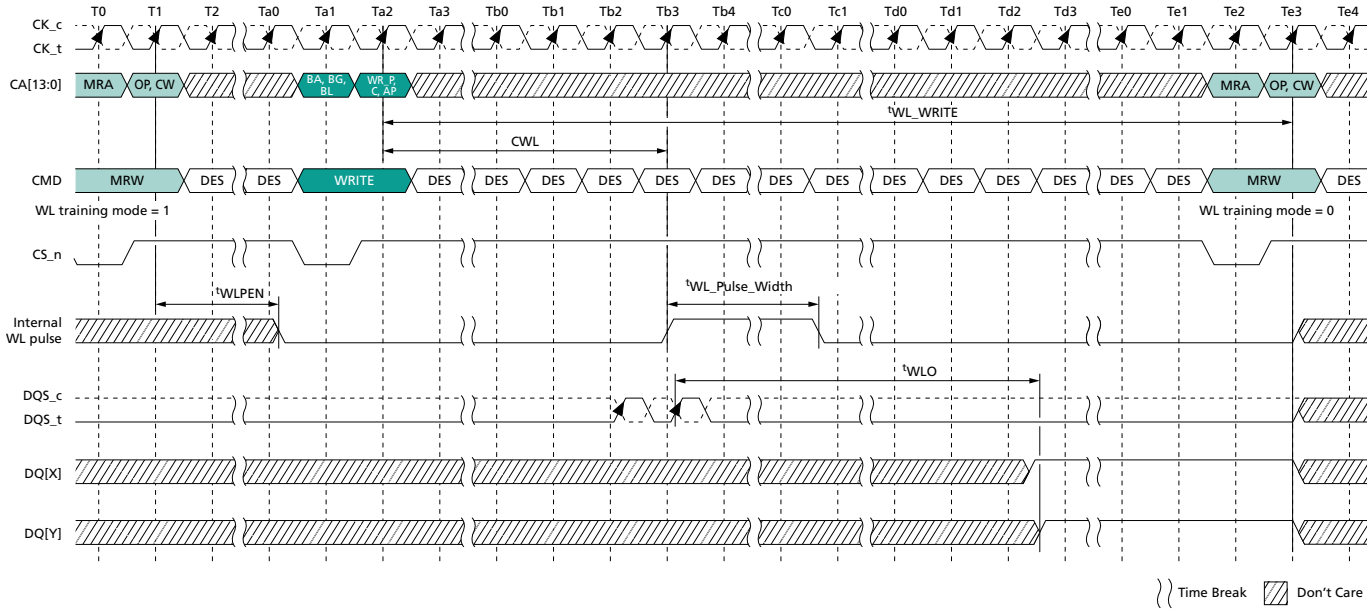


Figure 118: Write Leveling Training Mode (External Training, 1N Mode, 1 Sample)



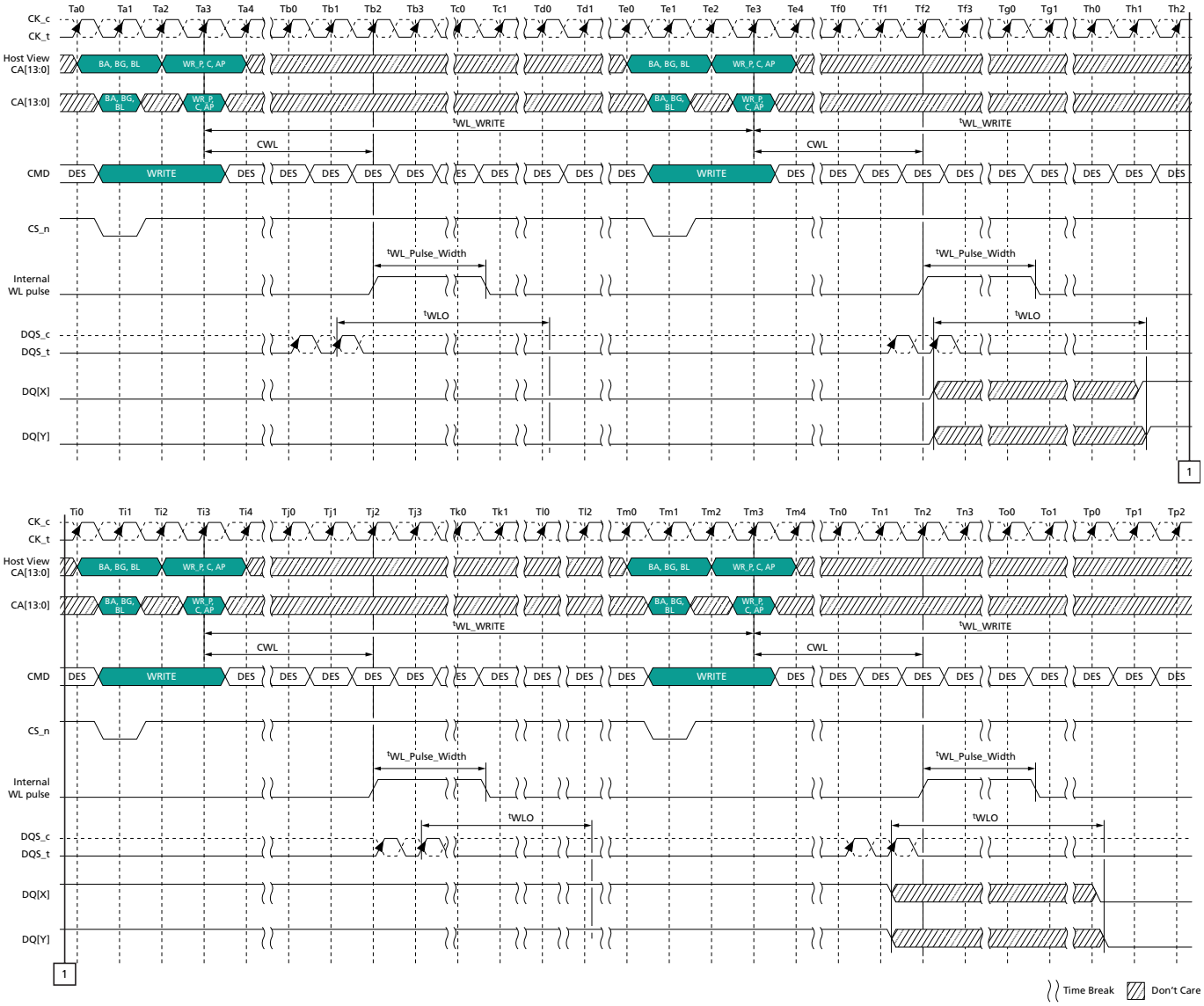
The memory controller initiates write leveling training mode of all DRAMs by setting MR2:OP[1] = 1. When entering write leveling training mode, the DQ pins are in undefined driving mode. Since the controller levels one rank at a time, all non-target ranks will set write leveling training mode to disabled. The controller may assert non-target ODT through the normal WRITE command protocol. The DQS_RTT_PARK termination applies to the DQS_t and DQS_c signals.

The controller drives DQS differentially LOW prior to sending the MRW command to enable write leveling training mode. The WRITE command must occur after a delay of ^{t}WLPEN relative to the MRW-enabled write leveling training mode.

The device samples the internal write leveling pulse and asynchronously feeds back the result of this sample on the DQ bus, transitioning between ^{t}WLOmin and ^{t}WLOmax. The controller can sample the state of any DQ bit after ^{t}WLOmax. Based on the sampled state, the controller decides to increment or decrement the DQS delay setting, and launches the next WRITE command with an associated DQS pulse (or pulse sequence) after some time, which is controller-dependent. Once a 0 to 1 transition on the DQ bus is detected, the controller locks the DQS delay setting and external write leveling is achieved for the device.

Write leveling training may be executed by issuing consecutive WRITE commands after write leveling mode has been enabled (no requirement to exit and re-enter between each WRITE command). The minimum WRITE-to-WRITE command spacing during write leveling mode is ^{t}WL_Write and is defined as max(CWL, last DQS differential toggle) + ^{t}WLO (max) + 2nCK. An example of consecutive WRITE commands given during write leveling training is shown below.

Figure 119: Consecutive WRITE Commands During Write Leveling Training Mode (External Training, 2N Mode, 4 Samples)



Write Leveling Internal Cycle Alignment Operation

After the external write leveling training step completes, and after the host DQS signals have been aligned to the pin-level write latency timing, the host applies a negative offset (WL_ADJ_start) to the DQS timing. The WL_ADJ_start offset moves the DQS timing prior to the internal write leveling pulse (causing LOW observed on the DQ pins), and it is dependent on the ^{t}WPRE setting (shown in the table below). This will be a reference point for aligning the internal write leveling pulse via the WICA settings in MR3.

The internal cycle alignment training begins when an MRW command is issued to enable internal write timing in MR2 (keeping OP[1]=1 and setting MR2:OP[7]=1). The host sweeps the write leveling internal cycle alignment (WICA) delay settings in MR3, starting with the 0^{t}CK offset default. Increasing the WICA mode register offset setting speeds up the timing of the WRITE command by reducing the WRITE

command to internal write pulse delay until the DQS is aligned with the internal write leveling pulse assertion. Alignment results in a logic HIGH on the DQ pins.

The table below summarizes the WL_ADJ_start and WL_ADJ_end values per ^{t}WPRE setting.

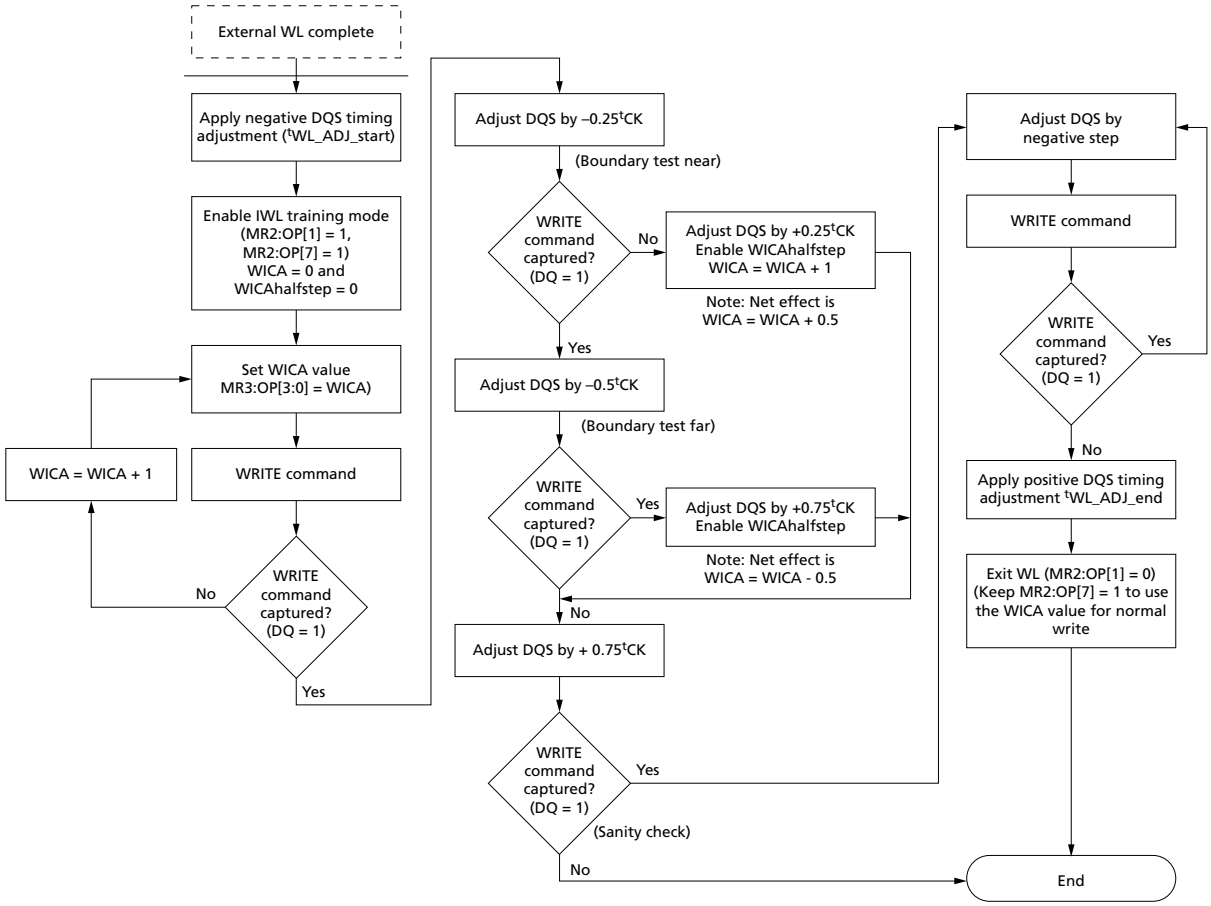
Table 214: WL Internal Cycle Alignment

WL_ADJ Term	Description	^{t}WPRE = 2^{t}CK	^{t}WPRE = 3^{t}CK	^{t}WPRE = 4^{t}CK[1]
WL_ADJ_start	Offset that the host applies to the DQS_t/DQS_c timing just after external write leveling alignment to write latency and prior theinternal cycle alignment training	–0.75 ^{t}CK	–1.25 ^{t}CK	–2.25 ^{t}CK
WL_ADJ_end	Offset that the host applies to the DQS_t/DQS_c timing after final phase alignment to the rising edge of the write leveling internal pulse. This will center the write leveling internal pulse rising edge within the preamble window	1.25 ^{t}CK	1.75 ^{t}CK	2.75 ^{t}CK

Notes: 1. For ^{t}WPRE = 4 ^{t}CK, CL is required to be greater than or equal to 30 during write leveling training mode operation. This is irrespective of the CL setting for ^{t}WPRE = 4 ^{t}CK during normal operation.

Due to potential measurement errors that can occur during the internal write leveling training, the device may include an optional 0.5 ^{t}CK adjustment for optimizing the internal cycle alignment. MR7:OP[0]=1 adds a +0.5 ^{t}CK adjustment for the lower byte of the DQs, while MR7:OP[1]=1 adds a +0.5 ^{t}CK adjustment for the upper byte of the DQs. The figure below is an example of an internal write leveling training flow with the addition of the +0.5 ^{t}CK WICA adjustment (additional flow shown in blue).

Figure 120: Write Leveling Training Flow with Half Step WICA



The two following timing diagrams demonstrate the write leveling training operation when internal write timings are enabled and the internal cycle alignment is set such that the internal write leveling pulse has not yet reached the host DQS toggles.

Figure 121: Write Leveling Training Mode (Internal Cycle Alignment, 2N Mode, 0 Sample)

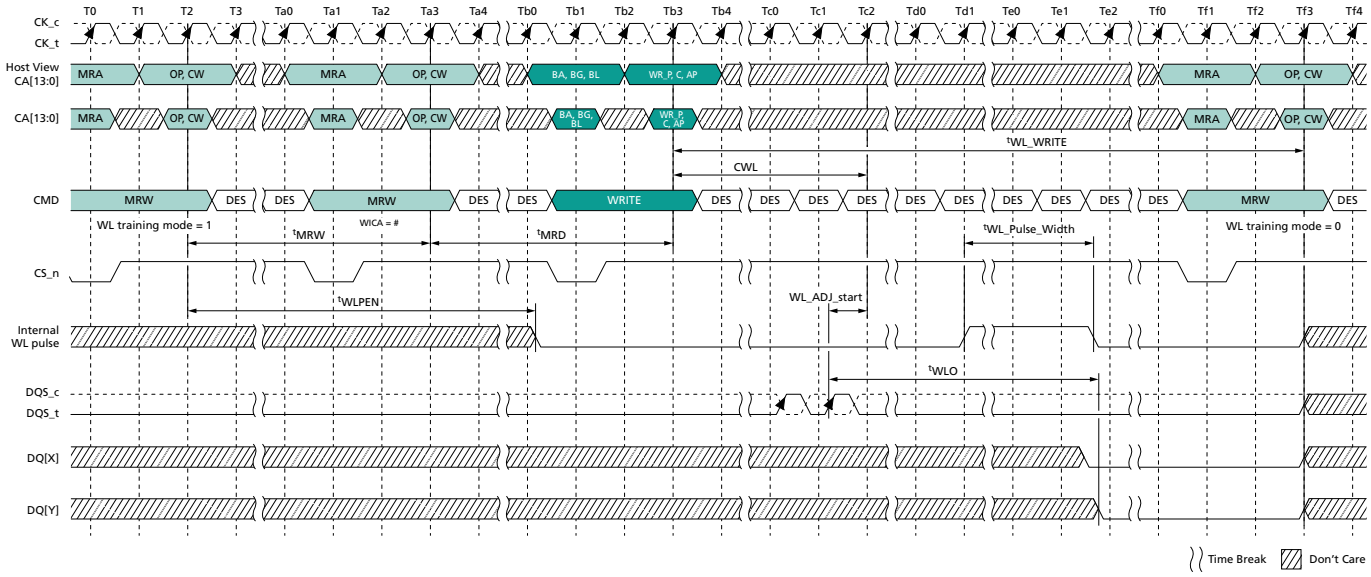
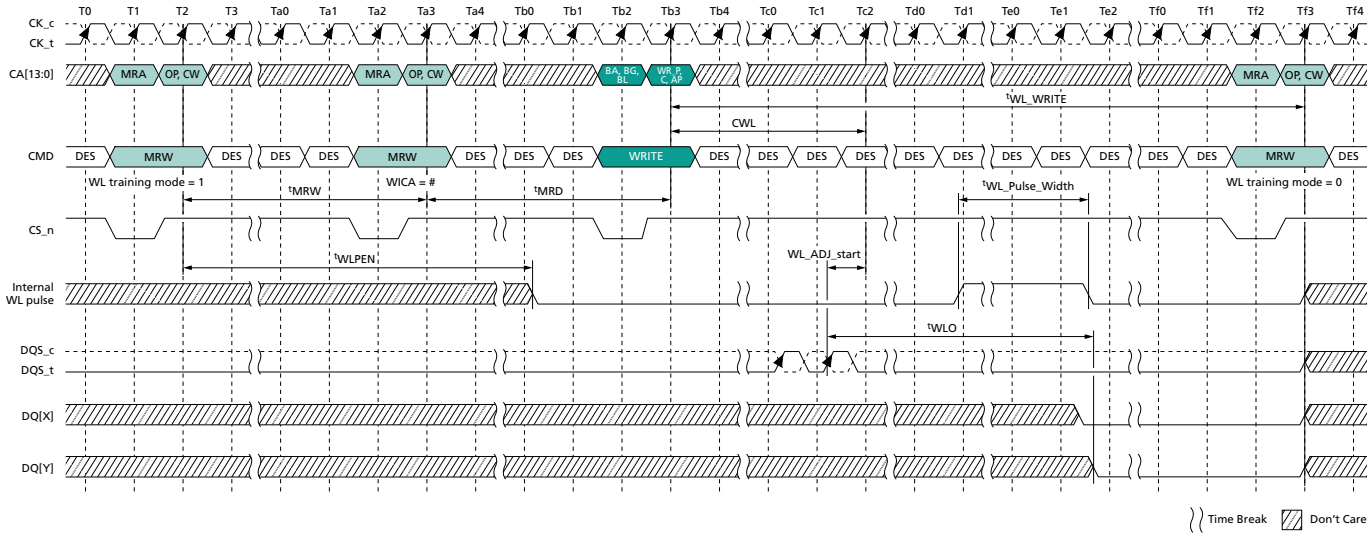


Figure 122: Write Leveling Training Mode (Internal Cycle Alignment, 1N Mode, 0 Sample)



The following two timing diagrams demonstrate the write leveling training operation when internal write timings are enabled and the internal cycle alignment is set such that the internal write leveling pulse has completed the course alignment to the host DQS timing.

Figure 123: Write Leveling Training Mode (Internal Cycle Alignment, 2N Mode, 1 Sample)

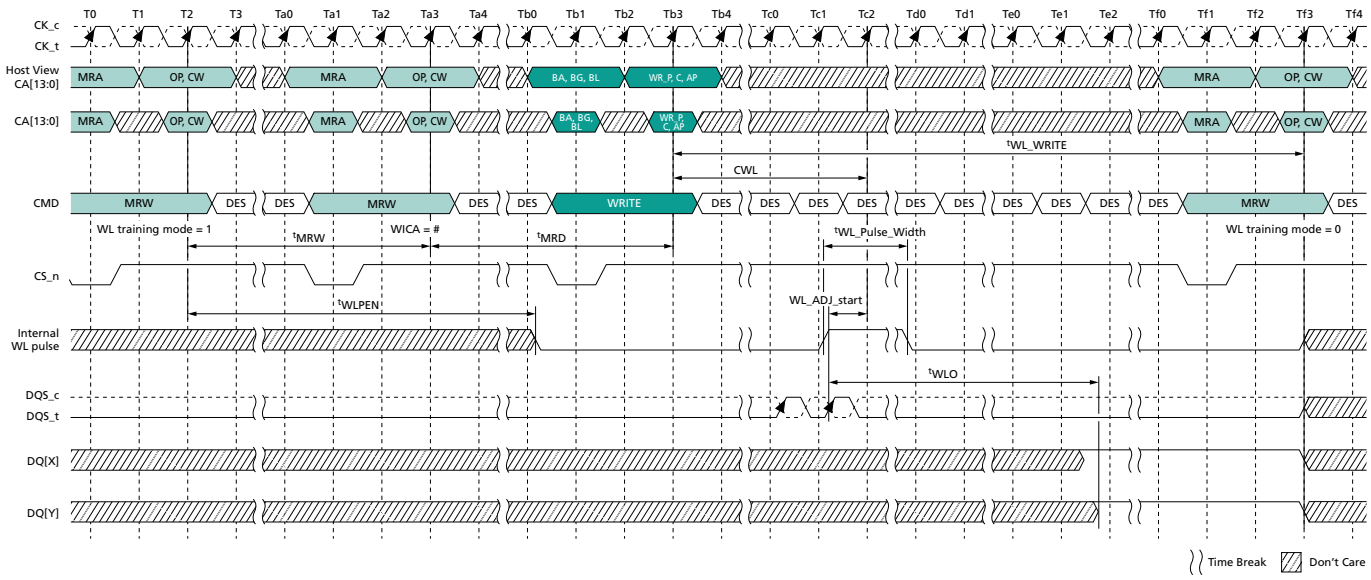
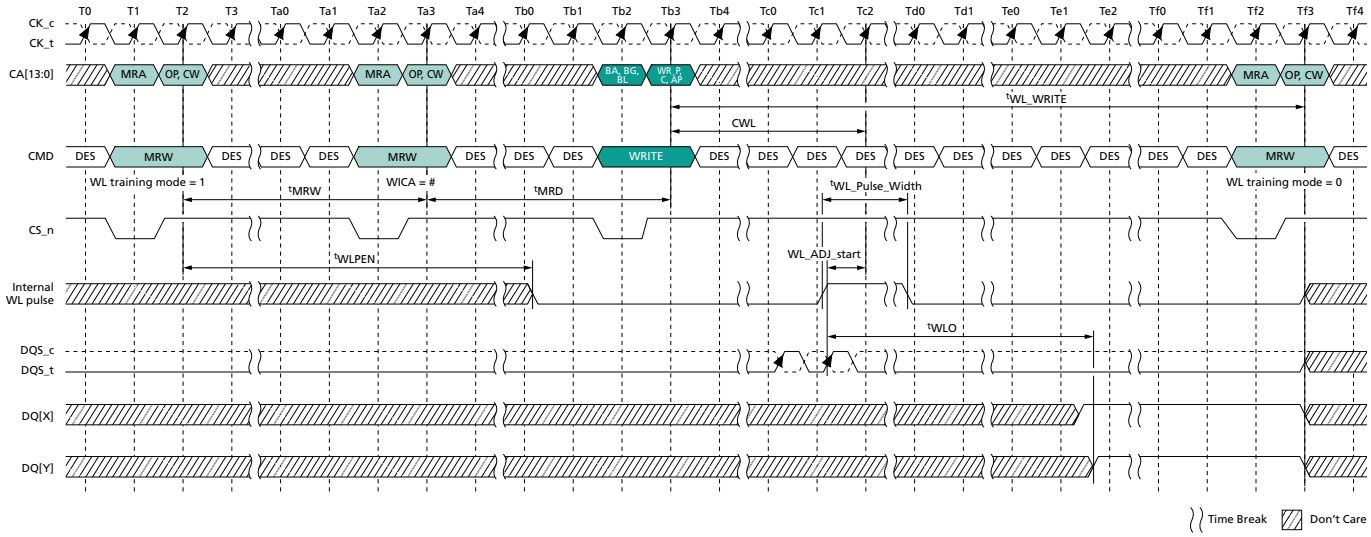
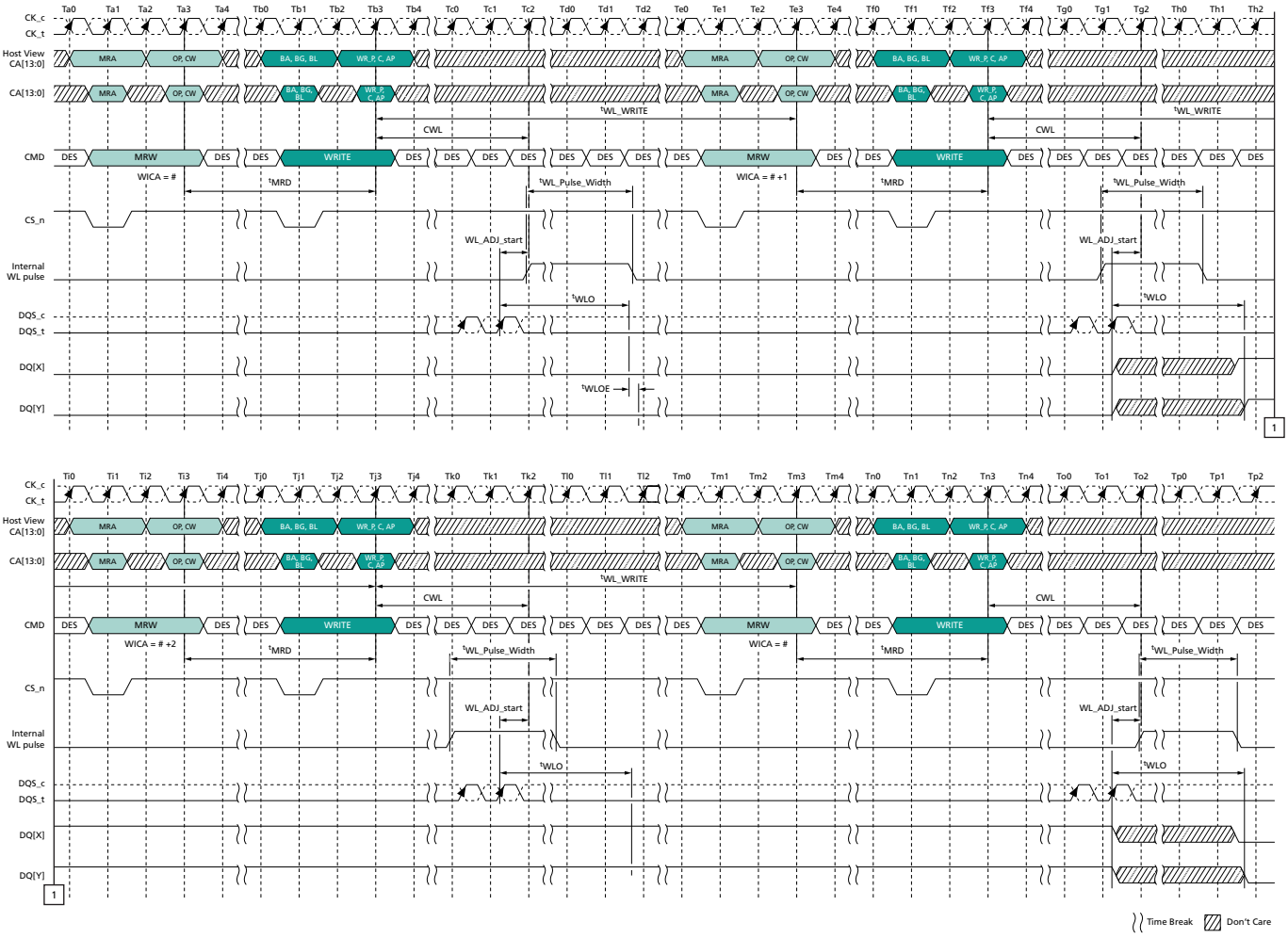


Figure 124: Write Leveling Training Mode (Internal Cycle Alignment, 1N Mode, 1 Sample)



An example of write leveling training internal cycle alignment executed by issuing consecutive WRITE commands after write leveling mode has been enabled (no requirement to exit and re-enter between each WRITE command) is shown below.

Figure 125: Consecutive WRITE Commands During Write Leveling Training Mode (Internal Training, 2N Mode, 4 Samples)



As previously noted, x16 devices allow for independent lower and upper byte write leveling training and setting. Although unique values are preferred to optimize (minimize) ^{t}DQSoffset, setting both the lower and upper bytes to use the same WICA offset is allowed since the internal paths for both bytes are expected to be closely matched; meaning, internal write leveling training that results in a different byte setting per byte indicates the internal paths are on a boundary between the two settings. When choosing a common WICA offset value, the starting values of the lower and upper WICA offset should differ by no more than one. The higher (smallest absolute value since the WICA values apply a negative offset) of the two values will be programmed in both bytes of the device to minimize the impact on the final training sweep.

Table 215: Common WICA Offset for x16 Upper and Lower Byte

Lower Byte WICA	Upper Byte WICA	Common WICA
-4	-3	-3
-2	-3	-2

When choosing a common 0.5 ^{t}CK WICA offset value, the WICA value programmed in both bytes of the device will be the same before applying the 0.5 ^{t}CK offset. (If the byte values are different, the higher

value is programmed in both bytes of the device, as noted above, and the 0.5 tCK offset step is skipped). If the 0.5 tCK training indicates that one byte requires the +0.5 tCK offset but the other byte does not, this also indicates the two bytes are on a boundary between the two settings. In this case, the +0.5 tCK will be applied to both bytes, resulting in the higher (smallest absolute) value being used.

Table 216: Common Half WICA for x16 Upper and Lower Byte

Lower Byte WICA	Lower Byte +0.5tCK WICA	Upper Byte WICA	Lower Byte +0.5tCK WICA	Common WICA
-4	n/a	-3	n/a	-3
-4	Yes	-4	No	-4 +0.5 (-3.5 total)
-3	No	-3	Yes	-3 +0.5 (-2.5 total)

When using a common WICA offset value approach to the internal write leveling training, both bytes perform the final training sweep after applying the common WICA offset value (both the full cycle and 0.5 tCK WICA, if applicable).

Write Leveling Internal Phase Alignment and Final Host DQS Timing Operation

Once the internal cycle alignment is achieved, the host shall perform a final fine sweep of the DQS timings with internal write timing enabled (MR2:OP[7]=1) to establish an even closer phase alignment to the rising edge of the internal write leveling pulse. Once this is complete, the host will then add a positive offset of WL_ADJ_end (dependent upon tWPRE) to the DQS_t-DQS_c timings. This results in a tDQSoffset between -0.5 tCK and +0.5 tCK with measurement adjustments of tWLS/tWLH, placing the rising edge of the internal write leveling pulse within the preamble. If the optional half step WICA process is used during write leveling training, this results in a tDQS offset between -0.25 tCK and +0.25 tCK with measurement adjustments of tWLS/tWLH. After the WL_ADJ_end offset has been applied, the host will disable write leveling training mode (MR2:OP[1]=0). The internal write timing will remain enabled and the internal cycle alignment setting will retain the coarse setting that was trained. After every reset, the host must either restore these settings or execute the full write leveling training flow.

The following figure shows the timing relationships for the final placement of the host DQS timings relative to the internal write leveling pulse. However, it is not necessary to execute this write leveling training mode measurement to finalize the setting. (Note that this figure is for illustration purposes only.)

Figure 126: Final Timings After Write Leveling Training is Complete (2N Mode)

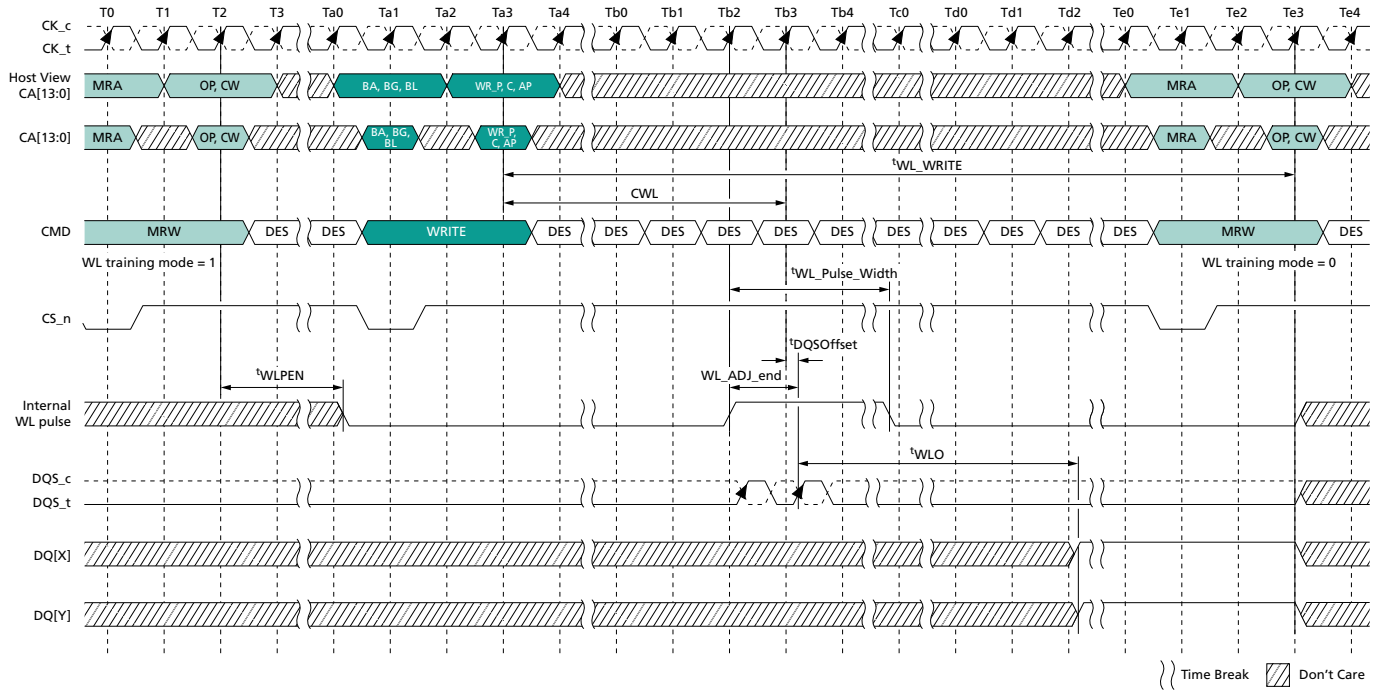
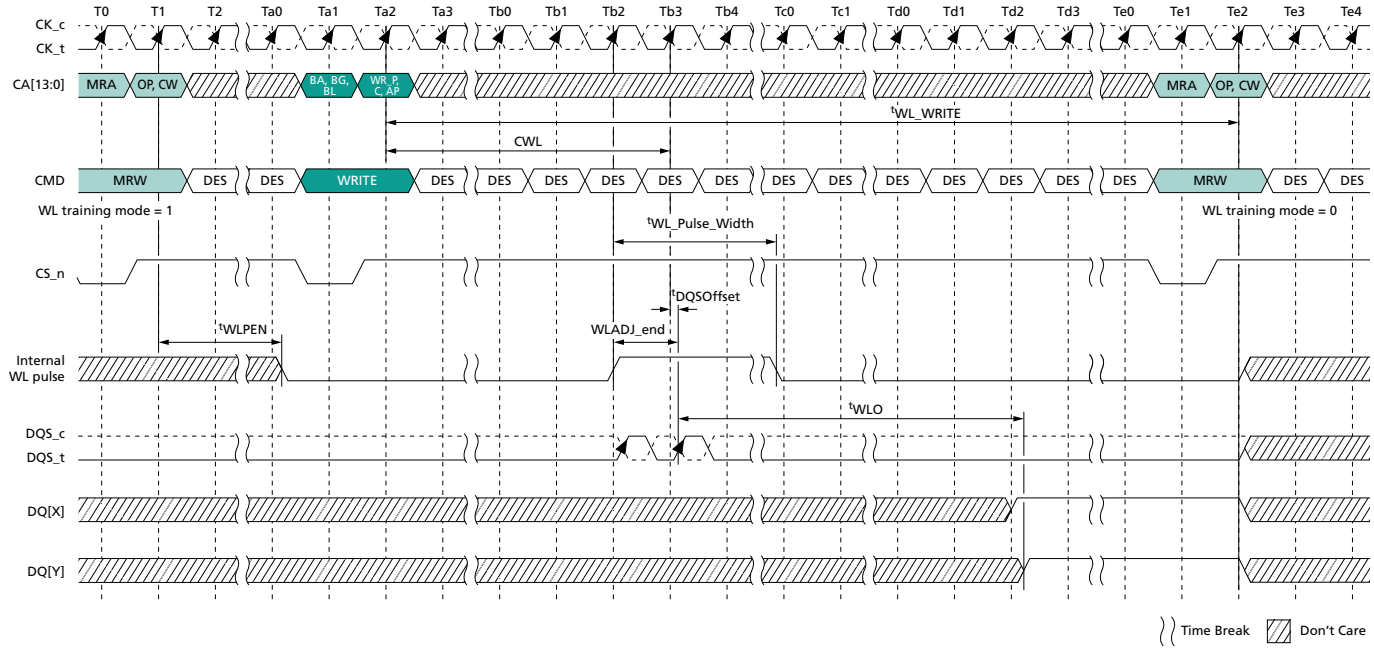


Figure 127: Final Timings After Write Leveling Training is Complete (1N Mode)



DRAM Termination During Write Leveling

When the DRAM is in write leveling mode, the DQS_c/DQS_t termination (DQS_RTT_PARK) and the command and control termination (RTT_CA, RTT_CK, RTT_CS) are the same as for functional opera-

tion. The DQ signals are not terminated in the DRAM, but instead are driving values to the controller. The host controller applies termination for the DQ signals.

Table 217: DRAM Termination During Write Leveling

ODT Enabled	DQS_t, DQS_c Termination	DQ Termination
RTT_WR	DQS_RTT_PARK	Off
RTT_Park, RTT_WR disabled	DQS_RTT_PARK	Off

Notes: 1. Termination for TDQS/DM is not included since TDQS and DM are disabled during write leveling training mode.

Read Training Pattern

Training of the memory interface requires the ability to read a known pattern from the device, prior to enabling writes to the device. Due to the increased clock frequencies in DDR5, a simple repeating pattern is not sufficient for read training. A linear feedback shift register (LFSR) for a pattern generator is also required.

The read training pattern is accessed when the host issues an MRR command to the MR31 address (OP only need be valid) and CRC must be disabled prior to issuing this command. In this case, the returned data is a pattern instead of the contents of a mode register. The timing of the read data return is the same as for an MRR or READ command, including the operation of the strobes (DQSL_t, DQSL_c, DQSU_t, DQSU_c). The device also supports non-target ODT.

An alternate continuous burst mode is available and is configured with MRW to MR25:OP[3]=1. Once this mode is configured, any subsequent MRR (not only to MR31, but any MR) to that device starts the pattern output and automatically continues to output the appropriate pattern until it is stopped by either a system reset or by issuing a MRW MR25:OP[3] = 0b command that reverts it to the MRR command-based (default) mode, as shown in the Timing Diagram for Continuous Burst Mode Read Training Patterns figure shown later in this section.

Once MR25:OP[3] = 0b, MRR command-based (default) mode is registered by the device, it stops all pattern traffic by ^{t}Cont_Exit. Since there is no minimum time for ^{t}Cont_Exit, the device may stop the pattern prior to ^{t}Cont_Exit, potentially truncating any current burst pattern. To ensure the device's state machine doesn't enter metastability while turning off the output pattern, the host must issue a second MR25:OP[3]=0 MRW command (default) after waiting ^{t}MRW, which then starts ^{t}Cont_Exit_delay. After ^{t}Cont_Exit_delay expires, any other valid command is then legal. All read training patterns (modes) are supported in continuous burst mode. The host must disable read CRC, if enabled, prior to using continuous burst mode.

Prior to utilizing either read training pattern mode (Continuous Burst Output mode or MRR Command Based mode), the initial seed value will need to be programmed in MR26-MR30, else the default values will be used. The default value for the Read Pattern Data0/LFSR0 (MR26) register setting is 0x5A, and the default value for the Read Pattern Data1/LFSR1 (MR27) register setting is 0x3C. The Read Pattern Invert (MR28, MR29) register settings default to 0. The Read LFSR Assignments (MR30) register setting default is 0xFE.

The device does not store the current LFSR state when exiting the continuous burst output mode and may clear the pattern values stored in MR26-MR30; therefore, any subsequent pattern reads will require the host to reprogram the seed, pattern, inversion, and LFSR assignments in MR26-MR30.

The read training pattern has two primary modes of operation: serial format and LFSR. LFSR mode is required due to the device's higher frequency bus operation. There is a secondary mode associated with the LFSR mode, which enables the generation of a simple high frequency clock pattern instead of

the LFSR pattern. The read training pattern is a full BL16 pattern for each MRR command issued to the read training pattern address.

Only BL16 Mode is supported by the read training pattern, and it should not be disturbed by an ACT command until after the completion of training.

Table 218: Read Training Pattern Address

MR Address	Operating Mode	Description
MR31	Read Training Pattern	Reserved. No specific register fields are associated with this address. In response to the MRR to this address, the device sends the BL16 read training pattern. All 8 bits associated with this MR address are reserved.

The following table shows the MR field and encodings for the read training pattern format settings. The default value for the read training pattern format register setting is 0x0.

Table 219: Read Training Pattern Format

MR Address	Operating Mode	Description
MR25:OP[0]	Read Training Pattern Format	0 = Serial, 1 = LFSR
MR25:OP[1]	LFSR0 Pattern Option	0 = LFSR, 1 = Clock
MR25:OP[2]	LFSR1 Pattern Option	0 = LFSR, 1 = Clock
MR25:OP[3]	Continuous Burst Mode	0 = MRR command-based (default), 1 = continuous burst output

For serial read training pattern format mode, the following mode registers are programmed with the data pattern. Two 8-bit registers provide a 16 UI pattern length and two 8-bit registers provide up to x16 data width for per-DQ-lane inversion.

LFSR mode requires an 8-bit mode register to program the seed for the 8-bit LFSR. The Read Pattern Data0/LFSR0 and Read Pattern Data1/LFSR1 registers are re-purposed to program the LFSR seed when the Read Training Pattern Format is set to LFSR.

Default Read Pattern Data0/LFSR0 register setting: 0x5A

Table 220: Read Pattern Data0 / LFSR0

MR Address	MRW OP	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR26	UI	7	6	5	4	3	2	1	0

Default Read Pattern Data1/LFSR1 register setting: 0x3C

Table 221: Read Pattern Data1 / LFSR1

MR Address	MRW OP	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR27	UI	15	14	13	12	11	10	9	8

The values for the Read Pattern Data0/LFSR0 and Read Pattern Data1/LFSR1 registers may be restored to the default values under the following conditions:

- Self refresh
- Power-down entry
- Exiting continuous burst output mode

If any of the above conditions occur, and non-default values are desired, the host will need to reprogram the contents of MR26 and MR27 prior to utilizing either read training pattern mode (continuos burst output mode or MRR command based mode)

In both cases, when the Read Training Pattern Format is set to serial mode or LFSR mode, the Read Pattern Invert - Lower DQ bits and Read Pattern Invert - Upper DQ bit settings additionally invert the pattern, per DQ bit. The Read Pattern Invert - Lower DQ bits register applies to x4, x8, and x16 devices. The Read Pattern Invert - Upper DQ bits register applies to x16 devices only, for the upper byte.

Default Read Pattern Invert - Lower DQ bits register setting: 0x00

Table 222: Read Pattern Invert - Lower DQ Bits

MR Address	MRW OP	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR28	DQ Invert	DQL7	DQL6	DQL5	DQL4	DQL3	DQL2	DQL1	DQL0

Default Read Pattern Invert - Upper DQ bits register setting: 0x00

Table 223: Read Pattern Invert - Upper DQ Bits

MR Address	MRW OP	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR29	DQ Invert	DQU7	DQU6	DQU5	DQU4	DQU3	DQU2	DQU1	DQU0

The values for the Read Pattern Invert0 and Read Pattern Invert1 registers may be restored to the default values under the following conditions:

- Power-down entry
- Self refresh entry
- Exiting continuous burst mode

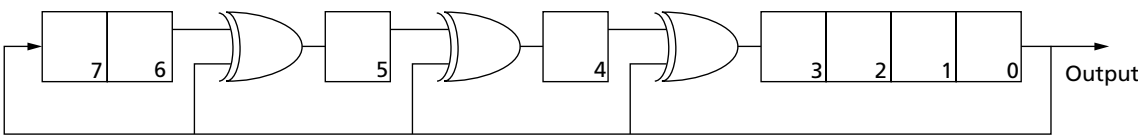
If any of the above conditions occur, the host must reprogram the contents of MR28 and MR29 prior to utilizing either read training pattern mode (continuous burst output mode or MRR command based mode).

A value of 0 in any bit location of the Read Pattern Invert - Lower DQ bits or Read Pattern Invert - Upper DQ bits registers leave the pattern un-inverted for the associated DQ. A value of 1 in any bit location of the Read Pattern Invert - Lower DQ bits or Read Pattern Invert - Upper DQ bits registers invert the pattern for the associated DQ.

LFSR Pattern Generation

The LFSR is an 8-bit Galois LFSR. The polynomial for the LFSR is x8+x6+x5+x4+1. The figure below shows the logic to implement the LFSR. The numbered locations within the shift register show the mapping of the seed/state positions within the register. There are two instances of the same LFSR polynomial. These two instances have unique seeds/states and supply patterns to any of the DQ outputs.

Figure 128: Read Training Pattern LFSR



The seed location in the figure clarifies the mapping for the Read Pattern Data0/LFRS0 and Read Pattern Data1/LFSR1 mode registers relative to the LFSR logic. The LFSR output is directed to any number of the DQ outputs, depending on the LFSR assignment programming. These assignments between LFSR0 and LFSR1 to each DQ output create a unique pattern sequence for better coverage of

DQ to DQ crosstalk interactions. The LFSR assignments are programmed according to the following table.

Default Read LFSR Assignments register setting: 0xFE

Table 224: Read LFSR Assignments

MR Address	MRW OP	LFSR Assignment	MR Setting	
MR30	OP0	DQL0/DQU0	0 = Read Training Pattern Data0 / LFSRO	1 = Read Training Pattern Data1 / LFSR1
	OP1	DQL1/DQU1	0 = Read Training Pattern Data0 / LFSRO	1 = Read Training Pattern Data1 / LFSR1
	OP2	DQL2/DQU2	0 = Read Training Pattern Data0 / LFSRO	1 = Read Training Pattern Data1 / LFSR1
	OP3	DQL3/DQU3	0 = Read Training Pattern Data0 / LFSRO	1 = Read Training Pattern Data1 / LFSR1
	OP4	DQL4/DQU4	0 = Read Training Pattern Data0 / LFSRO	1 = Read Training Pattern Data1 / LFSR1
	OP5	DQL5/DQU5	0 = Read Training Pattern Data0 / LFSRO	1 = Read Training Pattern Data1 / LFSR1
	OP6	DQL6/DQU6	0 = Read Training Pattern Data0 / LFSRO	1 = Read Training Pattern Data1 / LFSR1
	OP7	DQL7/DQU7	0 = Read Training Pattern Data0 / LFSRO	1 = Read Training Pattern Data1 / LFSR1

The values for the Read LFSR Assigments register may be restored to the default values under the following conditions:

- Power-down entry
- Self refresh entry
- Exiting continuous burst output mode

If any of the above conditions occur, the host must reprogram the contents of MR30 prior to utilizing either read training pattern mode (continuous burst output mode or MRR command based mode).

The LFSR output changes at the UI frequency, producing a new output value on every UI. The LFSR only changes state to support the read data after the MRR to the Read Training Pattern address (MR31). When there are no MRR accesses to the Read Training Pattern address (MR31), the LFSR retains its previous state (from the end of the previous Read Training Pattern MRR access completion); therefore, the full state space of the LFSR may be traversed through a series of 16 MRR commands, each of which accesses 16 UIs of LFSR output. The BL for the LFSR data is always BL16. The state of the LFSR can also be changed by sending a new MRW command to reset the LFSR0 and LFSR1 seed mode registers (MR26 and MR27) or through the reset conditions listed for those registers. A setting of 0x00 in either of the LFSR seed registers (MR26 and MR27) does not produce a pattern with any transitions to 1. When set to this value, the LFSR produces a constant 0 pattern.

When the LFSR0 Pattern Option (MR25:OP[1]) is set to 1, the pattern supplied by the device is a high-frequency clock pattern instead of the LFSR. This clock pattern is sent only to the DQ signals that have a setting of 0 in the corresponding DQ opcode location in the Read LFSR Assignments register. The first UI of the pattern has a value of 0. The second UI has a value of 1, and this continues to toggle for each subsequent UI.

When the LFSR1 Pattern Option (MR25:OP[2]) is set to 1, the pattern supplied by the device is a high-frequency clock pattern instead of the LFSR. This clock pattern is sent only to the DQ signals that

have a setting of 1 in the corresponding DQ opcode location in the Read LFSR Assignments register. The first UI of the pattern has a value of 0. The second UI has a value of 1, and this continues to toggle for each subsequent UI.

The state of the LFSR does not change when an MRR to MR31 occurs if the associated LFSR Pattern Option is set to 1 in MR25[1] for LFSR0, or MR25[2] for LFSR1, designating the clock pattern. The state of both LFSR0 and LFSR1 also does not change when an MRR to MR31 occurs if the serial mode is selected by setting MR25[0] = 0b. The Read LFSR Assignments settings have no impact on whether or not the LFSR state progresses with each MRR to MR31. Only the Read Training Pattern Format and LFSR Pattern Option settings determine whether the LFSR is actively computing next states.

Read Training Pattern Examples

The following table shows the bit sequence of the read training pattern, for the following programming:

- Read Training Pattern Format = 0 (Serial)
- LFSR0 Pattern Option = 0 (These are don't-cares when in Serial Training Pattern Format)
- LFSR1 Pattern Option = 0 (These are don't-cares when in Serial Training Pattern Format)
- Read Pattern Data0/LFSR0 = 0x1C
- Read Pattern Data1/LFSR1 = 0x59
- Read Pattern Invert0 = 0x55
- Read Pattern Invert1 = 0x55

Table 225: Serial Bit Sequence Example

Pin	Invert	Bit Sequence															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQL0	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQL1	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQL2	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQL3	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQL4	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQL5	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQL6	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQL7	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQU0	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQU1	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQU2	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQU3	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQU4	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQU5	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQU6	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQU7	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0

The following table shows the bit sequence of the read training pattern, for the following programming:

- Read Training Pattern Format = 1 (LFSR)

- LFSR0 Pattern Option = 0
- LFSR1 Pattern Option = 0
- Read Pattern Data0/LFSR0 = 0x5A
- Read Pattern Data1/LFSR1 = 0x3C
- Read LFSR Assignments = 0xFE
- Read Pattern Invert0 = 0x00
- Read Pattern Invert1 = 0xFF

Table 226: LFSR Bit Sequence Example 1

Pin	Invert	LFSR	Bit Sequence															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQL0	0 (No)	0	0	0	1	1	0	0	0	0	0	0	1	1	1	0	1	0
DQL1	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL2	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL3	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL4	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL5	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL6	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL7	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQU0	1 (Yes)	0	1	1	0	0	1	1	1	1	1	1	0	0	0	1	0	1
DQU1	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU2	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU3	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU4	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU5	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU6	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU7	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1

The following table shows the bit sequence of the read training pattern, for the following programming:

- Read Training Pattern Format = 1 (LFSR)
- LFSR0 Pattern Option = 0
- LFSR1 Pattern Option = 1 (clock pattern option)
- Read Pattern Data0/LFSR0 = 0x00 (when the LFSR seed is set to 0, a constant 0 pattern is produced)
- Read Pattern Data1/LFSR1 = 0x3C (this value is don't care when LFSR1 pattern option = 1)
- Read LFSR Assignment = 0x04
- Read Pattern Invert - Lower DQ bits = 0xFB

- Read Pattern Invert - Upper DQ bits = 0xFB

Table 227: LFSR Bit Sequence Example 2

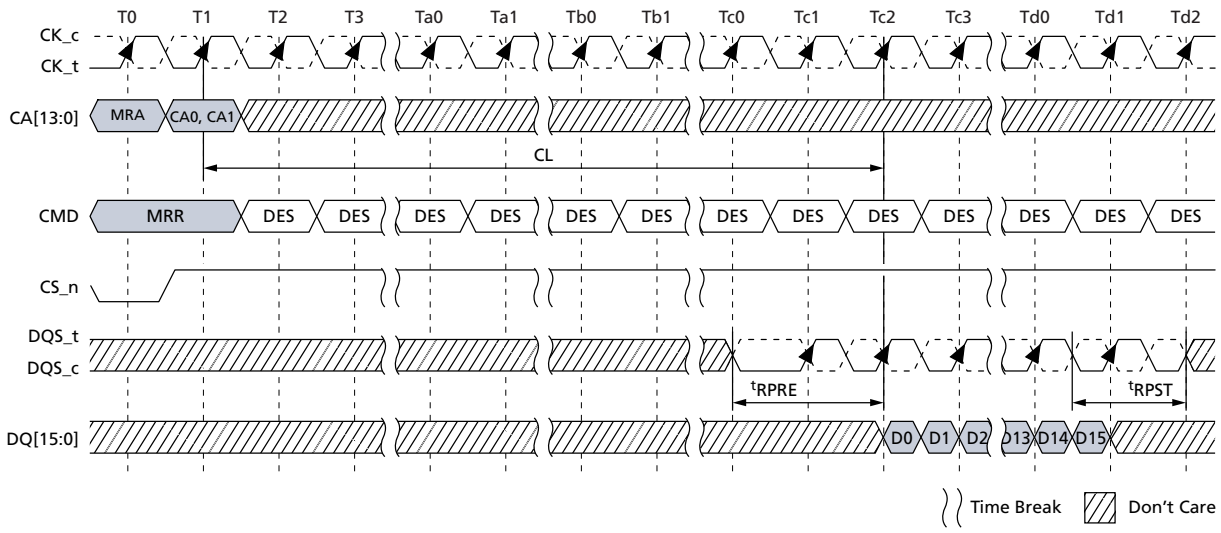
Pin	Invert	LFSR	Bit Sequence															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQL0	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL1	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL2	0 (No)	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
DQL3	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL4	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL5	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL6	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL7	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU0	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU1	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU2	0 (No)	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
DQU3	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU4	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU5	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU6	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU7	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Read Training Pattern Timing Diagrams

The data return and strobe sequence timings should match the READ operation timing. The timing of the read training pattern is similar to the MRR operation, with the exception that the MRR to the address that invokes the read training pattern is a full BL16 pattern. The timing between MRR commands to access the read training pattern is defined as ^{t}MRR_p, which supports back-to-back data patterns. This is faster than a normal MRR-to-MRR condition, which is defined as ^{t}MRR.

The following timing diagram shows the general timing sequence for an MRR that accesses the read training pattern.

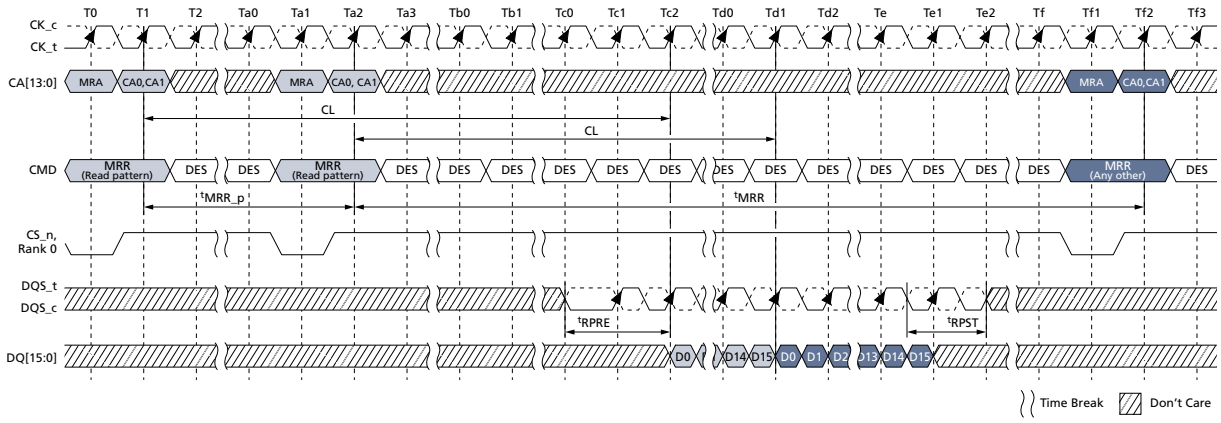
Figure 129: Read Training Patterns



Note: 1. The read training pattern must align to the preamble timings.

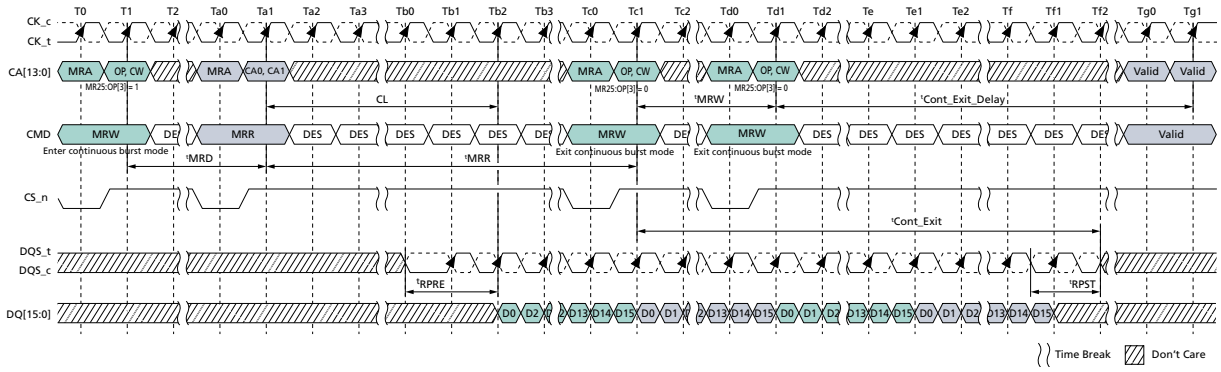
The read training pattern must also support back-to-back traffic for any number of MRR commands sequenced every 8CK. The following timing diagram shows a back-to-back pattern example.

Figure 130: Back-to-Back Read Training Patterns



Note: 1. The read training pattern must align to the preamble timings.

Figure 131: Continuous Burst Mode Read Training Patterns



Note: 1. The read training pattern shall align to the preamble timings and exits after MRW (continuous exit encoding) is received, but before ^{t}Cont_exit expires. During ^{t}Cont_exit, the data output may not follow the read pattern data.

Read Preamble Training Mode

Read preamble training mode supports read leveling of the host receiver timings. This mode supports MRR transactions that access the read training pattern and cannot be used during any other data transactions. Similar to read training pattern mode, read preamble training mode needs to be entered with CRC disabled.

Read preamble training mode changes the read strobe behavior such that the strobes are always driven by the device, and only toggle during a 1^{t}CK preamble plus the actual burst of the read data. There is no toggle during the postamble time. This mode enables the host to detect the timing of when the first data and associated strobe is returned after a READ command.

Entry and Exit for Preamble Training Mode

The device enters read preamble training mode by setting MR2:OP[0] = 1. Read preamble training mode is exited by setting MR2:OP[0] = 0. Read preamble training model must not be disturbed by an ACT command until the completion of training.

Table 228: Read Preamble Training Mode

MR Address	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR2	Valid	Valid	Valid	Valid	Valid	Valid	Valid	Read preamble training mode

Table 229: Preamble Training Mode Configuration

MR Address	Operating Mode	Description
MR2:OP[0]	Read preamble training mode enable	0 = Normal Mode (default) 1 = Read Preamble Training Mode

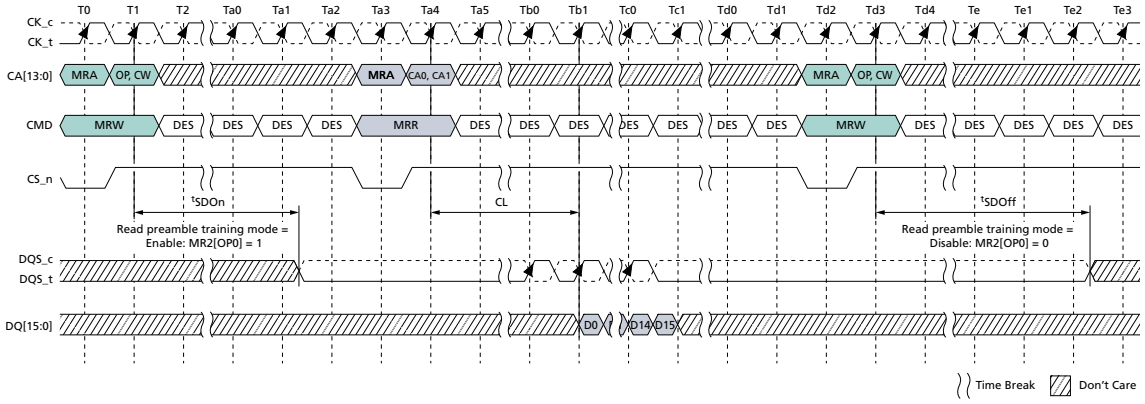
Preamble Training Mode Operation

Once the device is placed in read preamble training mode, the only data transactions supported are MRR commands. All non-data commands, such as MRW, are still supported in this mode. Once read preamble training mode is enabled, the device will drive DQS_t LOW and DQS_c HIGH within ^{t}SDOn and remain at these levels until an MRR command is issued.

During read preamble training mode, a 1 tCK preamble will be used instead of the programmed DQS preamble setting. Once the MRR command is issued, the device will drive DQS_t/DQS_c after CL-tRPRE (where tRPRE = 1CK), like a normal READ burst with the Read DQS Offset setting in MR40 applied. In response to the MRR to the designated read training pattern address, the device must also drive the DQ pattern as per the read pattern configuration while in this mode. The MRR commands may be sequenced to enable back to back bursts on the DQ bus.

Read preamble training mode is exited within tSDOff after setting MR2:OP[0]. The following figure shows the timing for the strobe driven differential LOW after read preamble training mode is enabled, and also shows the strobe timings, including a 1 tCK preamble, after an MRR command to access the read training pattern.

Figure 132: Preamble Training Mode Entry, Read Training Pattern Access, and Read Preamble Training Mode Exit



DQS Interval Oscillator

As voltage and temperature changes on the die, the DQS clock tree delay shifts and may require re-training. An internal DQS clock-tree oscillator, which measures the amount of delay over a given time interval (determined by the controller), enables the controller to compare the trained delay value to the delay value seen at a later time. The DQS interval oscillator provides the controller with important information regarding the need to re-train and the magnitude of potential error.

The DQS interval oscillator starts by issuing an MPC command with start DQS interval OSC (DQSOSCST) opcode, OP[7:0] = 0000 0111b set as described in the MPC Operation section. This starts an internal ring oscillator that counts the number of times a signal propagates through a copy of the DQS clock tree.

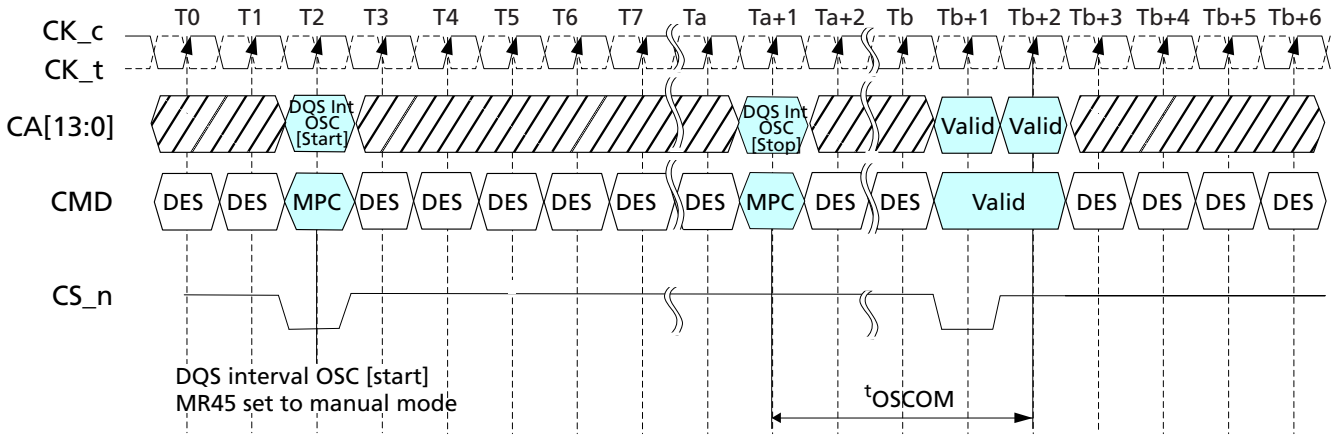
The DQS interval oscillator may be stopped by issuing an MPC command with stop DQS interval OSC (DQSOSCSP) opcode, OP[7:0] = 0000 0110b, as described in the MPC Operation section, or the controller may instruct the device to count for a specific number of clocks and then stop automatically (see mode registers 45, 46 and 47 for more information). If MR45 is set to automatically stop the DQS oscillator, the MPC command with stop DQS interval OSC opcode will not be used. When the DQS oscillator is stopped by either method, the result of the oscillator counter is automatically stored in MR46 and MR47 after the oscillator is stopped and within tOSCOA for automatic mode and tOSCOM for manual mode.

MRW commands to MR45 during an ongoing DQS interval oscillator operation are not permitted. MR45 may be reprogrammed tMRD after the oscillator is stopped by the automatic stop.

The device responds in one of two ways if an MPC command with start DQS interval OSC opcode is issued during an ongoing DQS interval oscillator operation (automatic or manual): The device ignores the concurrent start operation, in which case the DQS interval oscillator operation proceeds as normal with all timing constraints referencing the original start operation; or, the device restarts the DQS interval oscillator operation, in which case all timing constraints reference the most recent (subsequent) start operation. The host must account for the worst-case option in the event that a concurrent start operation is issued. If issuing a concurrent MPC command [start DQS interval OSC] results in a loss of run time tracking, the results stored in MR46 and MR47 are ignored and the full operation restarts.

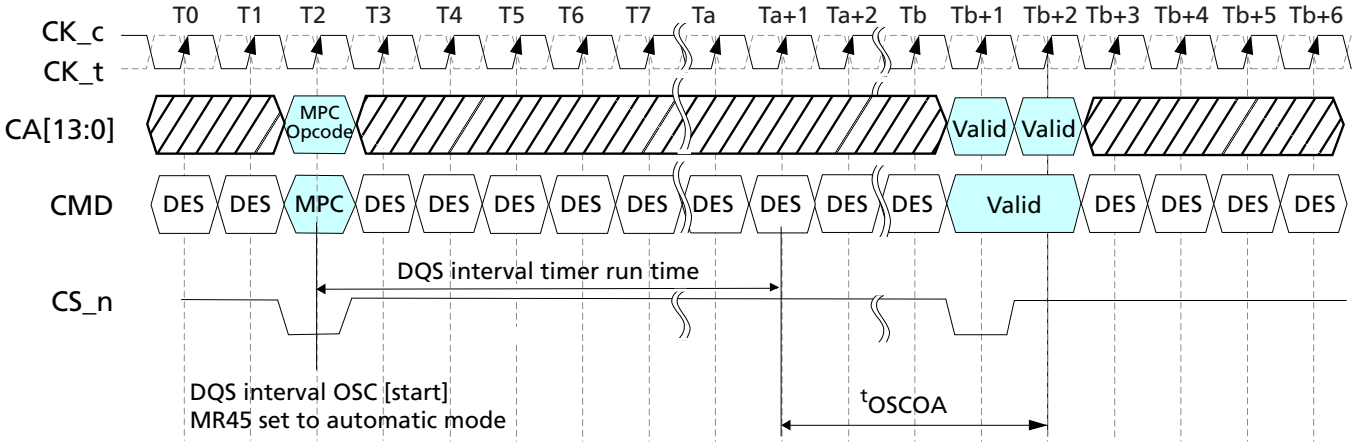
Entering self refresh during an ongoing DQS interval oscillator operation is permitted. Upon exiting self refresh, an operation started in automatic mode is allowed to complete naturally based upon the specified number of clocks (cumulative before and after self refresh). If a manual operation started prior to entering self refresh is not stopped prior as well, the operation is manually stopped upon self refresh exit. The results stored in MR46 and MR47 for a DQS interval oscillator operation that spans self refresh entry/exit is ignored and the full operation restarted.

Figure 133: DQS Interval Oscillator Manual Mode



Note: 1. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 134: DQS Interval Oscillator Automatic Mode



Note: 1. DES commands are shown for ease of illustration; other commands may be valid at these times.

The controller may adjust the accuracy of the result by running the DQS interval oscillator for shorter (less accurate) or longer (more accurate) duration. The accuracy of the result for a given temperature and voltage is determined by the following equation:

$$\text{DQS oscillator granularity error} = \frac{2 \times (\text{DQS delay})}{\text{Run time}}$$

Where:

- Run time = total time between start and stop commands
- DQS delay = value of the DQS clock tree delay ^{t}RX_DQS2DQ (MIN/MAX)

An additional device matching error must be included, which is the difference between DQS training circuit and the actual DQS clock tree across voltage and temperature. The matching error is vendor specific. Therefore, the total accuracy of the DQS oscillator counter is given by:

$$\text{DQS oscillator accuracy} = 1 - \text{granularity error} - \text{matching error}$$

Example: If the total time between start and stop commands is 100ns, and the maximum DQS clock tree delay is 400ps (^{t}RX_DQS2DQ,MAX), the DQS oscillator granularity error is:

$$\text{DQS oscillator granularity error} = \frac{2 \times (0.4\text{ns})}{100\text{ns}} = 0.8\%$$

This equates to a granularity timing error of 3.2ps.

Assuming a circuit matching error of 5.5ps across voltage and temperature, the accuracy is:

$$\text{DQS oscillator accuracy} = 1 - \frac{3.2 + 5.5}{400} = 97.8\%$$

Example: Running the DQS oscillator for a longer period improves the accuracy. If the total time between start and stop commands is 250ns, and the maximum DQS clock tree delay is 400ps (^{t}RX_DQS2DQ,MAX), the DQS oscillator granularity error is:

$$\text{DQS oscillator granularity error} = \frac{2 \times (0.4\text{ns})}{250\text{ns}} = 0.32\%$$

This equates to a granularity timing error of 1.28ps.

Assuming a circuit matching error of 5.5ps across voltage and temperature, the accuracy is:

$$\text{DQS oscillator accuracy} = 1 - \frac{1.28 + 5.5}{400} = 98.3\%$$

The result of the DQS interval oscillator is defined as the number of DQS clock tree delays that can be counted within the run time, determined by the controller. The result of the MPC command [start DQS interval OSC] operation is stored in MR46 and MR47. MR46 contains the least-significant bits (LSB) of the result; MR47 contains the most-significant bits (MSB) of the result. MR46 and MR47 are overwritten by the device when an MPC command [stop DQS interval OSC] is received. The device counter counts to its maximum value (=2^{16}) and stops. If the maximum value is read from the mode registers, the memory controller must assume that the counter overflowed the register and discarded the result. The longest run time for the oscillator that will not overflow the counter registers can be calculated as follows:

$$\text{Longest run time interval} = 2^{16} \times {}^{t}\text{RX\_DQS2DQ (MIN)}$$

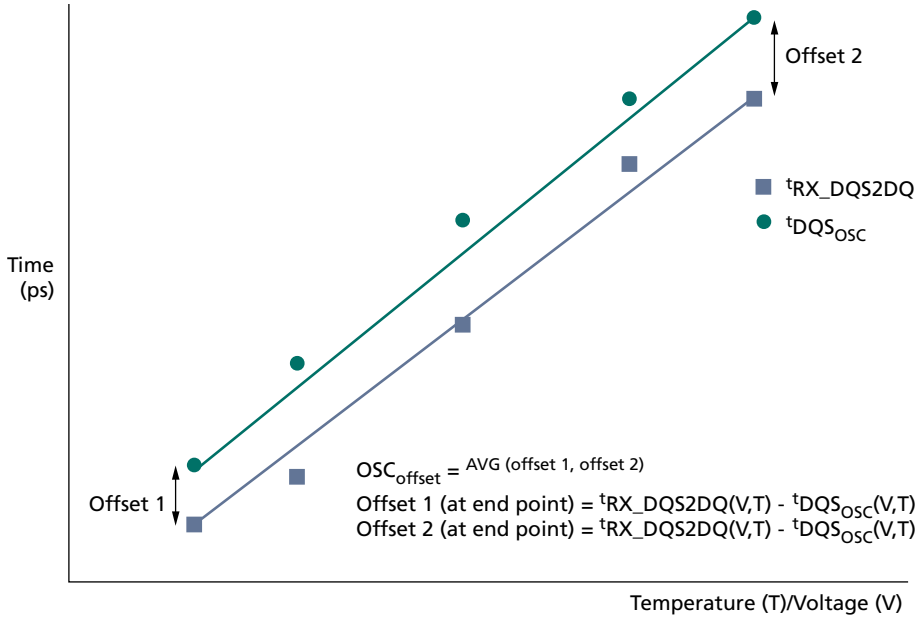
Interval Oscillator Matching Error

The interval oscillator matching error is defined as the difference between the DQS training circuit (interval oscillator) and the actual DQS clock tree across voltage and temperature.

Parameters:

- ^{t}RX_DQS2DQ: Actual DQS clock tree delay
- ^{t}DQSOSC: Training circuit (interval oscillator) delay
- OSCOffset: Average delay difference over voltage and temperature (shown in the following figure)
- OSCMatch: DQS oscillator matching error

Figure 135: Interval Oscillator Offset OSCoffset



OSCmatch:

$$OSC_{Match} = [^{t}RX\_DQS2DQ(V,T) - {}^{t}DQS,OSC(V,T) - OSC_{offset}]$$

^{t}DQSOSC:

$$^{t}DQS,OSC(V,T) = \frac{\text{Run time}}{2 \times \text{Count}}$$

Table 230: DQS Oscillator Matching Error Specification

Parameter	Symbol	MIN	MAX	Unit	Notes
DQS oscillator matching error	OSC_{Match}	-10	10	ps	1,2,3,4,5,6,7,8
DQS oscillator offset	OSC_{offset}	-150	150	ps	2,4,6,7

Notes: 1. OSC_{Match} is the matching error between the actual DQS and DQS interval oscillator over voltage and temperature.
2. This parameter is characterized or guaranteed by design.
3. The OSCmatch is defined as the following, where ^{t}RX_DQS2DQ (V,T) and ^{t}DQS,OSC (V,T) are determined over the same voltage and temperature conditions:

$$OSC_{Match} = [^{t}RX\_DQS2DQ(V,T) - {}^{t}DQS,OSC(V,T) - OSC_{offset}]$$

4. The oscillator run time must be at least 200ns for determining ^{t}DQS,OSC (V,T).

$$^{t}DQS,OSC(V,T) = \frac{Run\ time}{2 \times Count}$$

5. The input stimulus for ^{t}RX_DQS2DQ is consistent over voltage and temperature conditions.
6. The OSCoffset is the average difference of the endpoints across voltage and temperature.
7. These parameters are defined per channel.
8. ^{t}RX_DQS2DQ (V,T) delay is the average of DQS to DQ delay over the runtime period.
9. The matching error and offset of OSC came from DQS2DQ interval oscillator.

^{t}RX_DQS2DQ Offset Due to Temperature and Voltage Variation

As temperature and voltage change on the die, the DQS clock tree shifts and may require retraining. The oscillator is typically used to measure the amount of delay over a given time interval (determined by the controller), enabling the controller to compare the trained delay value to the delay value seen at a later time. The ^{t}RX_DQS2DQ offset due to temperature and voltage variation specification can be used for instances when the oscillator cannot be used to control the ^{t}RX_DQS2DQ.

Table 231: ^{t}RX_DQS2DQ Offset Due to Temperature and Voltage Variation: 3200-4800

Parameter	Symbol	3200		3600		4000		4400		4800		Units	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
^{t}RX_DQS2DQ_-temp	DQS to DQ offset temperature variation	-	12.75	-	11.34	-	10.20	-	9.28	-	8.50	ps/10°C	1,3
^{t}RX_DQS2DQ_-volt	DQS to DQ offset voltage variation	-	45.00	-	43.00	-	41.00	-	39.00	-	32.00	ps/50mV	2,3

Notes: 1. ^{t}RX_DQS2DQ max delay variation as a function of temperature.
2. ^{t}RX_DQS2DQ max delay variation as a function of the DC voltage variation for V_{DDQ} and V_{DD}. It includes the V_{DDQ} and V_{DD} AC noise impact for frequencies >20 MHz and max voltage of 45mVpk-pk from DC -20 MHz at a fixed temperature on the package. For tester measurement V_{DDQ}=V_{DD} is assumed
3. Absolute value of DQS to DQ offset.

Table 232: ^{t}RX_DQS2DQ Offset Due to Temperature and Voltage Variation: 5200-6400

Parameter	Symbol	5200		5600		6000		6400		Units	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
^{t}RX_DQS2DQ_temp	DQS to DQ offset temperature variation	-	7.85	-	7.29	-	6.80	-	6.38	ps/10°C	1,3
^{t}RX_DQS2DQ_volt	DQS to DQ offset voltage variation	-	30.00	-	TBD	-	TBD	-	TBD	ps/50mV	2,3

Notes: 1. ^{t}RX_DQS2DQ max delay variation as a function of temperature.
2. ^{t}RX_DQS2DQ max delay variation as a function of the DC voltage variation for V_{DDQ} and V_{DD}. It includes the V_{DDQ} and V_{DD} AC noise impact for frequencies >20 MHz and max voltage of 45mVpk-pk from DC -20 MHz at a fixed temperature on the package. For tester measurement V_{DDQ}=V_{DD} is assumed.

3. Absolute value of DQS to DQ offset.

Table 233: ^{t}RX_DQS2DQ Offset Due to Temperature and Voltage Variation: 6800-7600

Parameter	Symbol	6800		7200		7600		8000		8400/8800		Units	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
^{t}RX_DQS2DQ_-temp	DQS to DQ offset temperature variation	-	TBD	-	TBD	-	TBD	-	TBD	-	TBD	ps/10°C	1,3
^{t}RX_DQS2DQ_-volt	DQS to DQ offset voltage variation	-	TBD	-	TBD	-	TBD	-	TBD	-	TBD	ps/50mV	2,3

Notes: 1. ^{t}RX_DQS2DQ max delay variation as a function of temperature.
2. ^{t}RX_DQS2DQ max delay variation as a function of the DC voltage variation for V_{DDQ} and V_{DD}. It includes the V_{DDQ} and V_{DD} AC noise impact for frequencies >20 MHz and max voltage of 45mVpk-pk from DC -20 MHz at a fixed temperature on the package. For tester measurement V_{DDQ}=V_{DD} is assumed
3. Absolute value of DQS to DQ offset.

Table 234: ^{t}RX_DQS2DQ Offset Due to Temperature and Voltage Variation: 8000-8800

Parameter	Symbol	8000		8400		8800		Units	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
^{t}RX_DQS2DQ_temp	DQS to DQ offset temperature variation	-	TBD	-	TBD	-	TBD	ps/10°C	1,3
^{t}RX_DQS2DQ_volt	DQS to DQ offset voltage variation	-	TBD	-	TBD	-	TBD	ps/50mV	2,3

Notes: 1. ^{t}RX_DQS2DQ max delay variation as a function of temperature.
2. ^{t}RX_DQS2DQ max delay variation as a function of the DC voltage variation for V_{DDQ} and V_{DD}. It includes the V_{DDQ} and V_{DD} AC noise impact for frequencies >20 MHz and max voltage of 45mVpk-pk from DC -20 MHz at a fixed temperature on the package. For tester measurement V_{DDQ}=V_{DD} is assumed
3. Absolute value of DQS to DQ offset.

Duty Cycle Adjuster

The device supports a mode register adjustable duty cycle adjuster (DCA) to enable the memory controller to adjust the internally generated DQS clock tree and DQ duty cycle to compensate for systemic duty cycle errors of all DQS and DQs.

The DQS DCA is located before the DQS clock tree or equivalent place. The DCA requires a locked DLL state and affects the DQS and DQ duty cycle during the following operations:

- Read
- Read preamble training
- Read training pattern
- Mode register read

The controller can adjust the duty cycle through all DCA mode registers and can determine the optimal mode register setting for DCA in numerous ways.

DCA Range

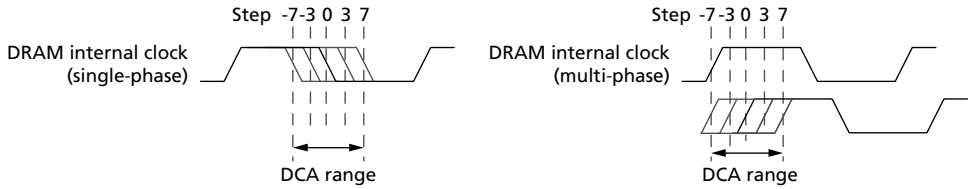
The global DCA step range is from -7 to +7, as defined in MR43 and MR44. The actual step size cannot be defined because the variation of duty cycle by changing DCA code is not linear.

Table 235: DCA Range

Parameter	Min/Avg/Max	Value	Unit	Notes
Duty cycle adjuster range	Min	28	ps	1
	Max	56		

Notes: 1. These values are guaranteed by design

Figure 136: DCA Range



Relationship Between DCA Code Change and Single/2-Phase Internal Clock(s)/DQS Timing

In the case where the DQS clock tree is implemented in a single/2-phase clock(s) scheme, the duty/cycle ratio of all DQS per device can be adjusted directly according to the internal clock(s) controlled by the DCA code.^{t}DQSCK is not changed by a DCA code change.

Using a 2-phase clock scheme, the rising edge of the 0° clock is the reference edge, while the 180° clock is adjusted based on 0° clock. The rising edge of 0° clock is for even burst bit data, and the rising edge of 180° clock is for odd burst bit data.

The global DCA adjustment uses the DCA for single/two-phase clock(s) mode register bits (MR43:OP[3:0]). A positive DCA adjustment results in a larger duty cycle ratio, while a negative DCA adjustment results in a smaller duty cycle ratio.

In addition to the global DCA adjustment, a per-pin DCA adjustment allows an additional step range of -3 to +3, per DQS/DQ. The 2-phase clock per-pin DCA adjustment uses the OP bits [3,1:0] of MR103 (DQSL_t), MR105 (DQSL_c), MR107 (DQSU_t), MR109 (DQSU_c), MR133 (DQL0), MR141 (DQL1), ..., MR253 (DQU7). The per-pin DCA adjustment is additive to the global DCA adjustment, as shown in the examples below:

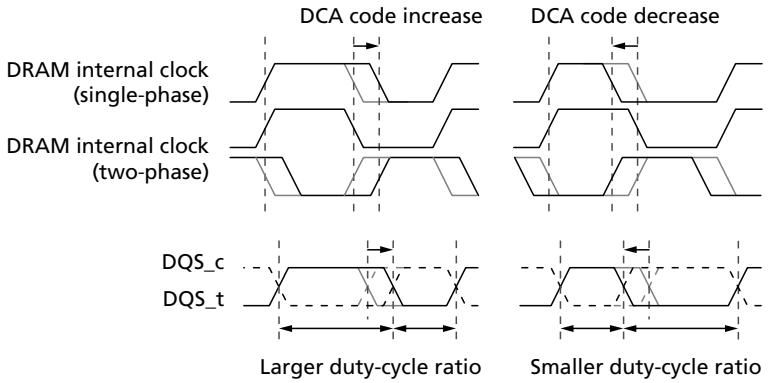
Table 236: DCA Range Examples (Not All Possible Combinations)

Global DCA Adjustment	Per-Pin DCA Adjustment	Total DCA Adjustment at Pin
DCA Step -3	DCA Step -2	DCA Step -5
DCA Step -2	DCA Step +2	DCA Step -0
DCA Step 0	DCA Step +1	DCA Step +1
DCA Step +2	DCA Step -3	DCA Step -1
DCA Step +4	DCA Step +3	DCA Step +7
DCA Step +7	DCA Step +2	DCA Step +9

Like the global DCA adjustment, the actual step size for the per-pin DCA adjustment cannot be defined because the variation of duty cycle by changing DCA code is not linear; however, the per-pin DCA adjustment is approximately the same as the global DCA adjustment.

Mode register OP bits associated with the IBCLK and QBCLK may not be supported on the device with a 2-phase clock scheme.

Figure 137: Example: DCA Code Change and Single/2-Phase Internal Clock(s)/DQS



Relationship Between DCA Code Change and 4-Phase Internal Clock(s)/DQS Timing

In the case where the DQS clock tree implemented in a 4-phase clocks scheme, the even and odd duty/cycle ratio of all DQS per device can be adjusted respectively because the internal 4-phase clocks can be independently controlled by the DCA code.

In case of 4-phase internal clocks, for example, because QCLK(90°)/IBCLK(180°)/QBCLK(270°) are adjusted based on ICLK(0°), the controller can first confirm the first BL is synchronized with ICLK(0°), and then perform the full DCA training operation, which needs to have an even number of MRR (or Read) - MRR (or Read) timing to avoid confusion whether the first BL is synchronized with ICLK(0°) or IBCLK(180°).

Figure 138: Relationship Between DCA Code Change for QCLK and the 4-Phase Internal Clock(s)/DQS Waveform

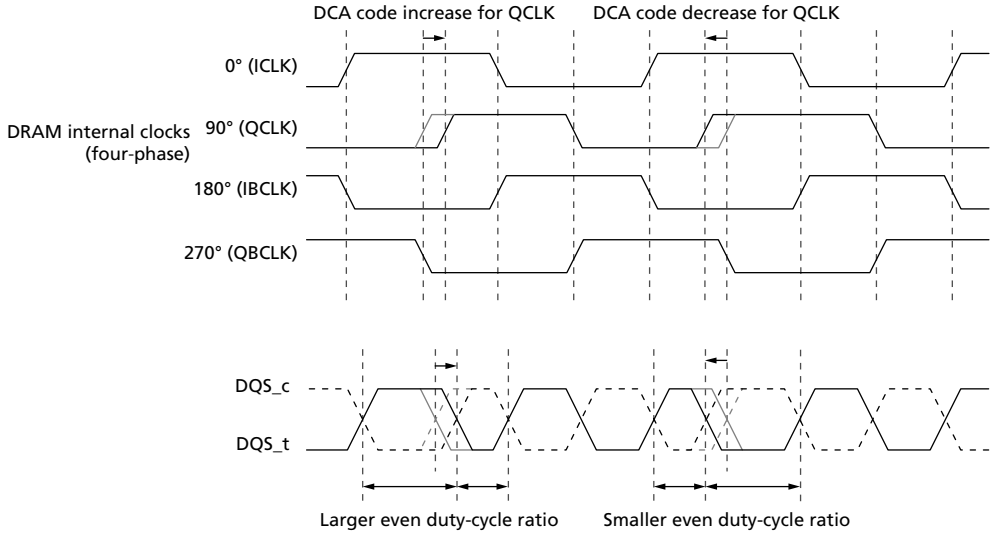


Figure 139: Relationship between DCA Code Change for IBCLK and the 4-Phase Internal Clock(s)/DQS

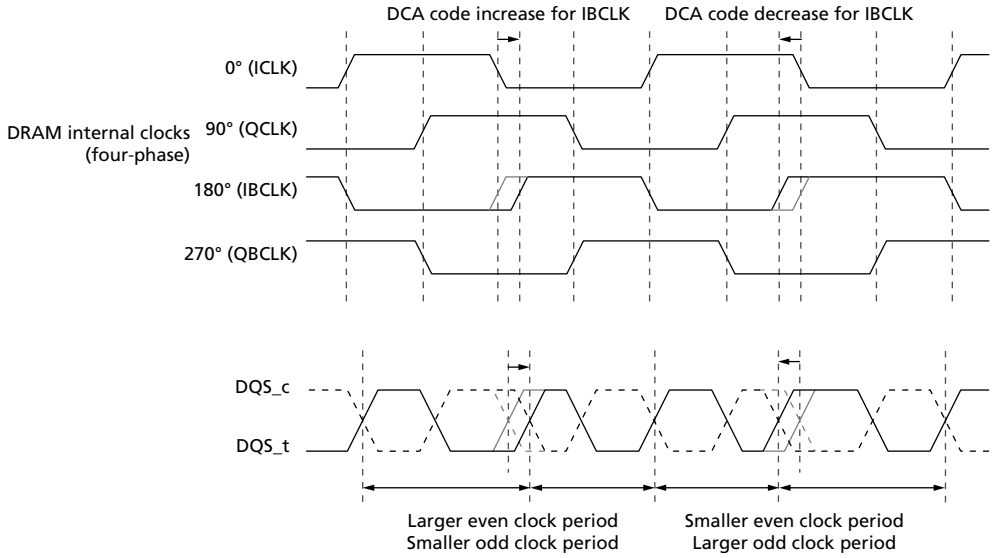
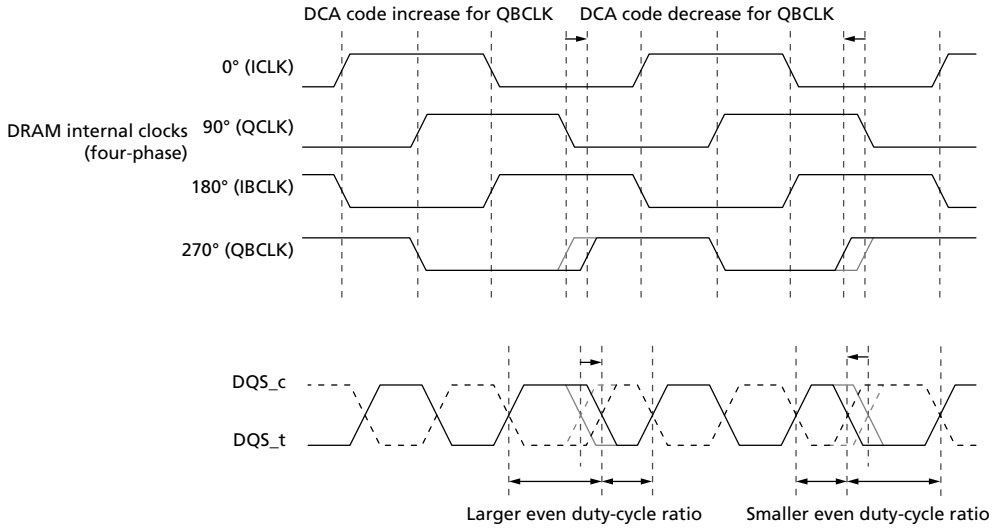


Figure 140: Relationship between DCA Code Change for QBCLK and the 4-Phase Internal Clock(s)/DQS



Relationship Between DCA Code Change and DQs Output/DQS Timing

The DQS DCA code change effect to DQ oupput is as follows. The rising edge of DQS_t affects the even data output. The falling edge of DQS_t affects the falling edge of the odd data output.

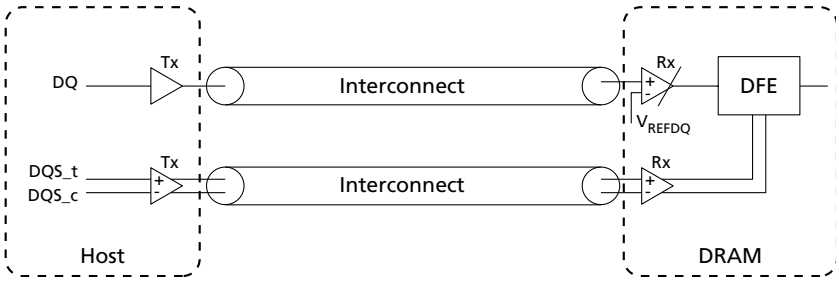
Decision Feedback Equalization

At data rates ≥2933 MT/s, signal degradation due to inter symbol interference (ISI) is expected to increase and the data eye at the device ball is expected to be closed. Because the memory channel is very reflective due to the many impedance mismatched points that exist along the memory subsystem, ISI due to reflections is expected to increase.

Traditional methods of characterizing the receiver using the input eye mask are no longer sufficient. DDR5 requires equalization to help improve (or open up) the data eyes after data is latched by the receiver. A 4-tap decision feedback equalization (DFE) helps equalize the DQ signals without amplifying the noise due to insertion loss and reflections, which is a common side effect of other equalization techniques (for example, CTLE). The following figure shows an example of a memory subsystem with DFE circuit included on the device.

At the 1980-2100 MT/s data rates, the device's DFE is disabled. Setting either the global DFE gain and tap 1-4 enable bits to disable or setting all DFE gain and tap 1-4 bias bits to step 0 disables the DFE.

Figure 141: Memory Subsystem with DFE Circuit on the Device

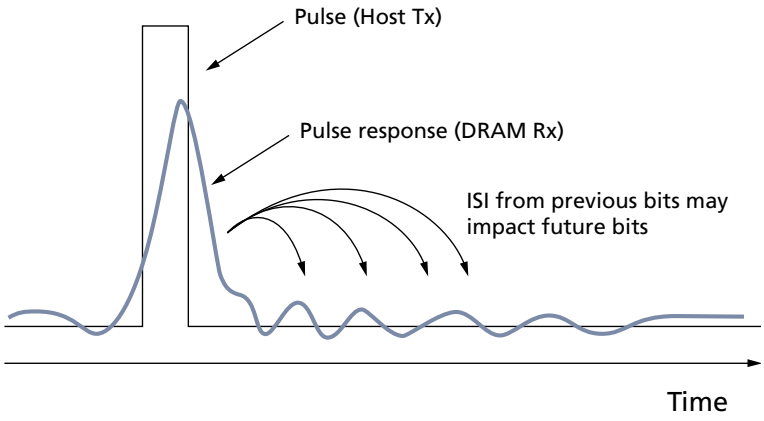


Pulse Response of a Reflective Memory Channel

A reflection-dominated channel, such as those found in a memory subsystem, is anticipated to substantially reduce data eye at the device ball due to the effects of insertion loss and reflections. The following figure illustrates what a pulse response of a very reflective channel might look like.

The attenuation, as well as the ringing of the signal, can cause the data eye to close at the device ball. Moreover, the ringing can impact future bits that are being sent into the channel (that is, if the pulse response is for bit n, then the ringing from bit n can impact the signal integrity of future bits n+1, n+2, n+3, n+4, etc). Phrased another way, the signal integrity of any bit (for example bit n) can be impacted by the signals of the previous bits (n-1, n-2, n-3, n-4, etc).

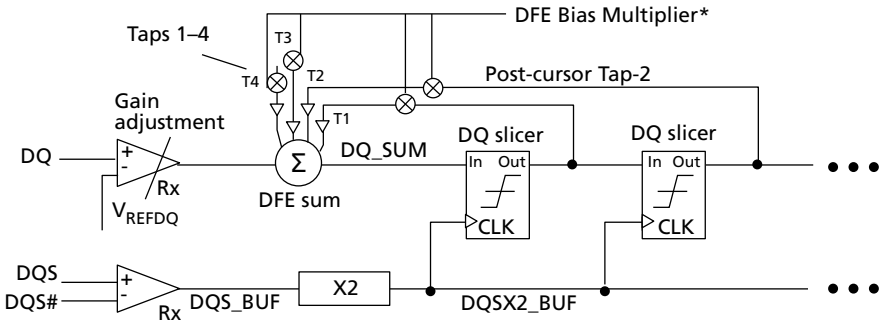
Figure 142: Pulse Response of a Reflective Channel



DFE Components

The 4-tap DFE subsystem consists of a gain amplifier, a DFE summer, four DQ slicers (also called taps) with outputs that loop back to the DFE summer, and a coefficient multiplier for each tap. The gain control of the front end is used to ensure the cursor or the current bit is in a congruent relationship with the ISI correction required for the channel. The taps T1, T2, T3, T4 coefficients provide the corrections needed to the current bit by adding or subtracting the effects of ISI of the previous bits.

Figure 143: 4-Tap DFE



*Vendor-specific; consult vendor data sheet

The mode registers shown in the following tables are used by the memory controller to set the strengths of the gain amplifier and the strengths of the correction of the taps to adapt the ISI cancellation in accordance with the channel performance. Optimal values used for the strengths of the gain amplifier and of the taps are system-dependent, and are usually obtained through a combination of simulations, platform characterizations, and other methods.

Table 237: DFE Gain Adjustment MIN/MAX Ranges (3200-7200)

Description	3200-4800			5200-6400			6800-7200			Unit	Notes
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
DFE gain bias max	6	–	–	6	–	–	TBD	-	-	dB	1,2,3,4
DFE gain bias min	–	–	-6	–	–	-6	-	-	TBD	dB	1,2,3,4
DFE gain bias average step size	-	2	-	-	2	-	-	TBD	-	dB	1,2,3,4
DFE GAIN bias DNL	-1	–	+1	-1	–	+1	TBD	-	TBD	dB	1,2,3,4
DFE GAIN bias INL	-1	–	+1	-1	–	+1	TBD	-	TBD	dB	1,2,3,4
DFE gain bias tolerance time	^{t}DFE	-	-	^{t}DFE	-	-	TBD	-	-	ns	1,2,3,4

Notes: 1. All parameters are defined over the Rx V_{REF} range from 0.5 * V_{DDQ} to 0.9 * V_{DDQ}.
2. DFE gain bias are for all voltage and temperature ranges.
3. These values are defined over the entire voltage and temperature ranges.

4. These parameters are to evaluate the relative ratio of DFE gain bias settings, and absolute values of all parameters are not subject to silicon validation or production tests.

Table 238: DFE Gain Adjustment MIN/MAX Ranges (7600-8800)

Description	7600-8000			8400-8800			Unit	Notes
	MIN	TYP	MAX	MIN	TYP	MAX		
DFE gain bias max	TBD	–	–	TBD	–	–	dB	1,2,3,4
DFE gain bias min	–	–	TBD	–	–	TBD	dB	1,2,3,4
DFE gain bias average step size	-	TBD	-	-	TBD	-	dB	1,2,3,4
DFE GAIN bias DNL	TBD	–	TBD	TBD	–	TBD	dB	1,2,3,4
DFE GAIN bias INL	TBD	–	TBD	TBD	–	TBD	dB	1,2,3,4
DFE gain bias tolerance time	TBD	-	-	TBD	-	-	ns	1,2,3,4

Notes: 1. All parameters are defined over the Rx V_{REF} range from 0.5 * V_{DDQ} to 0.9 * V_{DDQ}.
2. DFE gain bias are for all voltage and temperature ranges.
3. These values are defined over the entire voltage and temperature ranges.
4. These parameters are to evaluate the relative ratio of DFE gain bias settings, and absolute values of all parameters are not subject to silicon validation or production tests.

Table 239: DFE Tap Coefficients MIN/MAX Ranges (3200-7200)

Description	3200-4800			5200-6400			6800-7200			Unit	Notes
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
DFE tap-1 bias max	50	–	–	50	–	–	TBD	-	-	mV	1,2,4,5,7
DFE tap-1 bias min	–	–	-200	–	–	-200	-	-	TBD	mV	1,2,4,6,7
DFE tap-2 bias max	75	–	–	75	–	–	TBD	-	-	mV	2,4,5,7
DFE tap-2 bias min	–	–	-75	–	–	-75	-	-	TBD	mV	2,4,6,7
DFE tap-3 bias max	60	–	–	60	–	–	TBD	-	-	mV	2,4,5,7
DFE tap-3 bias min	–	–	-60	–	–	-60	-	-	TBD	mV	2,4,6,7
DFE tap-4 bias max	45	–	–	45	–	–	TBD	-	-	mV	2,4,5,7
DFE tap-4 bias min	–	–	-45	–	–	-45	-	-	TBD	mV	2,4,6,7
DFE tap bias average step size	–	5	–	–	5	–	-	TBD	-	mV	2,3,4,7
DFE tap bias DNL	-2.5	–	+2.5	-2.5	–	+2.5	TBD	-	TBD	mV	2,3,4,7
DFE tap bias INL	-2.5	–	+2.5	-2.5	–	+2.5	TBD	-	TBD	mV	2,3,4,7
DFE tap bias step time	^{t}DFE	–	–	^{t}DFE	–	–	TBD	-	-	mV	2,3,4

Notes: 1. As speed increases, the impact of loss from the channel makes the bias range of the first cursor asymmetric.
2. Values are defined for the entire voltage, temperature range, and Rx V_{REF} range from 0.5 * V_{DDQ} to 0.9 * V_{DDQ}.
3. Values are identical for taps 1-4.
4. These parameters are suggested to evaluate relative ratio of DFE taps 1~4, and absolute values of all parameters are not subject to silicon validation nor production test.
5. For the pulse response (...000010000... pulse pattern), a positive value corrects a negative post-cursor by setting the DFE tab bias sign bit (MR113~116, OP[6]) to 0 to apply a positive correction.
6. For the pulse response (...000010000... pulse pattern), a negative value corrects a positive post-cursor by setting the DFE tab bias sign bit (MR113~116, OP[6]) to 1 to apply a negative correction. For example, in a memory channel

where the ISI during the first post-cursor is dominated by bandwidth loss, the expected tap-1 bias sign bit will be set to 1.

7. Check the multiplier that is applied to the DFE tap bias setting (MR113, MR114, MR115, etc.) for total DFE feedback swing implemented in hardware.

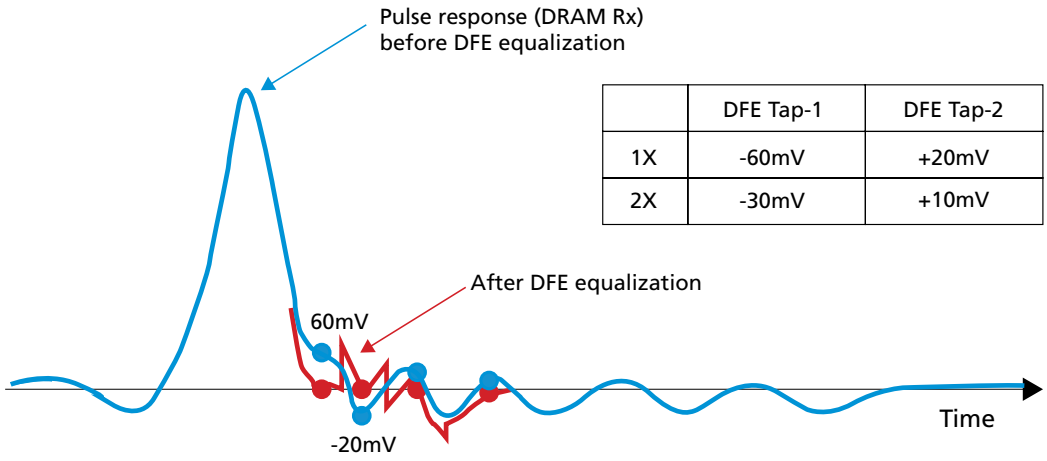
Table 240: DFE Tap Coefficients MIN/MAX Ranges (7600-8800)

Description	7600-8000			8400-8800			Unit	Notes
	MIN	TYP	MAX	MIN	TYP	MAX		
DFE tap-1 bias max	TBD	–	–	TBD	–	–	mV	1,2,4,5,7
DFE tap-1 bias min	–	–	TBD	–	–	TBD	mV	1,2,4,6,7
DFE tap-2 bias max	TBD	–	–	TBD	–	–	mV	2,4,5,7
DFE tap-2 bias min	–	–	TBD	–	–	TBD	mV	2,4,6,7
DFE tap-3 bias max	TBD	–	–	TBD	–	–	mV	2,4,5,7
DFE tap-3 bias min	–	–	TBD	–	–	TBD	mV	2,4,6,7
DFE tap-4 bias max	TBD	–	–	TBD	–	–	mV	2,4,5,7
DFE tap-4 bias min	–	–	TBD	–	–	TBD	mV	2,4,6,7
DFE tap bias average step size	–	TBD	–	–	TBD	–	mV	2,3,4,7
DFE tap bias DNL	TBD	–	TBD	TBD	–	TBD	mV	2,3,4,7
DFE tap bias INL	TBD	–	TBD	TBD	–	TBD	mV	2,3,4,7
DFE tap bias step time	TBD	–	–	TBD	–	–	mV	2,3,4

Notes: 1. As speed increases, the impact of loss from the channel makes the bias range of the first cursor asymmetric.
2. Values are defined for the entire voltage, temperature range, and Rx V_{REF} range from 0.5 * V_{DDQ} to 0.9 * V_{DDQ}.
3. Values are identical for taps 1-4.
4. These parameters are suggested to evaluate relative ratio of DFE taps 1~4, and absolute values of all parameters are not subject to silicon validation nor production test.
5. For the pulse response (...000010000... pulse pattern), a positive value corrects a negative post-cursor by setting the DFE tab bias sign bit (MR113~116, OP[6]) to 0 to apply a positive correction.
6. For the pulse response (...000010000... pulse pattern), a negative value corrects a positive post-cursor by setting the DFE tab bias sign bit (MR113~116, OP[6]) to 1 to apply a negative correction. For example, in a memory channel where the ISI during the first post-cursor is dominated by bandwidth loss, the expected tap-1 bias sign bit will be set to 1.
7. Check the multiplier that is applied to the DFE tap bias setting (MR113, MR114, MR115, etc.) for total DFE feedback swing implemented in hardware.

The figure below is an example of 1X and 2X multiplier cases which shows how the DFE tab biases move differently in hardware with the same pulse response.

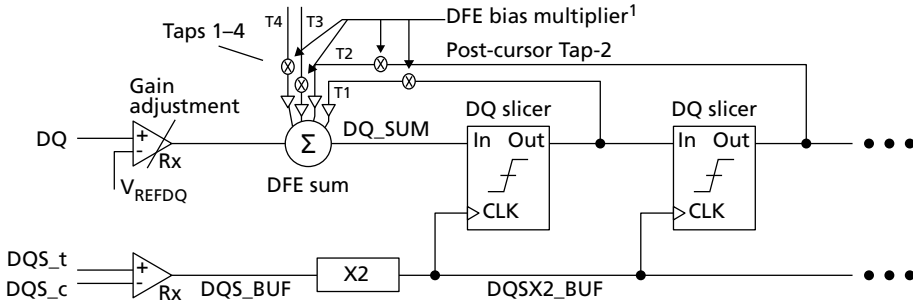
Figure 144: Example Case of DFE Tap Biases Moving with 1X and 2X Multiplier



	DFE Tap-1	DFE Tap-2
1X	-60mV	+20mV
2X	-30mV	+10mV

The device may implement 1-way interleave, 2-way interleave, or 4-way interleave 4-tap DFE memory circuitry. The 1-way interleaved 4-tap DFE architecture (shown below) requires a strobe multiplier, which is at Nyquist rate. The output of the DQ slicer runs at same speed as received data.

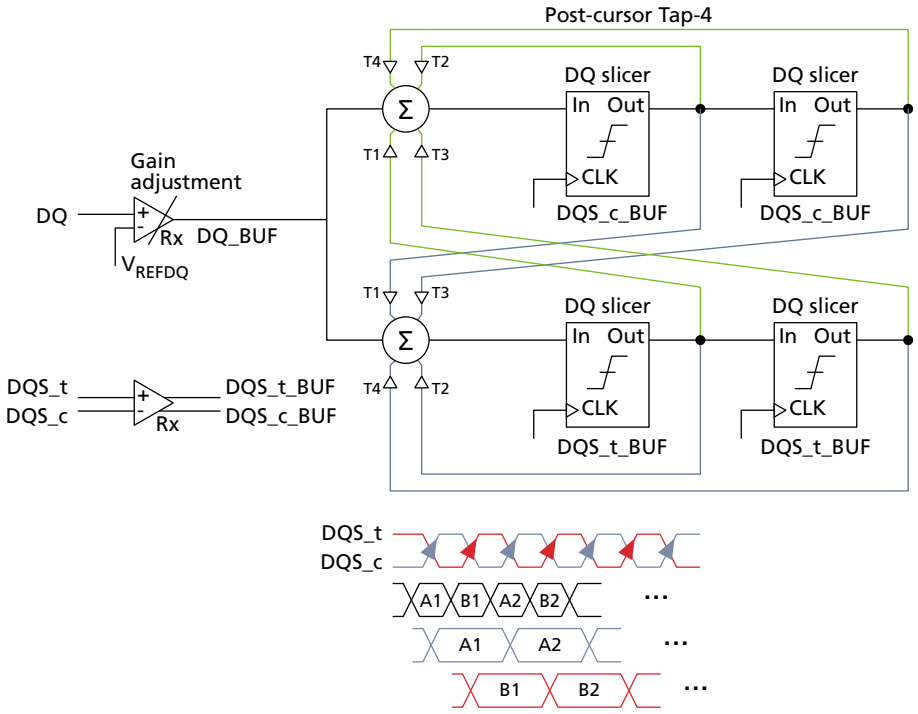
Figure 145: 1-Way Interleave 4-Tap DFE



Note: 1. Vendor-specific; consult vendor data sheet.

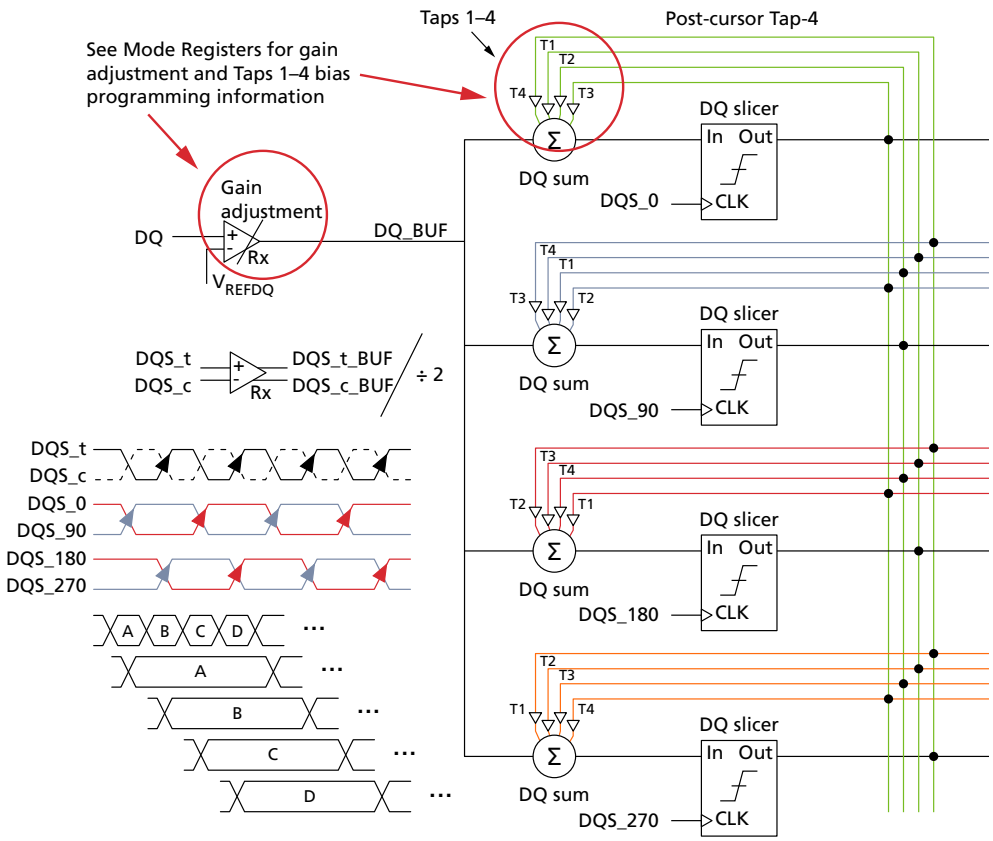
A 2-way interleave 4-tap architecture (shown below), can use the strobe as-is. In this case, the output of the DQ slicer runs at half the speed as received data.

Figure 146: 2-Way Interleave 4-Tap DFE



A 4-way interleave 4-tap architecture (shown below), requires a divided clock. In this case, the output of the DQ slicer runs at one-quarter the speed as received data.

Figure 147: 4-Way Interleave 4-Tap DFE



Loopback Mode

With loopback mode, the device feeds a received signal/data to an external receiver for multiple purposes. This mode enables the host (memory controller or test instrument) to monitor the data that was just sent to the device without having to store the data in the device or use READ operations to retrieve data sent to the device.

This mode requires data be sent to the loopback path before it is sent to the core so that READ/WRITE commands are not required for loopback to be operational. Additionally, there are inherent limitations when characterizing the receiver using statistical analysis methods such as bit error rate (BER) analysis. For example, at BER=1E+$^{-16}$, the following occurs: there is not enough memory depth in the device to store all the 1E+^{16} data; the amount of time to perform multiple READ/WRITE commands to/from the memory is prohibitively long; because the amount of time involved performing these operations is much longer than the refresh rate interval, the host or memory controller must also manage refreshes during testing to ensure data retention; and, limited pattern depth means limited inter symbol interference (ISI) and limited random jitter (Rj), and therefore, limited errors at the receiver.

Use of loopback is a necessity for characterizing the receiver without the limitations and complexities of other traditional validation methods. Loopback can also be used during normal operation, as described in the Loopback Write Burst Output Mode section below.

Loopback Output Definition

Loopback requires two output pins: one single-ended loopback strobe (LBDQS) and one single-ended loopback data (LBDQ).

The default RTT state for loopback is RTT_OFF, designated by MR36:OP[2:0] = 000b. In this state, both the LBDQS and LBDQ outputs are disabled. If the loopback pins of several DDR5 devices are connected together and the end device needs termination, there is a RZQ/5 (48 ohms) option available by setting MR36:OP[2:0] = 101b.

Selecting a loopback output value via MR53:OP[4:0] other than the default loopback disabled (MR53:OP[4:0] = 00000b) results in the LBDQS and LBDQ pins transitioning from RTT_OFF to a device drive state.

Before changing the loopback output select from upper byte to lower byte or vice versa, the host must set loopback output select to MR53:OP[4:0]=00000b to disable loopback mode.

The LBDQS output transitions with the differential input crossing point of DQS_t/DQS_c for x4 and x8 device configurations, plus latency. LBDQS transitions with DQSL_t/DQSL_c for x16 devices if DML or a DQL is selected for output, or with DQSU_t/DQSU_c for x16 devices if DMU or a DQU is selected for output. If an RFU output is selected, or if DMU or a DQU is selected on a x4 or x8 device where DQSU_t/DQSU_c is not valid, LBDQS remains in a device drive state.

The LBDQ output transitions with the receiver data state of the DM or DQ pin selected by MR53:OP[4:0]. If an RFU output is selected, or if an invalid output for device configuration is selected, the LBDQ output remains in a device drive state.

Table 241: Loopback Output Definition

Condition	LBDQS	LBDQ	Notes
Loopback disabled	RTT_Loopback	RTT_Loopback	
Loopback enabled	Selected phase	Selected phase and selected DQ	1

Notes: 1. Selection of an unsupported RFU/DM/DQ for the device configuration results in undefined LBDQS toggling and the LBDQ in a driven state.

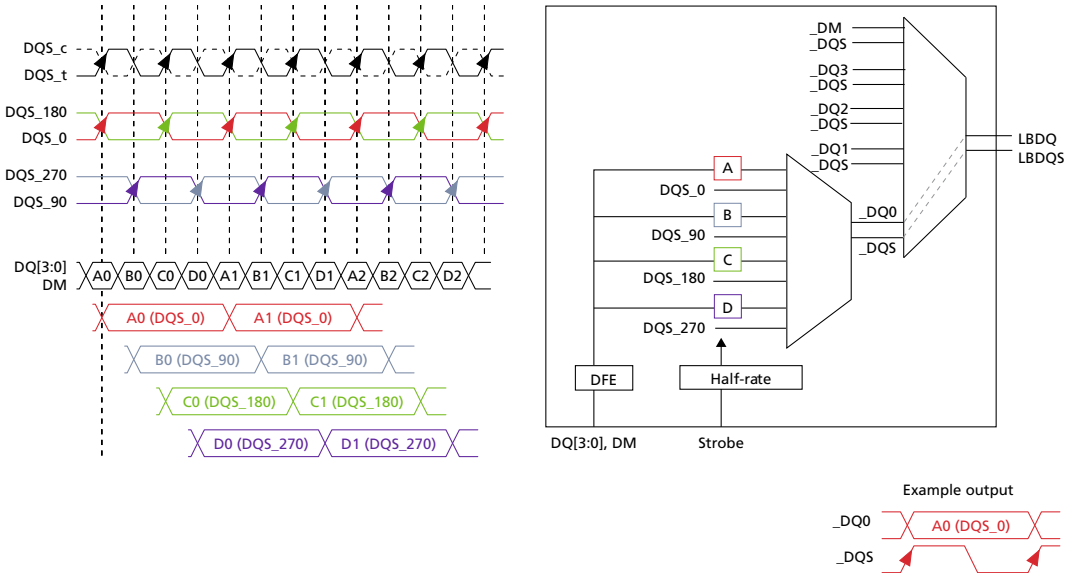
Loopback Phase

Due to the high data rates of the device, loopback may be implemented with 2-way or 4-way interleaved outputs. With a 2-way implementation, the DQS and selected DM/DQ are sampled and output every 1CK or 2UI. Similarly, with a 4-way implementation, the DQS and selected DM/DQ are sampled and output every 2CK or 4UI.

To be able to sample all bits with a 2-way or 4-way interleave implementation, the loopback select phase programmed in MR53:OP[6:5] allows selection of the DQS/DM/DQ phase to be output. In 2-way mode, Phase A and Phase B are valid options. In 4-way mode, Phase A, Phase B, Phase C and Phase D are valid options.

The figure below shows an example loopback implementation for a four-way interleave x4 device. This example requires a divided clock to produce DQS_0, DQS_90, DQS_180 and DQS_270. Phase A-D refers to the four-bit naturally aligned bits in a data stream. The output of the DQ slicer runs at one-quarter the speed as received data. In a four-way interleave design, the data is received at full speed, but internally the data is latched only at quarter speed. For example, if the input bit stream consists of A, B, C, and D, the multiplexer input A receives data bit A and strobe DQS_0; multiplexer input B receives data bit B and strobe DQS_90; multiplexer input C receives data bit C and strobe DQS_180; and multiplexer input D receives data bit D and DQS_270.

Figure 148: Example: Four-Way Interleave Loopback Circuit on a x4 Device



Loopback Output Mode

Loopback output mode selects whether to output LBDQS and LBDQ in normal output mode or write burst output mode, based on MR53:OP[7]. In the default normal output mode (MR53:OP[7] = 0b), the selected DM/DQ state is captured with every DQS_t/DQS_c toggle for the selected loopback phase. In write burst output mode (MR53:OP[7] = 1b), the selected DM/DQ state is output on LBDQ when qualified by the write enable, which means data is only captured during the write burst and not during the preamble or postamble.

Loopback Normal Output Mode (Default)

In normal output mode (MR53:OP[7] = 0b), the selected DM/DQ state is captured with every DQS_t/DQS_c toggle for the selected loopback phase and output on LBDQ. The LBDQS output is delayed by ^{t}LBDLY from the selected DQS_t/DQS_c loopback phase. Phase C and D are inverted from Phase A and B, respectively. Since no WRITE commands are required in normal output mode, MR settings pertaining to preamble, postamble, and CWL are ignored by the loopback function. Additional requirements for normal output mode:

- Loopback in normal output mode is not supported after completing write leveling training with internal write timing mode set MR2:OP[7]=1.
- DQS must be driven differentially LOW (DQS_t low, DQS_c high) prior to entry into normal output mode.
- DQS_t/DQS_c must be continuously driven during loopback operation. (HiZ state not allowed.)
- Only DSEL and MRW commands applied at command pins during normal ouput mode.
- RESET is required to exit loopback normal output mode.

No DFE reset is assumed after first rising edge of DQS_t. Device array data is not guaranteed after entering normal output mode.

Loopback Normal Output Mode Timing Diagrams

Figure 149: Loopback Normal Output Mode Entry

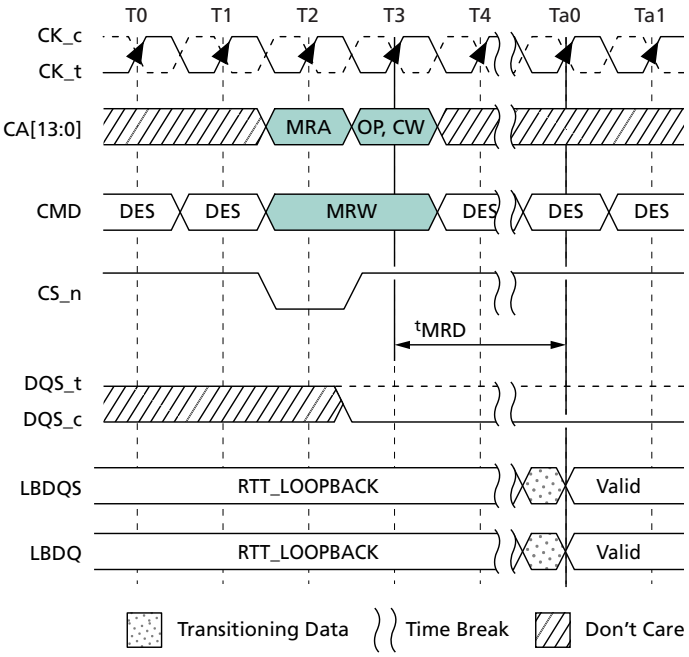


Figure 150: Loopback Normal Output 4-Way Mode Phase B Example

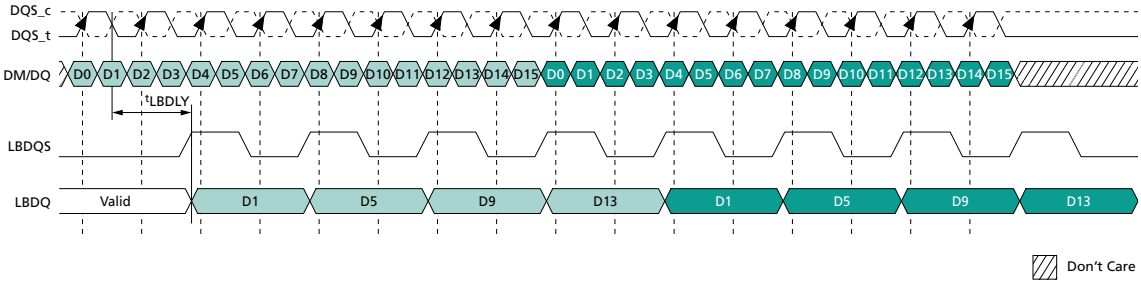


Figure 151: Loopback Normal Output 4-Way Mode Phase B 1CK Mid Gap Example

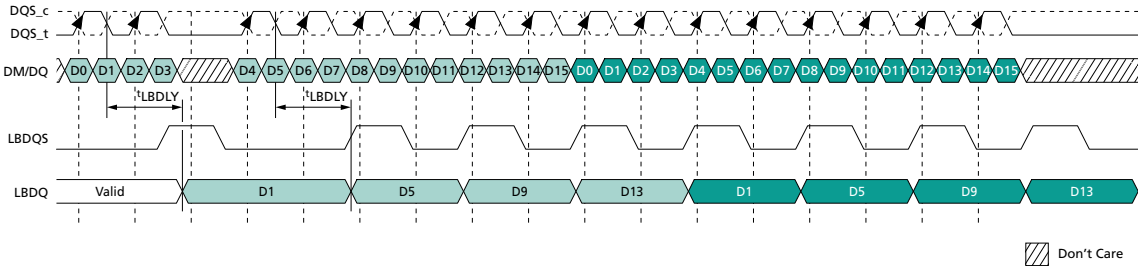


Figure 152: Loopback Normal Output 4-Way Mode Phase B 2CK Gap Example

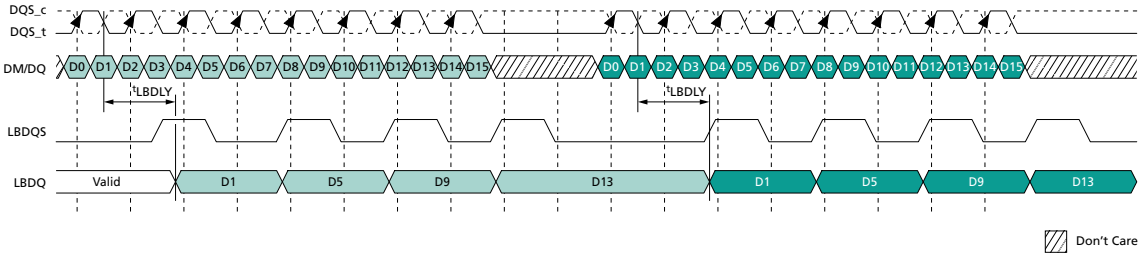
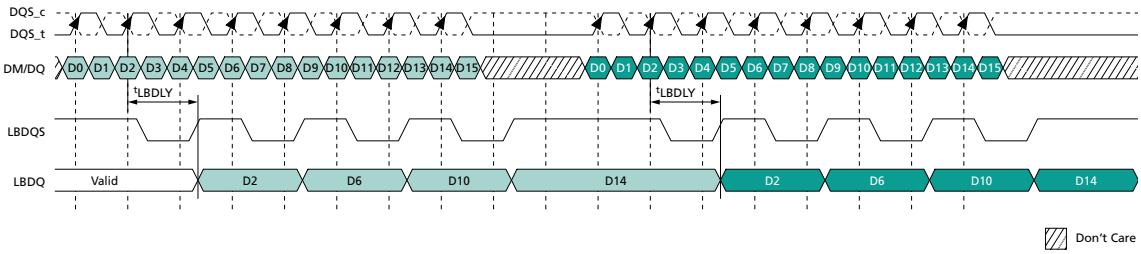


Figure 153: Loopback Normal Output 4-Way Mode Phase C 2CK Gap Example



Loopback Normal Mode with CRC Output Timings

Figure 154: Loopback Normal Output 4-Way Mode Phase B with CRC, No Gap

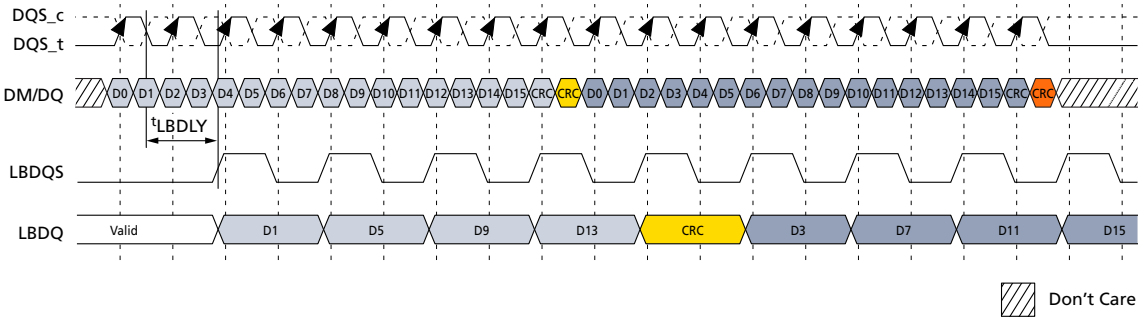


Figure 155: Loopback Normal Output 4-Way Mode Phase B with CRC, 1CK Gap

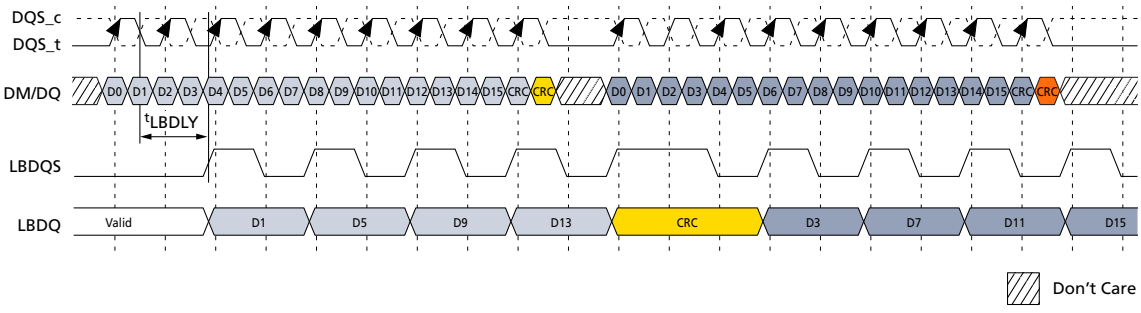
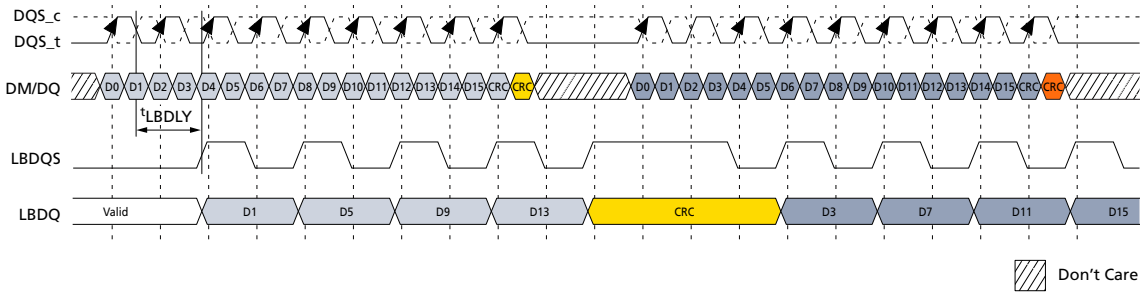


Figure 156: Loopback Normal Output 4-Way Mode Phase B with CRC, 2CK Gap



Loopback Write Burst Output Mode

In write burst output mode (MR53:OP[7] = 1b), loopback data is only generated during the write burst, so it is effectively masked for the DQS toggles during the preamble or postamble. Normal WRITE operation for the command, DQS and DM/DQ, is assumed. MR settings pertaining to preamble, postamble, and CWL apply, as they do for any WRITE command.

To prevent loopback interference on the device within the normal data path, the device optionally may output the second preamble pulse for the special case of WPRE=4CK and selection of Phase C or D for data burst bit phase alignment or Phase A or B for strobe phase alignment. With this behavior, all phases are inverted from normal behavior.

Implementation of 2-way or 4-way interleave loopback introduces complexity in write burst mode when the DQS toggle is not continuous. If the DQS toggle is continuously generated by WRITE commands spaced BL/2, loopback aligns the LBDQS/LBDQ output with the selected phase for all write bursts. In cases where gaps in WRITE commands are greatre than BL/2, the phase is determined by the analysis of the conditions.

Table 242: Loopback Output Phase

Write-to-Write Separation	Phase	Notes
X = BL/2	Selected	
X < BL/2	Determined via analysis of specific conditions	1

Notes: 1. Specific conditions include 2-way/4-way interleave implementation, selected phase, data rate, preamble, postamble, CRC and write burst gap duration.

In the case where continuous bursts are not issued in loopback write burst output mode, selection of Phase C or D for data burst alignment or Phase A or B for strobe phase alignment may result in the last ^{t}LBQSH width of a burst that does not comply with specifications. Additional requirements for write burst output mode:

- Write leveling training is required prior to write burst loopback operation.
- All write timing and voltage requirements must be followed. Failure to meet this requirement results in unknown data written to the device, and the loopback pins may not output the captured input data as expected.

Loopback Write Burst Output Mode Timing Diagrams

Figure 157: Loopback Write Burst Output 4-Way Mode Phase B WPRE = 2CK Example

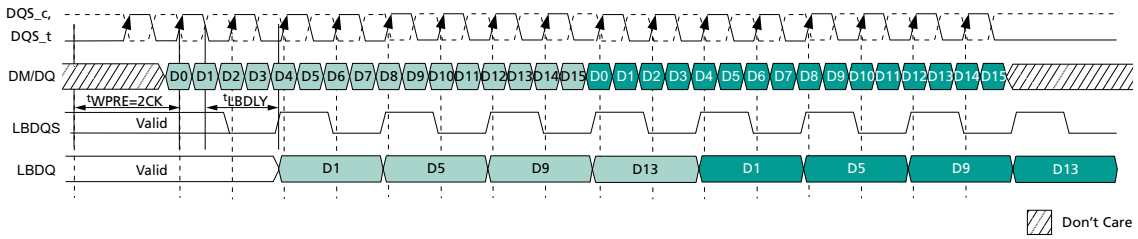


Figure 158: Loopback Write Burst Output 4-Way Mode Phase C WPRE = 2CK Example

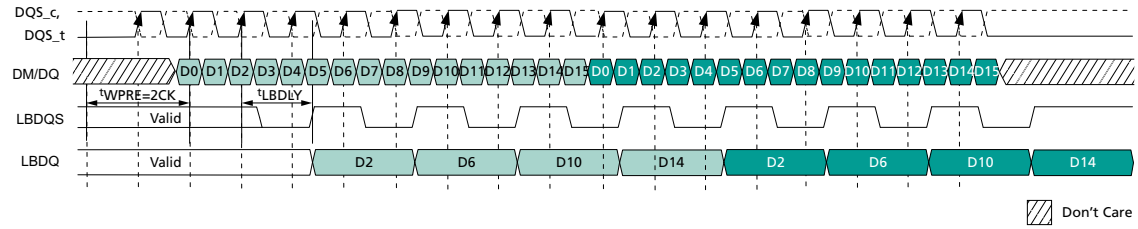


Figure 159: Loopback Write Burst Output 4-Way Mode Phase B Data Burst Bit and Phase D Strobe Alignment WPRE = 4CK Optional Example

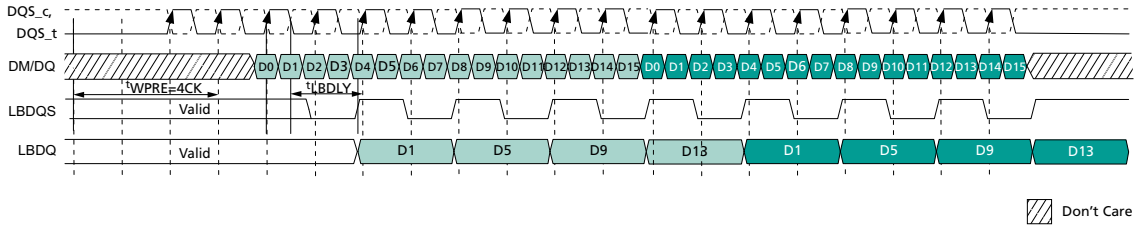
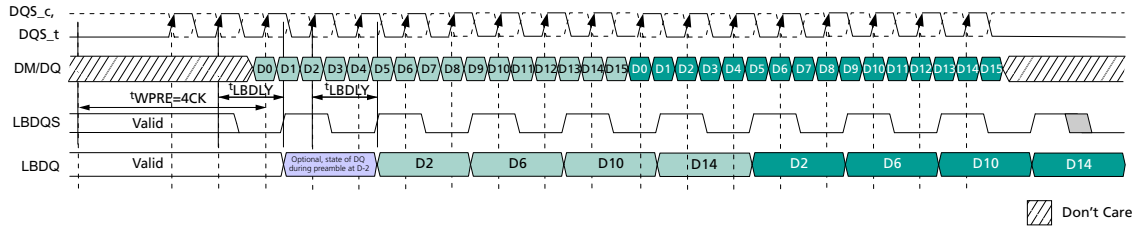
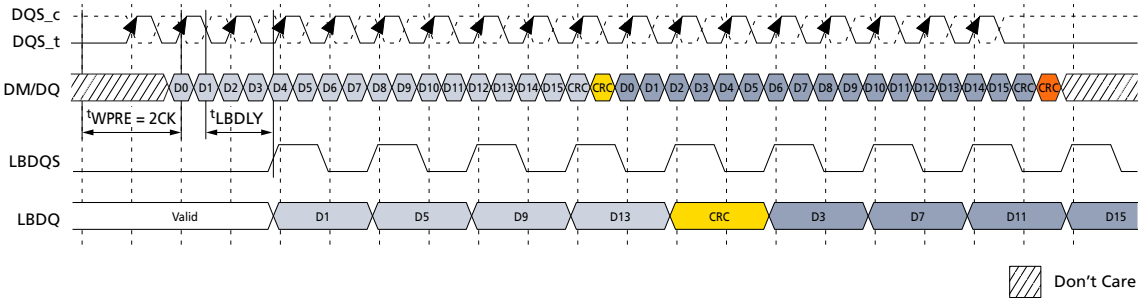


Figure 160: Loopback Write Burst Output 4-Way Mode Phase C Data Burst Bit and Phase A Strobe Alignment WPRE = 4CK Optional Example



Loopback Write Burst with CRC Output Mode Timing Diagrams

Figure 161: Loopback Write Burst with CRC Output Mode 4-Way Phase B with CRC, No Gap



Loopback Timing and Levels

The LBDQS output is delayed from the selected DQS_t/DQS_c loopback phase. The timing parameter, ^{t}LBDLY, is shown in the following table.

Table 243: Loopback LBDQS Output Timing (3200-6400)

Speed		3200/3600/4000/4400		4800/5200		5600/6000/6400		Unit
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
Loopback Timing:LBDQS Delay from selected DQS loopback phase	^{t}LBDLY	-	20	-	20	-	20	ns

Table 244: Loopback LBDQS Output Timing (6800-8800)

Speed		6800/7200		7600/8000		8400/8800		Unit
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
Loopback Timing:LBDQS Delay from selected DQS loopback phase	^{t}LBDLY	-	TBD	-	TBD	-	TBD	ns

The interaction between LBDQS and LBDQ is described in the Loopback Output Timing section. ODT for loopback is described in the On-Die Termination for Loopback Signals section. Output driver electrical characteristics for loopback is described in the Output Driver DC Electrical Characteristics for Loopback Signals LBDQS, LBDQ section.

Cyclical Redundancy Check

CRC Polynominal and Logic Equation

The device supports cyclical redundancy check (CRC) for READ and WRITE operations, enabled by separate mode register bits. Write CRC and data mask (DM) functions are not supported simultaneously and cannot be enabled together.

The CRC polynomial is the ATM-8 HEC, X^8+X^2+X^1+1

A combinatorial logic block implementation of this 8-bit CRC for 64-bits of data contains TBD two-input XOR gates contained in eight 6 XOR gate deep trees.

Table 245: Error Detection Details

Error Type	Detection Capability
Random single-bit error	100%
Random double-bit error	100%
Random odd count error	100%
Random multi-bit error within two adjacent transfers	100%

CRC Combinatorial Logic Equations

```
module CRC8_D64;
// polynomial: (0 1 2 8)
// data width: 64
// convention: the first serial data bit is D[63]
// initial condition all 0 implied
function [7:0]
nextCRC8_D64;
input [63:0] Data;
reg [63:0] D;
reg [7:0] NewCRC;
begin
D = Data
;
NewCRC[0] = D[63] ^ D[60] ^
D[56] ^ D[54] ^ D[53] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^
D[45] ^ D[43] ^ D[40] ^ D[39] ^ D[35] ^ D[34] ^ D[31] ^
D[30] ^ D[28] ^ D[23] ^ D[21] ^ D[19] ^ D[18] ^ D[16] ^
D[14] ^ D[12] ^ D[8] ^ D[7] ^ D[6] ^ D[0];
NewCRC[1] = D[63] ^ D[61] ^ D[60] ^ D[57] ^
D[56] ^ D[55] ^ D[52] ^ D[51] ^ D[48] ^ D[46] ^ D[45] ^
D[44] ^ D[43] ^ D[41] ^ D[39] ^ D[36] ^ D[34] ^ D[32] ^
D[30] ^ D[29] ^ D[28] ^ D[24] ^ D[23] ^ D[22] ^ D[21] ^
D[20] ^ D[18] ^ D[17] ^ D[16] ^ D[15] ^ D[14] ^ D[13] ^
D[12] ^ D[9] ^ D[6] ^ D[1] ^ D[0];
NewCRC[2] = D[63] ^ D[62] ^ D[61] ^ D[60] ^
D[58] ^ D[57] ^ D[54] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
D[44] ^ D[43] ^ D[42] ^ D[39] ^ D[37] ^ D[34] ^ D[33] ^
D[29] ^ D[28] ^ D[25] ^ D[24] ^ D[22] ^ D[17] ^ D[15] ^
D[13] ^ D[12] ^ D[10] ^ D[8] ^ D[6] ^ D[2] ^ D[1] ^ D[0];
NewCRC[3] = D[63] ^ D[62] ^ D[61] ^ D[59] ^
```

```
D[58] ^ D[55] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^ D[45] ^
D[44] ^ D[43] ^ D[40] ^ D[38] ^ D[35] ^ D[34] ^ D[30] ^
D[29] ^ D[26] ^ D[25] ^ D[23] ^ D[18] ^ D[16] ^ D[14] ^
D[13] ^ D[11] ^ D[9] ^ D[7] ^ D[3] ^ D[2] ^ D[1];
NewCRC[4] = D[63] ^ D[62] ^ D[60] ^
D[59] ^ D[56] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^ D[46] ^
D[45] ^ D[44] ^ D[41] ^ D[39] ^ D[36] ^ D[35] ^ D[31] ^
D[30] ^ D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^ D[15] ^
D[14] ^ D[12] ^ D[10] ^ D[8] ^ D[4] ^ D[3] ^ D[2];
NewCRC[5] = D[63] ^ D[61] ^ D[60] ^
D[57] ^ D[53] ^ D[51] ^ D[50] ^ D[49] ^ D[47] ^ D[46] ^
D[45] ^ D[42] ^ D[40] ^ D[37] ^ D[36] ^ D[32] ^ D[31] ^
D[28] ^ D[27] ^ D[25] ^ D[20] ^ D[18] ^ D[16] ^ D[15] ^
D[13] ^ D[11] ^ D[9] ^ D[5] ^ D[4] ^ D[3];
NewCRC[6] = D[62] ^ D[61] ^ D[58] ^
D[54] ^ D[52] ^ D[51] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
D[43] ^ D[41] ^ D[38] ^ D[37] ^ D[33] ^ D[32] ^ D[29] ^
D[28] ^ D[26] ^ D[21] ^ D[19] ^ D[17] ^ D[16] ^ D[14] ^
D[12] ^ D[10] ^ D[6] ^ D[5] ^ D[4];
NewCRC[7] = D[63] ^ D[62] ^ D[59] ^
D[55] ^ D[53] ^ D[52] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^
D[44] ^ D[42] ^ D[39] ^ D[38] ^ D[34] ^ D[33] ^ D[30] ^
D[29] ^ D[27] ^ D[22] ^ D[20] ^ D[18] ^ D[17] ^ D[15] ^
D[13] ^ D[11] ^ D[7] ^ D[6] ^ D[5];

nextCRC8_D64 = NewCRC;
```

CRC Data Bit Mapping

The following figures show detailed bit mapping for x4, x8, and x16 devices. This bit mapping is common between WRITE and READ CRC operations.

Figure 162: x4 Devices

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7

Figure 163: x8 Devices

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7
DQ4	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ5	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ6	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ7	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7

Note: 1. The CRC of a x8 device is like that of two x4 devices, each nibble with identical CRC trees.

Figure 164: x16 Devices

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7
DQ4	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ5	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ6	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ7	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7
DQ8	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ9	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ10	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ11	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7
DQ12	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ13	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ14	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ15	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7

Note: 1. The CRC of a x16 device is like that of four x4 devices, each nibble with identical CRC trees.

Write CRC for x4, x8 and x16 Devices

The controller generates the CRC checksum and forms the write data frames.

For x8 devices, write CRC can be enabled or disabled independently per nibble. Two separate write CRC enable MR bits (for upper and lower nibbles) are defined. When at least one of two write CRC enable bits is set to 1, the timings of write CRC enable mode are applied to the entire device (both nibbles). When write CRC is enabled in one nibble and disabled in the other nibble in x8, the device does not check CRC errors on the disabled nibble; therefore, the ALERT_n signal and any internal status bit related to the CRC error is not impacted by the disabled nibble.

For x4 and x16 devices, only one of two write CRC enable bits is used, as defined in the mode register TBD table and notes. The unused write CRC enable bit is don't care (MR50:OP[2] is LOW).

The device checks for an error in received code words per each write CRC-enabled nibble by comparing the received checksum against the computed checksum. Errors are reported using the ALERT_n signal if there is a mismatch in any nibble.

The device can write data to the core without waiting for a CRC check for full writes. If bad data is written to the core, as identified by the CRC match and signaled on ALERT_n, the controller retries the transaction and overwrites the bad data. The host controller is responsible for data coherency.

When write CRC is enabled, there is no write latency adder.

Write CRC Auto-Disable

Write CRC auto-disable mode is enabled by programming the write CRC auto-disable mode enable bit MR50:OP[4] to 1.

When enabled, the device counts the number of write CRC error occurrences per device, regardless of configuration (x4, x8, and x16). When the number of write CRC errors occurring within the write CRC auto-disable window exceeds the write CRC auto-disable threshold (between 0 and 127) as programmed in MR51:OP[6:0], the device disables write CRC error checking of all nibbles and sets the write CRC auto-disable status bit MR50:OP[5] to 1. To exceed the write CRC auto-disable threshold, the number of write CRC errors must occur within the write CRC auto-disable window described below.

Unless the write CRC auto-disable status bit is set, the write CRC error counter is reset after the predetermined number of writes between 0 and 127, where 0 means an infinite window), as programmed in MR52:OP[6:0] so that the write CRC error count will accumulate during each write CRC auto-disable window. Once the write CRC auto-disable status bit is set, the write CRC error checking is not re-enabled at the end of the write CRC auto-disable window, even though the write CRC error counter is reset below the threshold value.

Write CRC error checking can be re-enabled by resetting the write CRC auto-disable status bit MR50:OP[5] to 0. This will reset the write CRC error counter and restart the write CRC auto-disable window

Prior to changing the write CRC auto-disable threshold as programmed in MR51:OP[6:0] or the write CRC auto-disable window as programmed in MR52:OP[6:0], the host disables the write CRC auto-disable mode (MR50:OP[4]=0). Once the updated values have been programmed in MR51 and/or MR52, write CRC auto-disable mode can be (re)enabled (MR50:OP[4]=1). Disabling the write CRC auto-disable mode, if enabled, resets the write CRC error counter and restarts the write CRC auto-disable window. However, if the write CRC auto-disable status bit had previously been set to 1 (MR50:OP[5]=1), the host is required to set MR50:OP[5]=0 to resume error counting.

Changes to the write CRC auto-disable threshold (MR51) and window (MR52) settings are only allowed when the CRC write auto-disable mode is disabled (MR50:OP[4]=0).

If the write CRC auto-disable threshold is reached and the device was driving ALERT_n LOW due to the current or a previous write CRC error, ALERT_n may be released upon satisfying CRC_ALERT_P-W_min.

When write CRC auto-disable mode is disabled (MR50:OP[4]=0), write CRC error counters may remain at reset values even if write CRC errors occur.

Read CRC for x4, x8 and x16 Devices

The device generates the read CRC checksum and forms the read data frames as shown in the CRC data bit mapping tables described above. The controller can check for an error in received code words per

nibble by comparing the received checksum against the computed checksum. If there is a mismatch in any of nibbles, the controller may retry the transaction.

Read latency adder when read CRC is enabled depends on data rate, as shown below.

Table 246: Read CRC Latency Addr

Data Rate (MT/s)	Read CRC Latency Adder (^{n}CK)
1980 MT/s ≤ Data Rate ≤ 2100 MT/s	0
2933 MT/s ≤ Data Rate ≤ 6000 MT/s	0
6000 MT/s < Data Rate ≤ 6400 MT/s	2

CRC Burst Order

When write CRC is enabled, the CRC bits are calculated based on the sequential burst address order of the write data for the WRITE command. This sequential order is '0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F' in BL16, and '0,1,2,3,4,5,6,7,T,T,T,T,T,T,T,T' or '8,9,A,B,C,D,E,F,T,T,T,T,T,T,T,T' in BC8 OTF.

When read CRC is enabled, the device's CRC generator overrides the CA burst order bits C3 and C2 to '00', and CRC bits are calculated based on the sequential burst address order of the read data for the READ command. This sequential order is '0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F' in BL16, and '0,1,2,3,4,5,6,7,T,T,T,T,T,T,T,T' or 'T,T,T,T,T,T,T,T,8,9,A,B,C,D,E,F' in BC8 OTF. The override values do not modify the actual data burst ordering, and are only used for the CRC calculations. Actual data burst follows the burst order as indicated by C3 and C2 in the READ command.

Write CRC Error Handling

When the device detects a CRC error on received code words in any nibble, it drives the ALERT_n signal to 0 for 12 to 20 clocks.

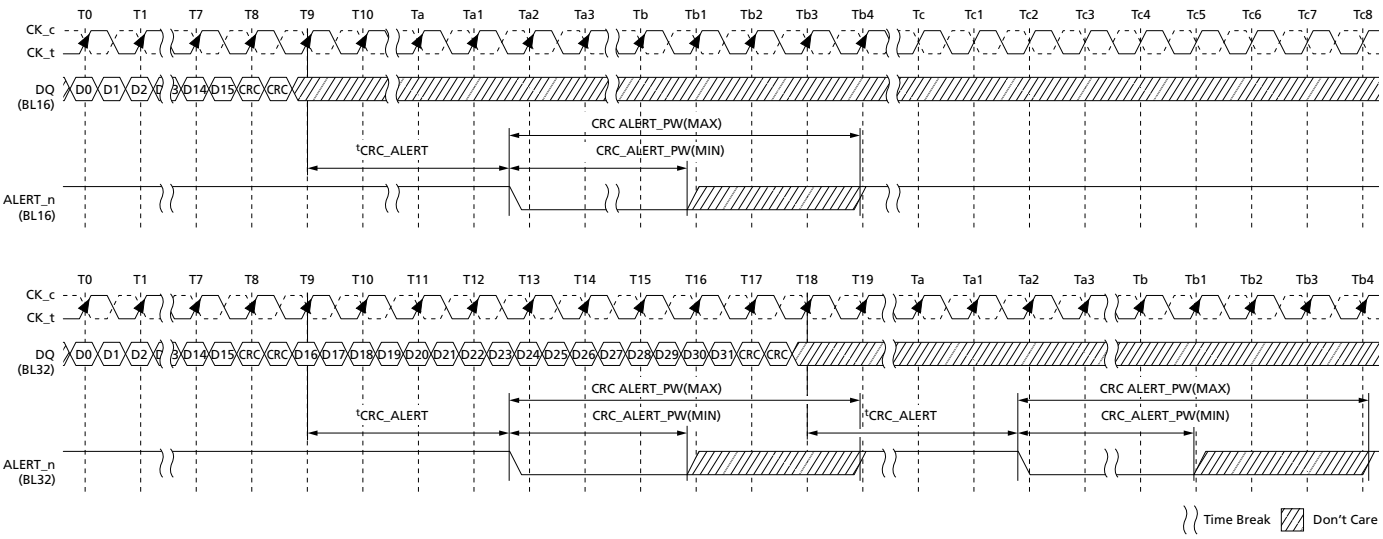
The latency-to-ALERT_n signal is defined as ^{t}CRC_ALERT in the figure below.

When a write CRC error is detected, the device sets the write CRC error status bit in MR50:OP[3] to 1. The write CRC error status bit remains 1 until the host clears it explicitly using an MRW command.

Upon seeing an error as a pulse width, the controller retries the write transactions. The controller understands the worst-case delay for ALERT_n (during initialization) and can backup the transactions accordingly, or the controller can be made more intelligent and try to correlate the write CRC error to a specific rank or a transaction. The controller is also responsible for opening any pages and ensuring that retrying of writes is done in a coherent fashion.

The pulse width may be seen longer than 20 clocks at the controller if there are multiple CRC errors, as the ALERT_n is a daisy chain bus.

Figure 165: CRC Error Reporting



Notes: 1. CRC ALERT_PW is specified from the point where the device starts to drive the signal LOW to the point where the device driver releases and the controller starts to pull the signal up.
2. Timing diagram applies to x4, x8, and x16 devices.

CRC Frame Format with BC8 OTF

CRC bits are always transferred on 17th and 18th UI in BC8 OTF mode. When read CRC is enabled during BC8 OTF read, DQ bits are driven HIGH and DQS is toggled by the device during the chopped data bursts. When write CRC is enabled during BC8 OTF write, DQ bits must be driven HIGH and DQS must be toggled by the controller during the chopped data bursts. In BC8 OTF mode, read CRC and write CRC bits are calculated with the inputs to the CRC engine for the chopped data bursts replaced by all 1s.

Figure 166: x4 Device CRC Bit Mapping in BC8 OTF Mode

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7

For a x4 device, the CRC tree input is 32 data bits as shown in the table above. The input for the remaining bits are 1.

CRC data bit mapping for x8 devices (BC8 OTF).

Figure 167: x8 Device CRC Bit Mapping in BC8 OTF Mode

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7
DQ4	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ5	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ6	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ7	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7

For a x8 device, the CRC tree inputs are two groups of 32 bits as shown in the table above. The inputs for the remaining bits are 1.

Figure 168: x16 Device CRC Bit Mapping in BC8 OTF Mode

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7
DQ4	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ5	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ6	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ7	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7
DQ8	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ9	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ10	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ11	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7
DQ12	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ13	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ14	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ15	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7

For a x16 device, the CRC tree inputs are four groups of 32 bits as shown in the table above. The inputs for the remaining bits are 1.

CRC Bit Mapping in BL32 Mode

In BL32 mode, CRC bits are calculated separately for the first and second halves of the data. CRC bits for the first half of data are transferred on 17th and 18th UI. CRC bits for the second half of data are transferred on the 35th and 36th UI.

ECC Transparency and Error Scrub

The ECC transparency and error scrub feature incorporates an ECC error check and scrub (ECS) mode with an error counting scheme for transparency. ECS mode enables the device to internally read data bits, correct single bit errors, and write back corrected data bits (scrub errors) to the array while providing transparency to error counts. ECS mode contains two options set via the mode register:

- Manual ECS mode (MR14:OP[7] = 1b): enables ECS operations via the multi-purpose command.
- Automatic ECS mode (MR14:OP[7] = 0b) (default): allows for an optional automatic ECS mode to run internally.

ECS is available on all device configurations.

ECS mode implements two counters to track ECC code word errors detected during operation: error counter (EC) and errors per row counter (EpRC).

EC defaults to counting rows with errors; however, it may also be configured to count code words with errors. In row mode (default), EC tracks the number of rows that have at least one code word error detected, subject to a threshold filter. In code word mode, EC tracks the total number of code word errors, also subject to the threshold filter. EpRC, tracks the error count of the row with the largest number of code word errors along with the address of that row. EpRC error reporting is also subject to a separate threshold filter.

A general functional block diagram example of the ECS Mode operation is shown in the figure below while the ECC Error Checking and Scrub mode, Mode Register (MR14), is shown in the following table below.

Figure 169: Functional Block Diagram Example: ECS Mode

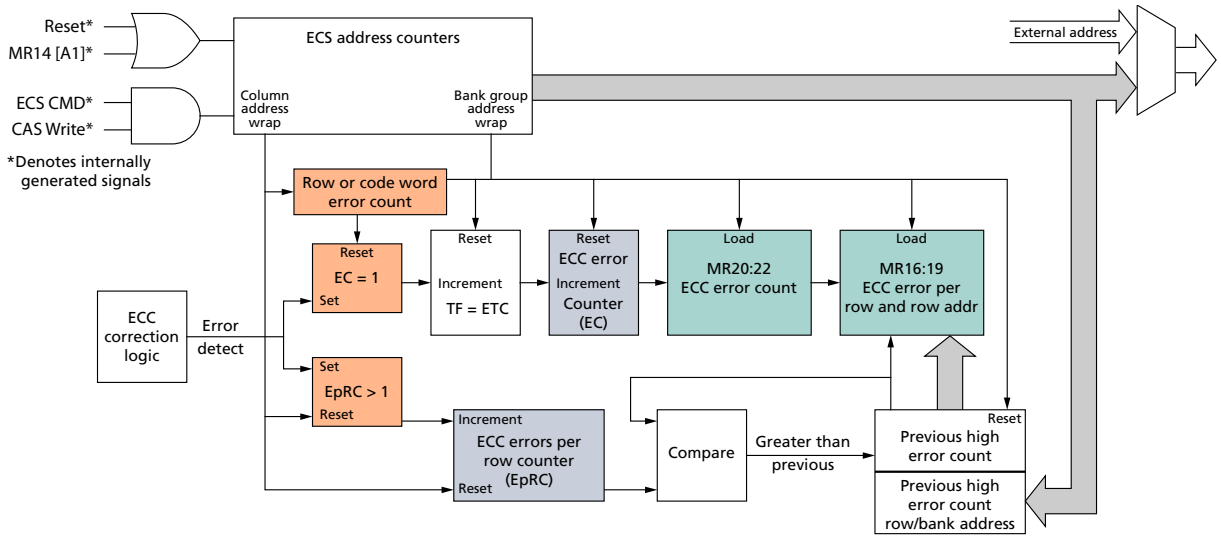


Table 247: Mode Register: ECS Mode

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
14	ECS mode	Reset ECS counters	Code-word/row count mode	RFU	CID3	CID2	CID1	CID0

Note: 1. CID[3:0] are used for 3DS devices only. For mono devices, set CID[3:0] to 0.

Mode Register and Device Initialization Prior to ECS Mode Operation

The ECC transparency and error scrub counters are set to zero. Internal ECS address counters are initialized by a RESET command or by manually writing MR14[6] = 1b. While MR14:OP[6] = 1b, ECS counters are reset and no additional ECS operations will occur. If a manual reset via mode register is utilized, MR14:OP[6] must be written back to 0 before any subsequent ECS operations will continue or a subsequent reset can be applied.

ECS mode selections, MR15:OP[3], automatic ECS in self refresh, MR14:OP[7], manual/automatic ECS mode, and MR14:OP[5], row/code word mode must be programmed during device initialization and must not be changed once the first ECS operation occurs, unless followed by issuing a RESET or ECS RESET COUNTERS; otherwise, an unknown operation could result during subsequent ECS operations.

An ECS RESET COUNTERS operation requires setting MR14:OP[6]=1b to reset MR16 - MR20. Setting MR14:OP[6]=0b is then required to re-enable manual or automatic ECS operations.

Manual ECS mode is enabled by MR14:OP[7] = 1b. A manual ECS operation requires an MPC command with OP[7:0]=0000 1100b.

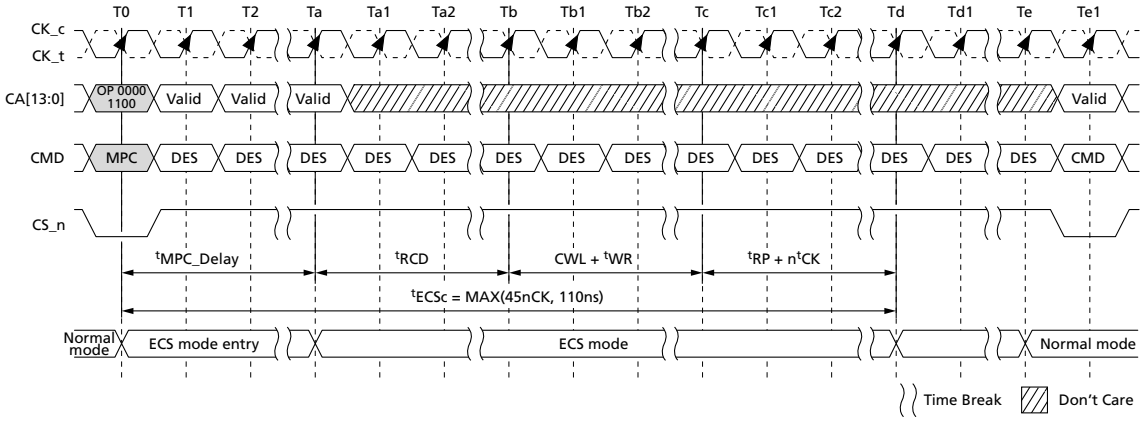
The device must have all array bits written to prior to executing ECS operation to avoid false failures.

ECS Operation

All banks must be precharged and in an idle state prior to executing a manual ECS operation.

Executing a manual ECS operation (MPC command with OP[7:0]=0000 1100b) generates the following internally self-timed command sequence: ACT--> RD --> WR --> PRE. ECS operation example timing shown in the figure below.

Figure 170: ECS Operation Timing Diagram



The minimum time for the ECS operation to execute is ^{t}ECSc (^{t}MPC_Delay + ^{t}RCD + CWL + ^{t}WR + ^{t}RP + ^{n}CK). ^{n}CK is required to satisfy ^{t}ECSc.

Upon execution of a manual ECS operation, DQs remain in RTT_PARK and DQS in DQS_RTT_PARK. The only commands allowed other than DES during ^{t}ECS for a manual ECS operation are ODT NT commands, which may change the DQ and DQS termination state. Any illegal usage of manual ECS mode (for example, refresh or temperature violations) results in operation not being guaranteed.

Executing a manual ECS operation using an MPC command with OP[7:0]=0000 1100b will issue an internally timed ACT command (row activation) based on the internal ECS address counters' row address, (^{t}MPC_Delay) after the MPC command. The ACT command should be followed by a WR

command ^{t}RCD later. The WR command performs an internal read-modify-write cycle on the code word determined by the internal ECS address counters' column address.

The internal read-modify-write cycle:

- Reads the entire code word (128 data bits and 8 check bits) from the array.
- Corrects a single bit error in the code word or check bits, if an error is detected.
- Writes the resultant code word back to the device array.

The WR command is followed by a PRE command CWL + ^{t}WR later. The PRE command automatically re-enables the device I/Os and address inputs, and it returns the device to idle mode (^{t}RP + ^{n}CK) after ^{t}ECSc is satisfied.

For each ECS operation, ECS address counters increment the column address after each internal ECS WR command, such that the next code word and check bits are selected. Once the column counter wraps (all code words and check bits on the row have been accessed), the row counter increments until all code words on each of the rows within a bank are accessed. When the row counter wraps (all rows within the bank have been accessed), the bank counter increments and the next bank within a bank group repeats the process of accessing each code word. When the bank counter wraps, the bank group counter increments and the next bank group repeats the process of accessing each code word, until all bank groups have been accessed.

After all the code words within the device are read, corrected and written once, the bank group counter wraps and the process begins again with the next manual ECS operation. The total number of manual ECS operations required to complete one cycle of error check and scrub is density and configuration dependent, as listed in the table below. The controller must track the number of manual ECS operations to complete a full scrub of the device.

Table 248: Number of Code Words Per Device

Configuration	8Gb	16Gb	24Gb	32Gb	64Gb
x4, x8, x16	2^26	2^27	2^27 * 1.5	2^28	2^29

To complete a full error check and scrub within the recommended 24 hours, the average periodic interval per ECS operation (^{t}ECSint) is 86,400 seconds divided by the total number of manual ECS operations to complete one full cycle of ECS. ^{t}ECSint is included in the following table.

Table 249: Average Periodic ECS Interval (^{t}ECSint)

Configuration	8Gb	16Gb	24Gb	32Gb	64Gb
x4, x8, x16	1.287ms	0.644ms	0.429ms	0.322ms	0.161ms

For the device to perform automatic ECS operations when in automatic ECS mode, the host needs to issue periodic REFab commands or periodically enter self refresh mode. The maximum spacing between REFab commands or self refresh entry for the device to complete the automatic scrub within the recommended 24 hours is ^{t}ECSint. Meeting this REFab/self refresh requirement enables the device to perform the automatic ECS operations without placing additional restrictions on refresh mode usage (i.e., all bank/same bank refresh or normal/FGR mode refresh) while in automatic ECS mode. REFab commands issued in excess of required by the device for automatic ECS operations (one per tECSint) may be used by the device for normal refresh operation. Issuing multiple REF commands shall not exceed the total number allowed within a 1 x ^{t}REFI window, as described in the Refresh Operation Scheduling Flexibility section of the spec.

When in automatic ECS mode, the ECS commands and timing are generated and satisfied internal to the device, following the average periodic ECS interval timings to ensure the error check and scrub is

completed and the transparency registers (MR16-20) are updated within the recommended 24 hour period.

The device is required to perform automatic ECS operations while in self refresh mode if automatic ECS is enabled by MR14 OP[7] = 0b or automatic ECS in self refresh is enabled by MR15 OP[3] = 1b to meet the average periodic ECS interval timings, regardless if self refresh is entered from manual or automatic ECS mode. However, some variation in the device scrubbing rate may be encountered while in self refresh since the device will need to sync the internal operations to an internal oscillator frequency. Entering and exiting self refresh does not reset the ECS transparency counters/registers. Interval timing for the maximum spacing between REFab commands or another self refresh entry is allowed to restart upon self refresh exit.

Writeback of Data During a x4 RMW and ECS Operation

The device may optionally support the suppressing of writeback for x4 devices and ECS writebacks, implementing the feature in MR9 or MR15. SPD specification indicates if the feature is supported and also whether to use MR9 or MR15 for enabling the modes. Micron devices define these bits in MR15, as shown in the table below. For complete details, see the Mode Registers section.

If MR15:OP[7]=1, x4 devices on writes perform an internal READ-MODIFY-WRITE operation for BL16. BL32 mode does not requires an internal READ-MODIFY-WRITE operation. The device corrects any single bit errors that result from the internal read of 128-bit data before merging the incoming 64-bit data and then re-computes 8 ECC check bits. Note that ECC check bits are computed after merging the incoming data with the corrected data from the array. The device then writes the incoming 64b data to the array along with the recomputed 8 ECC check bits. The device suppresses the writeback of 64-bit data that was fetched from the array irrespective of whether the 64-bit data needed any correction or not. Suppression of writeback (where applicable due to BC8 or DM usage) is not supported on x8/x16 devices; MR15:OP[7] must be set to 0b.

If MR15:OP[6]=1, the DRAM suppresses writeback of data and ECC check bits during ECS operation for x4, x8 and x16 devices. The device continues to count errors to provide transparency.

ECS Threshold Filter

The ECC transparency and error scrub scheme incorporates a user-programmable ECS threshold filter that masks error counts less than the programmed filter value. The value is set using MR15 as listed in the table below. The default MR15 setting is 256 fails per Gb of memory cells (OP[2:0]=011b).

Table 250: MR15 Transparency ECC Error Threshold Count per GB of Memory Cells and Automatic ECS in Self Refresh (For Reference Only)

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
15	x4 writes	ECS writeback	RFU		Automatic ECS in Self Refresh	OP[2:0]: 011b = 256 (default) OP[2:0]: 100b = 1024 OP[2:0]: 101b = 4096 OP[2:0]: 110b-110b = RFU		

Error Check and Scrub Error Tracking

The type of error tracking provided by the ECC transparency and error scrub is selectable using MR14:OP[5], which can track either the number of rows with errors (default) or code words with errors using the error counter. The row or code word error count is tracked and written to MR20. MR14:OP[5] is programmed during device initialization and should not be changed once the first ECS command is issued, otherwise an unknown operation could result. If MR14:OP[5] is changed without a power cycle

of the device, a MR14:OP[6]=1 reset must be issued prior to subsequent ECS commands to reinitialize the counters.

When the ECC row count mode is selected, the EC increments each time a row with check bit errors is detected. After all rows—in all banks, in all bank groups—have ECS operations performed, the result of the EC is loaded into MR20, subject to error threshold reporting. The EC is reset after the value has been transferred to the mode register.

MR20 is shown in the table below. EC[7:0] indicate error counts within a range. EC0 is set to 1 if EC0(min) (the ETC set by MR15) has been reached, but the fail count is less than or equal to EC0(max) = 2 * ETC * density(Gb) - 1. Likewise, the minimum values of EC[7:1] are defined as EC[x](min) = ETC * density(Gb) * 2^X, and maximum values are defined as EC[x](max) = 2 * (ETC * density(Gb) * 2^X) - 1. The exception is EC7(max), which is unlimited. The corresponding bit is set if the error count is within the required range.

Table 251: MR20 Number of Rows or Code Word Errors by Die (For Reference Only)

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
20	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

When the ECC code word error count mode is selected, the EC increments each time a code word with check bit errors is detected. After all code words—on all rows, in all banks, in all bank groups—have ECS commands performed, the result of the error counter is loaded into MR20, subject to error threshold reporting. The EC is reset after the value has been transferred to the mode register.

The ECC errors per row counter (EpRC) increments the number of code word errors on a given row after more than one error on a given row is detected. The EpRC counter resets with each column address wrap. Each row's code word error count is compared to the previous code word error count to determine the row address with the highest error count within the die. After reading all code words on a row, the number of errors counted is compared to the number of errors from the previous row. If the previous row error count is less than the present row error count, the present larger error count is saved to the previous high error count register, its associated address is saved to the previous high error count row/bank address/bank group register, and the present row error counter is cleared. If the previous row error count is greater than the present row error count, the previous row error count and register value remains unchanged; however, the present row error counter is cleared.

After all rows—in all banks, in all bank groups—have executed ECS operations, the result of the previous high error count (address and error count) are latched into MR16-19 when the bank group counter wraps, if the errors per row count (EPRC) meets or exceeds the row error threshold count (RETC) in the MR15 Transparency ECC Error Threshold Count per GB of Memory Cells and Automatic ECS in Self Refresh (For Reference Only table.

MR16-18 show in the table below contains the information for the row with the highest number of code word errors and is allocated as A[17:0] row address, BA[1:0] bank address, BG[2:0] bank group address. MR19 shown in the table below contains the information for the errors per row count (EpRC) for the number of code word errors on the highest failing row. REC[5:0] indicate error counts within a range. REC0 is set to 1 if REC0(min) (the RETC defined in the following table) has been reached, but the fail count is less than or equal to REC0(max) = 2 * RETC - 1. Likewise, the minimum values of REC[5:1] are defined as REC[x](min) = RETC * 2^X, and maximum values are defined as REC[x](max) = 2 * (RETC * 2^X)

- 1. The exception is REC5(max), which is unlimited. The corresponding bit is set if the error count is within the required range.

Table 252: MR16-19 Address of Row with Max Errors and Error Count (For Reference Only)

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
16	R7	R6	R5	R4	R3	R2	R1	R0
17	R15	R14	R13	R12	R11	R10	R9	R8
18	RFU	BG2	BG1	BG0	BA1	BA0	R17	R16
19	RFU	RFU	REC5	REC4	REC3	REC2	REC1	REC0

Table 253: Row Error Threshold Count (RETC)

	Error Count
Row Error Threshold Count (RETC)	4

The error counters (ECC error counter and ECC errors per row counter) reset each time the bank group counter wraps. This process occurs on the ECS operation following the ECS operation that processed the last row in the last bank in the last bank group. MR16-20 are not cleared after being read from; they retain the most recent written data until they are rewritten during a subsequent bank group wrap or reset by either issuing a RESET or ECS RESET COUNTERS command.

3DS Operation

The ECS feature supports 3DS stacking, where the chip ID and MR14:OP[3:0] (CID[3:0] respectively) command bits steer the ECS command to the proper mode registers (MR14-20) within the die stack. The CID[3:0] bits are ignored for MRW commands to MR14 or MR15, resulting in identical transparency settings for all die in a 3DS stack. The CID[3:0] bits must be set for MRR commands to MR14-20 to read out the data from the target die in the 3DS stack. The CID[3:0] bits are also used by the manual ECS MPC command. For single die packages, CID[3:0] should be set to 0.

Mode register configuration and readout of mode register data requires per DRAM addressing (PDA) mode.

Broadcasting the manual ECS MPC command to all die in the stack is not supported. The manual ECS MPC command-to-command spacing requires waiting ^{t}ECSc, even to different die in the stack. No other commands should be entered during ^{t}ECSc. The only commands allowed during ^{t}ECSc for a manual ECS operation are ODT_NT commands.

Refresh Management

Periods of high device activity may require additional REFRESH commands to protect data integrity. The requirement for additional REFRESH management (RFM) support is determined by the device; it will set the read-only MR58:OP[0] to show requirement:

MR58:OP[0] = 0 indicates no additional refresh is needed beyond the refresh requirement outlined in the REFRESH Operation section.

MR58:OP[0] = 1 indicates additional refresh management is required to ensure and protect data integrity, specific attempts to by-pass the on-die circuitry designed to protect data integrity may result in data disturb.

Table 254: Refresh Management Mode Register Definition

MR58:OP[0]	Refresh Management (RFM) Requirement
0	RFM not required
1	RFM required

A suggested implementation of refresh management by the controller monitors ACT commands issued per bank to the device. This activity can be monitored as a rolling accumulated ACT (RAA) count. Each ACT command increments the RAA count by 1 for the individual bank receiving the ACT command.

When the RAA counter reaches a vendor-specified initial management threshold (RAAIMT), which is set by the vendor in the read-only MR58:OP[4:1] bits (see table below), additional refresh management is needed. Executing the REFRESH MANAGEMENT (RFM) command allows additional time for the device to manage refresh internally. The RFM operation can be initiated to all banks with the REFRESH MANAGEMENT ALL (RFMab) command, or to a single bank address (BA[1:0]) in all bank groups with the REFRESH SAME BANK (RFMsb) command. A device with MR58:OP[0] = 0 treats the RFM command as a REF command.

Table 255: RAA Initial Management Threshold (RAAIMT) Mode Register Definition (For Reference Only)

MR58:OP[4:1]	RAAIMT Value	
	Normal Refresh Mode	FGR Refresh Mode
0000b-0011b	RFU	RFU
0100b	32	16
0101b	40	20
...	...	...
1001b	72	36
1010b	80	40
1011b-1111b	RFU	RFU

The RFM command bits are the same as the REF command, except for the state of CA9. If the refresh management required bit is 0 (MR58:OP[0] = 0), CA9 is only required to be valid (V) for a REF command, and then the device treats a RFM command as a REF command. If the refresh management required bit is 1 (MR58:OP[0] = 1), CA9 = H executes the REF command. Additionally, CA9 = L executes either an RFMab command if CA10 = L or an RFMsb command if CA10 = H.

The duration of the RFMab and RFMsb commands is dependent upon the device being in normal or FGR refresh mode. ^{t}RFM (MIN) is equivalent to ^{t}RFC (MIN). See the following table.

Table 256: ^{t}RFM Parameters

REFRESH MANAGEMENT Operation	Symbol	Value
NORMAL REFRESH MANAGEMENT (RFMab)	^{t}RFM1 (MIN)	^{t}RFC1 (MIN)
FINE GRANULARITY REFRESH MANAGEMENT (RFMab)	^{t}RFM2 (MIN)	^{t}RFC2 (MIN)
SAME BANK REFRESH MANAGEMENT (RFMsb)	^{t}RFMsb (MIN)	^{t}RFCsb (MIN)

When an RFM command is issued, the RAA counter in any bank receiving the command can be decremented by the RAAIMT value, down to a minimum RAA value of 0 (no negative or pull-in of RFM commands is allowed). Issuing an RFMab command enables the RAA count in all banks to be decremented by the RAAIMT value. Issuing an RFMsb command with BA[1:0] enables the RAA count only with that bank address across all bank groups to be decremented by the RAAIMT value

RFM commands are allowed to accumulate or postpone, but the RAA counter will never exceed a vendor-specified RAA maximum management threshold (RAAMMT), which is set by the vendor in the read-only MR58:OP[7:5] bits (see the following table). If the RAA counter reaches RAAMMT, no additional ACT commands are allowed until one or more REF or RFM commands have been issued to reduce the RAA counter below the maximum value.

Table 257: RAA Maximum Management Threshold (RAAMMT) Mode Register Definition (For Reference Only)

MR58:OP[7:5]	RAAMMT Value	
	Normal Refresh Mode	FGR Refresh Mode
000b-010b	RFU	RFU
011b	3x RAAIMT	6x RAAIMT
100b	4x RAAIMT	8x RAAIMT
101b	5x RAAIMT	10x RAAIMT
110b	6x RAAIMT	12x RAAIMT
111b	RFU	RFU

RFM command scheduling shall meet the same minimum separation requirements as those for the REF command (see the REFRESH Operation section). An RFM command does not replace the requirement for the controller to issue periodic REF commands to the device, nor does an RFM command affect internal refresh counters. The RFM commands are bonus time for the device to manage refresh internally. However, issuing an REF command also allows decrementing the RAA counter by the value set by MR59:OP[7:6], as shown in the table below. Hence, any periodic REF command issued enables the RAA counter of the banks being refreshed to be decremented by the MR59:OP[7:6] setting. Issuing an REFab command enables the RAA count in all banks to be decremented. Issuing an REFsb command with BA[1:0] enables the RAA count only with that bank address in all bank groups to be decremented.

Table 258: RAA Counter Decrement per REF Command Mode Register Definition

MR59:OP[7:6]	RAA Counter Decrement per REF Command
00b	RAAIMT
01b	RAAIMT* 0.5
10b	RFU
11b	RFU

No decrement to the RAA count values is allowed for entering/exiting self refresh. The per-bank count values before entering self refresh remain unchanged upon exit.

Adaptive Refresh Management (ARFM)

DDR5 supports an optional refresh management (RFM) mode called adaptive refresh management (ARFM). Because refresh management settings are read-only, adaptive RFM allows the controller flexibility to choose additional RFM threshold settings called RFM levels. The RFM levels permit alignment of the controller-issued RFM commands with the in-DRAM management of these commands. MR59:OP[5:4} enables selection of the adaptive RFM level, as shown in the following table.

Table 259: Mode Register Definition for Adaptive RFM Levels

MR59: OP[5:4]	RFM Level	RFM Requirement	RAAIMT Normal Refresh	RAAMMT Normal Refresh	RAA Decrement per REF Command	Notes
00b	Default	Default	Default	Default	Default	1,2
01b	Level A	RFM Required	RAAIMT-A	RAAMMT-A	RAADEC-A	1,2,3
10b	Level B	RFM Required	RAAIMT-B	RAAMMT-B	RAADEC-B	
11b	Level C	RFM Required	RAAIMT-C	RAAMMT-C	RAADEC-C	

Notes: 1. RAAIMT values for FGR are half of the normal refresh mode.
2. RAAMMT values for FGR are double that of the normal refresh mode.
3. RAAIMT, RAAMMT and RAADEC values for RFM levels A-C are set by the DRAM vendor.

Adaptive RFM mode inherits the RAA counting and decrement attributes of the standard RFM mode, while using the alternate RAAIMT, RAAMMT and RAADEC for the selected RFM level. Increasing the RFM level results in an increased need for RFM commands. Level C is the highest RFM level.

Setting MR59:OP[5:4] bits to something other than the default 00 enables the alternative RFM level for the adaptive RFM mode. The host decrements the rolling accumulated ACT (RAA) count to 0, either with RFM or pending REF commands, prior to making a change to the RFM level.

To inform the host of required RFM settings as the RFM level is changed by MR59:OP[5:4], the device modifies the corresponding mode register values for RAA required, RAAIMT, RAAMMT and RAADEC (MR58:OP[0], MR58:OP[4:1], MR58:OP[7:5], MR59:OP[7:6], respectively) for subsequent MRR commands. Mode register values that remain the same as the default settings indicate the default RFM threshold levels are supported at the selected ARFM level.

Adaptive RFM also allows a device shipped with RFM not required (MR58:OP[0]=0) to override that initial setting and enable RFM by programming a non-default RFM level. The device internally manages the change to treat the RFM command as an RFM command in this special override case, as shown in the table below. A device that supports ARFM, even if the device is shipped with RFM not required (MR58:OP[0]=0), sets MR58:OP[0] = 1 to indicate the chosen ARFM level is supported.

Table 260: RFM Commands Perceived by the Device

Command	MR58:OP[0]	MR59:OP[5:4]	Command Perceived by the Device	Notes
RFM	0b	00b	REF	1
RFM	0b	01b-11b	REF	
RFM	1b	00b	RFM	
RFM	1b	01b-11b	RFM	1,2

Notes: 1. If the optional ARFM (MR59:OP[5:4]=01b-11b) is not supported on the device, the command perceived by the device is determined by MR58:OP[0].
2. Adaptive RFM enables a device shipped with MR58:OP[0]=0 to override the initial setting and enable RFM by programming a non-default RFM level. The device changes MR58:OP[0]=1 to indicate the chosen ARFM level is supported.

Post Package Repair

Post package repair (PPR) enables a simple and easy method for repairing a failed row address. Two methods are provided: hard post package repair (hPPR) for a permanent row repair and soft post package repair (sPPR) for a temporary row repair. Additionally, DDR5 also optionally supports MBIST PPR (mPPR), which is used in conjunction with the MBIST feature to automatically repair failing addresses based on the results of MBIST.

Entry into hPPR, sPPR, MBIST and mPPR is protected through a sequential MRW guard key to prevent unintentional PPR programming. The sequential MRW guard key is the same for hPPR, sPPR, MBIST and mPPR.

The guard key requires a sequence of four MRW commands to be issued immediately after entering hPPR/sPPR/MBIST/mPPR, as shown in the figure below. The guard key sequence must be entered in the order specified in the table below. Any interruptions of the guard key sequence from other MRW/MRR commands or non-MR commands such as ACT, WR, or RD are not allowed. Although interruption of the guard key entry is not allowed, if the guard key is not entered in the required order, or if it is interrupted by other commands, hPPR/sPPR/MBIST/mPPR mode will not execute and the offending command that terminated the hPPR/sPPR/MBIST/mPPR entry may or may not execute correctly. However, the offending command does not cause device lock up. Offending commands that interrupt hPPR/sPPR/MBIST/mPPR include:

- Any interruptions of the guard key sequence from other MRW/MRR commands or non-MR commands
- MRW with CW = HIGH
- Two-cycle commands with CS_n LOW on the second cycle

Additionally, when the hPPR/sPPR/MBIST/mPPR entry sequence is interrupted, subsequent ACT and WR commands are conducted as normal commands. If an hPPR/sPPR/MBIST/mPPR operation is prematurely interrupted and/or terminated, the MR23:OP[1:0] must be reset to 0 prior to performing another hPPR/sPPR/MBIST/mPPR operation. The device does not provide an error indication if an incorrect hPPR/sPPR/MBIST/mPPR guard key sequence is entered.

Figure 171: Guard Key Timing Diagram

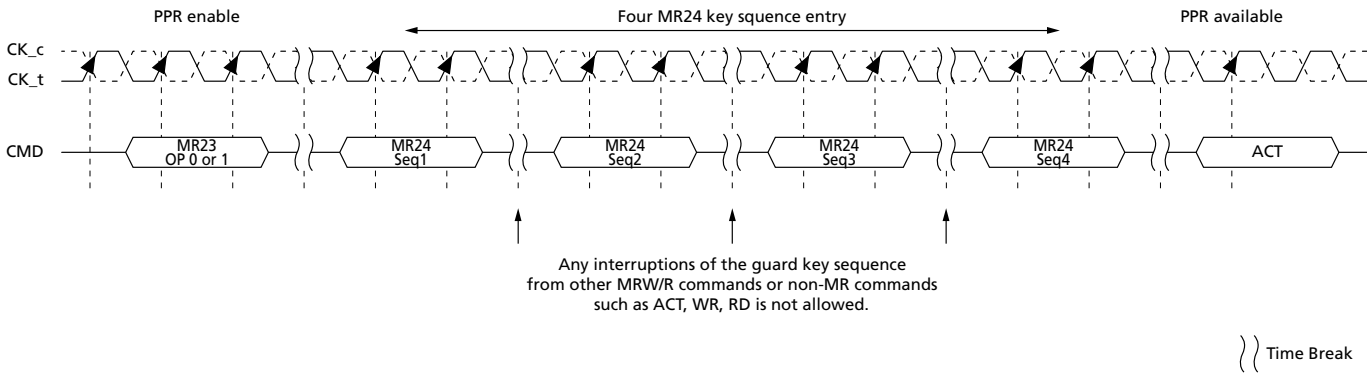


Table 261: hPPR vs. sPPR vs. mPPR

Condition	sPPR	hPPR	mPPR	Note
Persistence of repair	Volatile; repaired as long as V_{DD} is within operating range	Nonvolatile; repair is permanent after the repair cycle	Nonvolatile; repair is permanent after the repair cycle	Soft repairs are erased when V_{DD} is removed, device is reset, or sPPR UNDO command is performed to an unlocked sPPR row.
Length of time to complete repair cycle	CWL + 8*^{t}CK + ^{t}WR	^{t}PGM_hPPRa or ^{t}PGM_hPPRb	^{t}SELFREPAIR	
Number of repair elements per repair region[1]	1 per bank	At least 1 per bank	Vendor-specific	There is no ability to know how many mPPR elements remain in a given repair region. Host must rely on MBIST transparency in MR to determine mPPR success.
Simultaneous use of sPPR and hPPR within a repair region[1]	Previous hPPR are allowed before sPPR	Any outstanding sPPR must be cleared before a hPPR	Any outstanding sPPR must be cleared before MBIST or mPPR	
Repair sequence	1 method (WR)	1 method (WRA)	1 method (WRA)	
Device retains array data	Yes	No	No	sPPR data is not retained at the repaired row address. It must be copied or re-written.

Notes: 1. Repair region defined as the address space for which a single repair can be used. A repair region is either a BG or bank, depending on vendor implementation.

Table 262: Guard Key Encoding for MR24 (For Reference Only)

Guard Key	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
MR24 Seq1	1	1	0	0	1	1	1	1
MR24 Seq2	0	1	1	1	0	0	1	1
MR24 Seq3	1	0	1	1	1	0	1	1

Table 262: Guard Key Encoding for MR24 (For Reference Only) (Continued)

Guard Key	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
MR24 Seq4	0	0	1	1	1	0	1	1

Hard Post Package Repair

With hard PPR (hPPR), Micron's device can correct at least one row address per bank.

The hPPR resource designation (MR54,55,56,57) indicates hPPR resource availability, and it can be read or checked prior to implementing a repair.

IMPORTANT: hPPR repairs are permanent; the electrical-fuse cannot be switched back to an unfused state once it is programmed. The controller should prevent unintended hPPR mode entry and repair (for example, during the command/address training period).

Entry into hPPR is through a register enable; the ACT command is used to transmit the bank and row address of the row to be replaced. After ^{t}RCD time, a BL16 WRA command is used to select the individual device through the DQ bits and to transfer the repair address to the device. After program time and PREpb, hPPR mode must be exited so normal operation can resume.

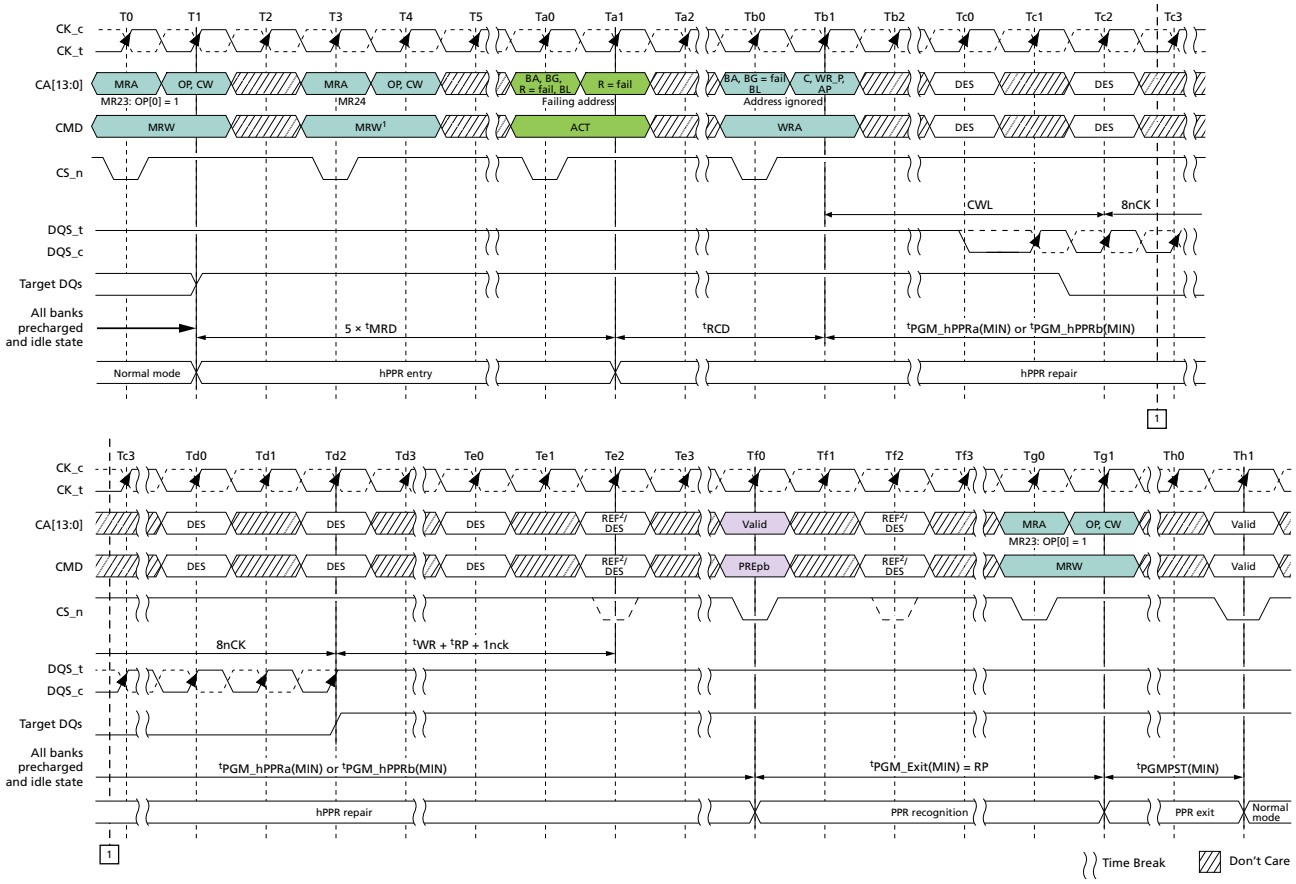
hPPR Fail Row Address Repair

1. Because the mode register address operand allows execution of the hPPR resource, MRR of hPPR resource designation (MR 54,55,56,57) must be read. After checking the hPPR resource availability of each bank from MRR, hPPR mode can be entered. If the MRR of hPPR resource designation (MR 54,55,56,57) is not available, the host controller should not issue hPPR mode.
2. Before entering hPPR mode, all banks must be precharged and in idle state, and CRC mode must be disabled.
3. Enable hPPR using MR23:OP[0] = 1 and wait ^{t}MRD
4. Issue the guard key as four consecutive MR24:OP[7:0] MRW commands, each with a unique address field OP[7:0]. Space each MRW command by ^{t}MRD.
5. Issue ACT command with the CID bits, bank group, bank and row fail address. Write data is used to select the individual device in the rank for repair. For non-3DS devices, the CID bits need only be valid and are ignored by the device.
6. After ^{t}RCD, issue WRA with a valid address. The device ignores the address given with the WRA command.
7. After CWL (CWL=CL-2), DQ[3:0] of the target device must be LOW for 8^{t}CK. If HIGH is driven to DQ[3:0] of a device for 8^{t}CK, the device does not conduct hPPR and retains data if the REFab/REFsb command is properly issued. If more than one device shares the same command bus, the devices not being repaired must have DQ[3:0] driven HIGH for 8^{t}CK. If all the DQ[3:0] data bits are neither all LOW nor all HIGH for 8^{t}CK, hPPR mode execution is unknown. For x8 and x16 devices, data bits other than DQ[3:0] are don't care. Note that a previous version of the spec required all DQs to be HIGH or LOW, but this was changed to DQ[3:0] to accommodate ECC UDIMMs and SODIMMs.
8. Wait ^{t}PGM_hPPRa or ^{t}PGM_hPPRb to allow repair at the target row address to occur internally, and then issue PREpb command.
9. Wait ^{t}PGM_Exit,min after the PREpb command to allow the device to recognize the repaired row address.
10. Exit hPPR by setting MR23:OP[0] = 0.
11. The device will accept any valid command after ^{t}PGMPST,min
12. In the case of multiple addresses to be repaired, repeat steps 3–10.

For a 3DS device the target die for the hPPR is selected by the CID[3:0] bits in the ACT, WRA and PRE commands. The CID bits must match in all three commands.

During hPPR mode, REFab/REFsb commands are allowed; however, array contents are not guaranteed. Upon receiving a REFab or REFsb command in hPPR mode, the device may ignore the refresh operation, but it will not disrupt the repair operation. Other commands except REFab/REFsb during ^{t}PGM can cause incomplete repair; therefore, no other commands except refreshes are allowed during ^{t}PGM. Once hPPR mode exits, with MR23:OP[0] = 0 and ^{t}PGMPST, confirm if the target row is repaired correctly by writing data into the target row and reading it back.

Figure 172: hPPR Fail Row Repair



Notes: 1. Allow REFab/REFsb from CWL+8^{t}CK+^{t}WR+^{t}RP+1^{t}CK after WR (does not guarantee array contents are refreshed during hPPR).
2. The timing diagram shows possible commands; however, not all shown can be issued at the same time. For example, if REF is issued at Te1, DES must be issued at Te2, as REF would be illegal at Te2. Likewise, DES must be issued ^{t}RFC prior to PREpb. All regular timings must still be satisfied.

Soft Post Package Repair

Soft post package repair (sPPR) is a way to quickly, but temporarily, repair one row address per bank (contrasted to hPPR, which takes longer and is a permanent repair of a row address.)

Some limitations and differences exist between an sPPR and an hPPR. Entry into sPPR is through a register enable; the ACT command is used to transmit the bank and row address of the row to be replaced. After ^{t}RCD, a BL16 WR command is used to select the individual devices through the DQ bits

and to transfer the repair address into an internal register in the device. After a write recovery time and PREpb command, sPPR mode must be exited and normal operation can resume.

Care must be taken to ensure refresh is not violated for the other rows in the array during the repair time. Also note that the device retains the soft repair information inside the device as long as V_{DD} remains within the operating region. If power is removed or the device is reset, the sPPR reverts to the unrepaired state. hPPR and sPPR may not be enabled at the same time. sPPR must be disabled, cleared and unlocked (if the device supports optional sPPR undo/lock) prior to entering hPPR, MBIST or mPPR mode.

With sPPR, Micron's device can repair one row address per bank. When the hPPR resources for a specific bank or bank group are used up, the specific bank or bank group has no more available resources for sPPR. If a repair sequence is issued to a a specific bank or bank group with no hPPR repair resource available, the device ignores the programming sequence.

Note that MR54-MR57 are NOT updated by an sPPR. The host controller must remember which sPPR resources have been updated since the last device reset.

The device may optionally support the sPPR UNDO and sPPR LOCK functions. The sPPR UNDO command undos a previous sPPR and causes the sPPR resource to be returned to its unused condition. The original row appears back in the memory map at its original location following an sPPR undo. The sPPR LOCK function locks the specific sPPR resource at its current location and does not allow another sPPR or an sPPR UNDO to be performed to that resource.

A row that has been replaced by a spare row does not need to be refreshed by the device. Likewise, a spare row that is not in the memory map — either from never being in the memory map or from an sPPR undo — does not need to be refreshed by the device. If moving a spare row in and out of the memory map, the host controller is responsible for sending enough ACTIVATE commands to any mapped out row to assure any required data retention. The host controller is also responsible for any data copy operations between the original row and spare row.

The host controller should read MR23:OP2 to determine whether the sPPR UNDO and sPPR LOCK functions are supported. 0=unsupported, 1=supported. The two features are supported together.

sPPR Fail Row Address Repair

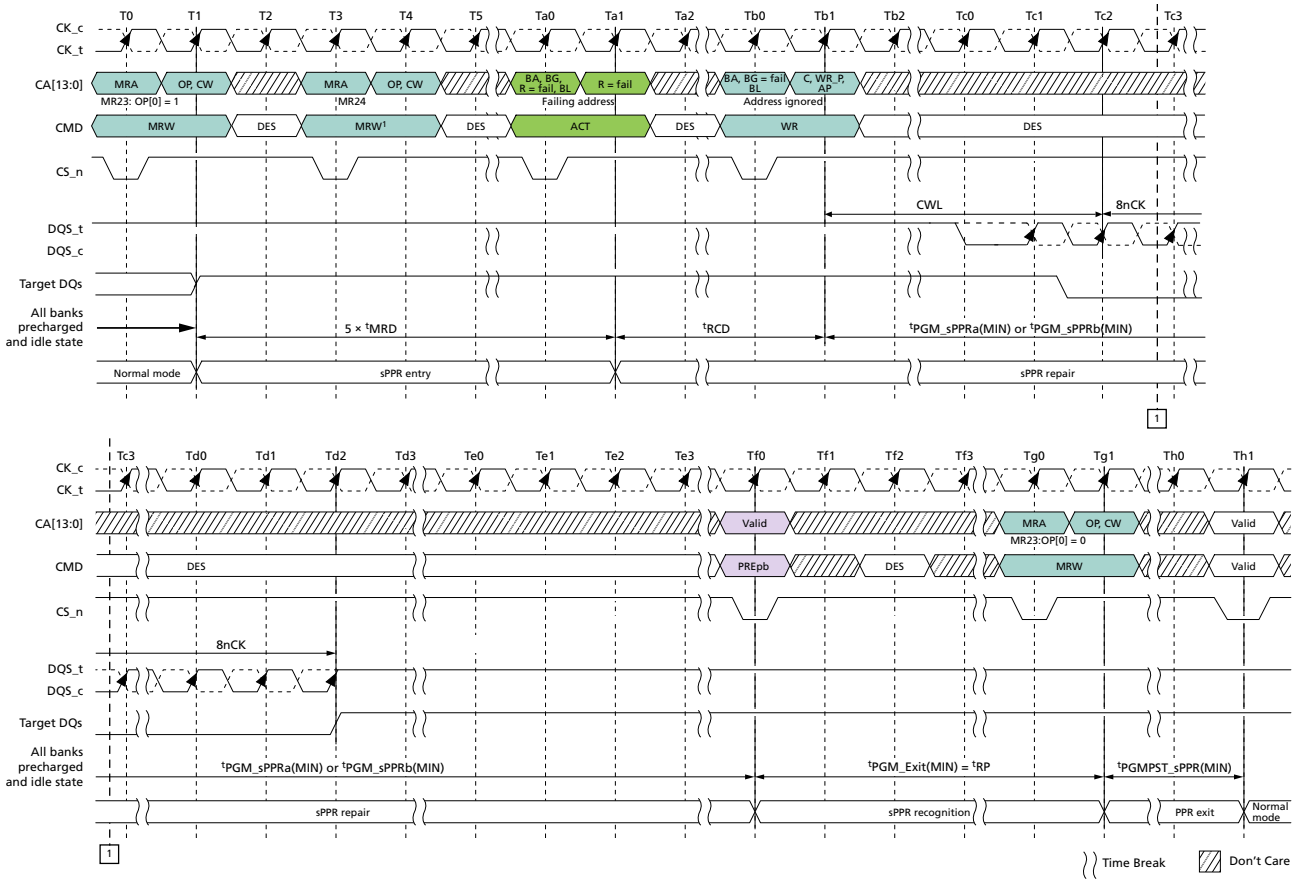
The following is the sPPR procedure with WR command. During this procedure, REFRESH commands are not allowed.

1. Back up the data of the target row address in the bank before executing sPPR. The back up data should be one row per bank. After sPPR completes, restore the data in the repaired array.
2. sPPR resources are shared with hPPR. The hPPR resource designation registers (MR54, 55, 56, 57) should be checked prior to sPPR. If the MRR of hPPR resource designation (MR54, 55, 56, 57) shows hPPR resources in the bank that is targeted for sPPR, the repair is not available. The host controller should not issue sPPR.
3. Before entering sPPR, all banks must be in a precharged and idle state, and CRC mode disabled.
4. Enable sPPR using MR23 bits OP[2:1] = 01 and wait ^{t}MRD.
5. Issue the guard key as four consecutive MRW commands, each with a unique address field OP[7:0]. Each MRW command must be spaced by ^{t}MRD. The guard key sequence is the same as hPPR.
6. Issue the ACT command with the CID bits, bank group, bank, and row fail address. Write data selects the individual device in the rank for repair. For non-3DS devices, the CID bits need only to be valid and are ignored by the device.
7. Issue a WR command after ^{t}RCD, with a valid column address. The device ignores the column address given with the WR command.
8. After CWL (CWL=CL-2), DQ[3:0] of the individual target device must be LOW for 8^{t}CK. If more than one device shares the same command bus, the devices that are not being repaired must have

DQ[3:0] driven HIGH for 8^{t}CK. If all of the DQ[3:0] data bits are neither all LOW nor all HIGH for 8^{t}CK, sPPR mode will be unknown. For x8 and x16 devices, data bits other than DQ[3:0] are don't cares. Note that a previous version of the spec required ALL DQs to be HIGH or LOW; this was changed to DQ[3:0] to accommodate ECC UDIMMs and SODIMMs.

9. Wait ^{t}PGM_sPPR,min for the internal repair register to be written, and then issue the PRE command to the bank.
10. Wait ^{t}RP after the PREpb command to allow the device to recognize the repaired row address.
11. Exit sPPR by setting MR23:OP[1] = 0 and waiting ^{t}MRD.
12. sPPR can be performed without affecting the previously performed hPPR provided a row is available in the repair region. When more than one sPPR request is made to the same repair region, the most recently issued sPPR address replaces the earlier issued one associated with the given bank and row addresses. In the case of conducting a soft repair address in a different bank group, repeat steps 4–11. During a soft repair, refresh commands are not allowed between sPPR MRS entry and exit.
13. For a 3DS device, the target die for the sPPR is selected by the CID[3:0] bits in the ACT, WR, and PRE commands. The CID bits must match in all three commands.

Figure 173: sPPR Fail Row Repair



sPPR UNDO

sPPR UNDO is a method of setting the sPPR resource back to its unused state, as it was following RESET. It follows the exact same protocol as the sPPR sequence, except with MR23 OP[2:1] set to 10.

The host controller must send the same CID bits, BG bits, bank bits, and row address in the ACTIVATE command as it did for the most recent sPPR completed in this repair region for this resource. The device may ignore the bank and row address bits if it so chooses, as the CID and BG bits may be enough to uniquely identify the sPPR resource depending on the number of repair elements. For non-3DS DRAMs, the CID bits need only be valid and are ignored by the device. If the bank and/or row address does not match that of the most recent sPPR to this resource, the device may or may not perform the undo. Any required copying of data is the host controller's responsibility.

Following an sPPR UNDO, a later sPPR may be done to assign the resource to a new or the same location. Data is retained in the sPPR resource, but it need not be refreshed by the device. If the host controller requires the data to remain valid, it must send enough ACT commands to the row while it is mapped in to guarantee the data.

This feature is optional. The sPPR UNDO function should only be done to devices in which MR23 bit 2 is read as a 1 upon an MRR.

sPPR LOCK

sPPR LOCK allows an sPPR resource to be locked in place. Locks are done to sPPR resources individually. Following an sPPR LOCK, any sPPR or sPPR UNDO is blocked to that spare resource. A hardware reset or power cycle must be done to undo the lock. The hardware reset or power cycle must also be done before any hPPR operation can be done if any sPPR resources are locked.

The sPPR LOCK uses the same protocol as the sPPR function except that MR23 OP[2:1] is set to 11. The ACTIVATE command must contain the CID bits, BG bits, bank bits and row address of the most recent sPPR for that resource. The device may ignore the bank and row address bits if it so chooses, as the CID and BG may be enough to uniquely identify the sPPR resource depending on the number of repair elements.

For non-3DS devices, the CID bits need only be valid and are ignored by the device. If the bank and/or row address does not match that of the most recent sPPR to this resource, the device may or may not perform the lock. This feature is optional. The sPPR lock function should only be done to devices in which MR23 bit 2 is read as a 1 upon an MRR.

Memory Built-in Self Test (MBIST)/Memory Built-in Self Test Post Package Repair (mPPR)

DDR5 devices can support the optional memory built-in self test (MBIST) and memory built-in self test-post package repair (mPPR) to help with hard failures such as single-bit or multi-bit failures in a single device so that weak cells can be scanned and repaired during the initialization phase. There are two distinct associated phases: MBIST (self-test phase) and mPPR (self-repair phase).

During MBIST, the DDR5 device uses vendor-specific patterns to test the memory array and detect hard failures. During mPPR, addresses of hard-failures are automatically repaired out. MBIST and mPPR may only be entered from the all banks Idle state. MBIST may be ran any time after the device has been properly initialized according to the Power-up Initialization Sequence section, but must be run prior to mPPR. After MBIST completes, MR22 transparency must be read. If transparency says that fails remain and the controller chooses to run mPPR, it must perform mPPR immediately after the device transparency is read.

mPPR resources are separated from normal hPPR/sPPR resources. mPPR resources are used for initial scan and repair, and hPPR/sPPR resources still must satisfy the number of repair elements as specified in the hPPR vs sPPR table. Once MBIST is done, the device updates the MBIST/mPPR transparency status in MR22:OP[2:0]. Detailed transparency status is described in mode register 22.

Two timings are associated with MBIST/mPPR: ^{t}SELFTEST and ^{t}SELFREPAIR. The time to test the array and detect failures is defined as ^{t}SELFTEST. The time to repair failures detected in the previous MBIST run using mPPR is defined as ^{t}SELFREPAIR. Multiple iterations of MBIST and mPPR may be required to repair all failures, and the transparency status will inform the host of this.

For 3DS devices, MBIST must be run on each logical rank in the 3DS package independently by configuring MR14:OP[3:0] prior to invoking MBIST. After MBIST is run on a single logical rank, MBIST/mPPR transparency in MR22 must subsequently be read to determine whether mPPR is needed on that logical rank. The controller may choose to run MBIST on all ranks before performing mPPR on all ranks sequentially, or it may perform MBIST on one rank followed by mPPR to the same rank, proceeding through each logical rank.

MBIST Sequence

The controller is required to issue an MRW command to enter the MBIST operation. The controller sets the MR23:OP[4] to HIGH, subsequently followed by the MR24 commands for the guard key, then the device enters MBIST operation and the device drives ALERT_n to LOW. Once the MBIST is complete, the device drives ALERT_n to HIGH to notify the controller that this operation is complete.

MBIST/mPPR transparency is updated in MR22, and signifies to the host whether mPPR must be performed to repair any found fails. If mPPR is required, the controller follows the mPPR sequence described in the mPPR Sequence section, and transparency is updated once mPPR is complete.

Device data is not guaranteed after MBIST PPR operation. During MBIST mode, only the DESELECT command is allowed. The DQ/DQS may either float (HI-Z) or perform RTT_PARK/DQS_RTT_PARK termination during ^{t}SELFTEST, depending on vendor-specific implementation, while CA/CS/CK ODT

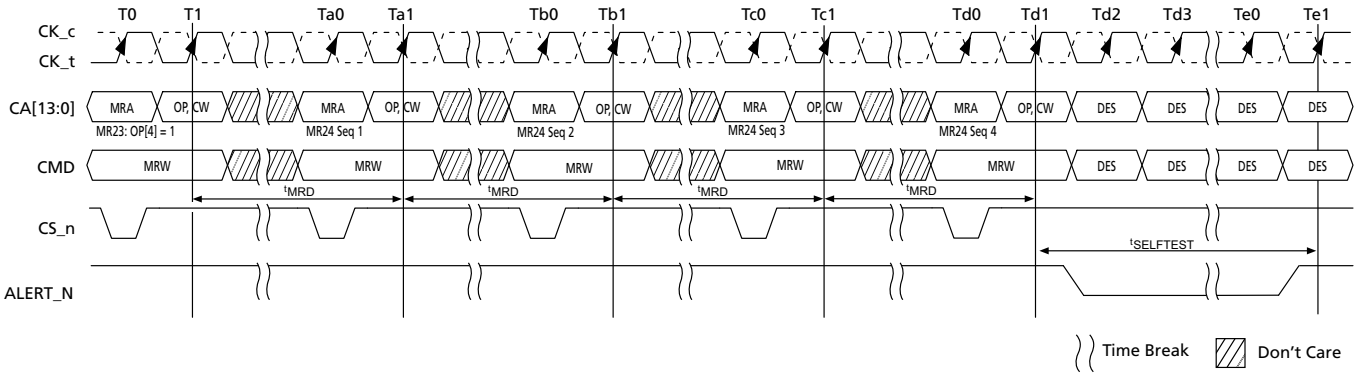
remains unchanged from it programmed state prior to MBIST. MBIST procedure is detailed in the MBIST Procedure table.

Table 263: MBIST Timing Parameter

Parameter	Density			MIN/MAX	Unit	Notes
	8Gb/16Gb	24Gb	32Gb			
tSELFTEST	9	14	19	MAX	S	1

Notes: 1. tSELFTEST applies per logical rank.

Figure 174: MBIST Procedure



mPPR Sequence

MBIST-PPR (mPPR) may be used after MBIST to repair failures found during the self-test phase. mPPR may only be performed after MR22 MBIST/mPPR transparency is read, and MR22 MBIST/mPPR transparency must be read after mPPR completes in order to determine if an additional mPPR or MBIST is required. If fails remain after the read of MR22 transparency, the mPPR sequence is described as follows:

1. All banks should be in a precharged and idle state, and CRC mode must be disabled prior to entering mPPR mode.
2. Enable mPPR using MR23:OP[3]=1 and wait tMRD.
3. Issue guard key sequence as four consecutive MR24:OP[7:0] MRW commands, each with a unique address field OP[7:0]. Each MRW command must be spaced by tMRD.
4. Issue the ACT command with a valid address. The device ignores the address given with the ACT command. Write data is used to select the individual DRAM in the rank for repair. For 3DS devices, CID on the ACT must be set to the same value programmed in MR14:OP[3:0], which determined the logical rank MBIST was last run on.
5. After tRCD, issue WRA with a valid address. The device ignores the address given with the WRA command. For 3DS devices, CID on the WRA must be set to the same value programmed in MR14:OP[3:0], which determined the logical rank MBIST was last run on.
6. After CWL (CL-2), DQ[3:0] of the individual target device must be LOW for 8tCK. Only devices that most recently have had an MR22 transparency result of 001b may be considered "target DRAMs". If more than one device shares the same command bus, devices that are not being repaired must have DQ[3:0] driven HIGH for 8tCK. If all of the DQ[3:0] data bits are neither all LOW nor all HIGH for

8tCK, the mPPR mode execution is unknown. For x8 and x16 devices, data bits other than DQ[3:0] are don't cares. Note: a previous version of the specification required all DQs to be HIGH or LOW; this was changed to DQ[3:0] to accommodate ECC UDIMMs and SODIMMs.

7. Wait tSELFREPAIR to allow the device to self repair the address(es) identified internally by MBIST, and then issue a PREab command.
8. Wait tPGM_exit after PREab command to allow the device to update MR22 transparency status.
9. Exit mPPR by setting MR23:OP[3]=0. Wait tPGMPST.
10. Read MR22 transparency status.
11. If additional fails remain, the controller may repeat steps 2-10. If no fails remain or the controller chooses not to perform additional mPPR, the device may continue to the next planned operation.

Figure 175: mPPR Row Repair Timing

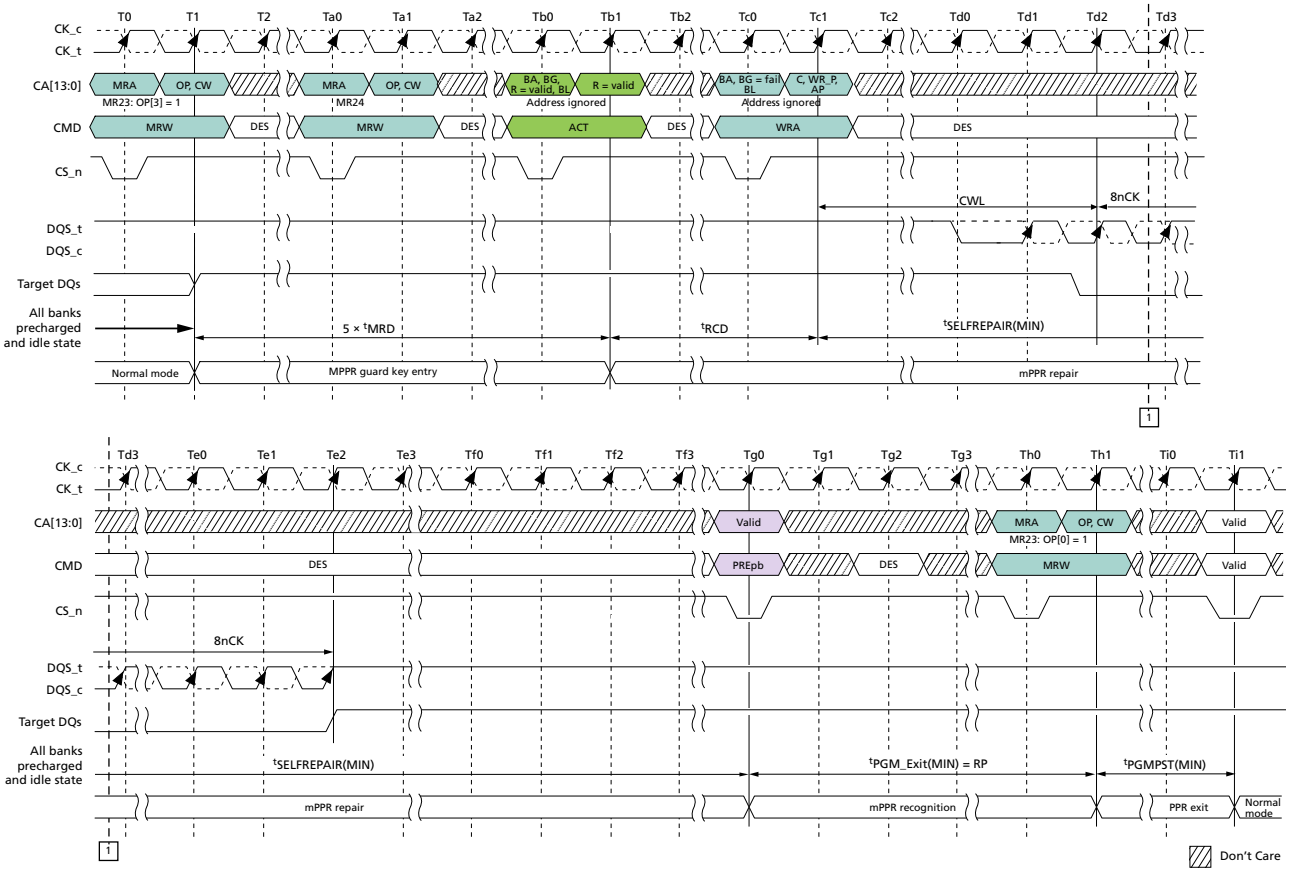
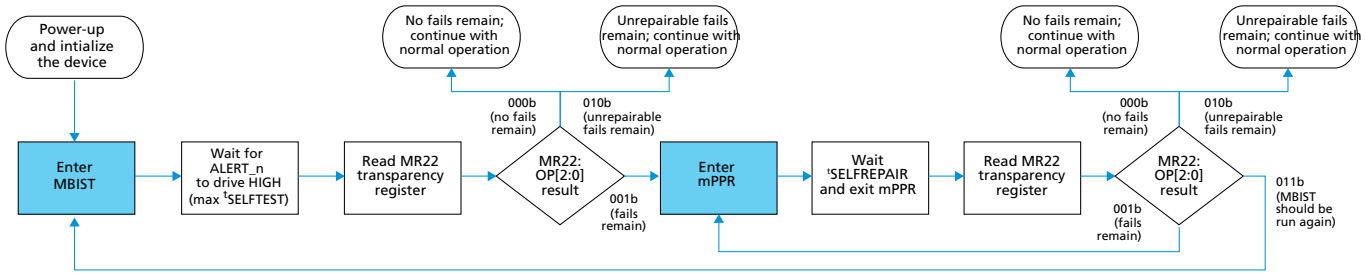


Table 264: mPPR Timings

Parameter	Symbol	3200-6400		6800-8800		Unit
		MIN	MAX	MIN	MAX	
mPPR programming time: x4,x8,x16	tSELFREPAIR	1000	-	TBD	-	ms

The figure below shows a detailed flow chart of the MBIST/mPPR sequence.

Figure 176: MBIST/mPPR Sequence



Notes: 1. mPPR may only be performed after an MR22:OP[2:0] transparency result of 001b.
2. 000b = **MBIST should be run again** indicates that fails were repaired with mPPR, but MBIST should be run again to load internal fail addresses for mPPR.
3. 011b = **Unrepairable fails remain** indicates there are not enough mPPR elements remaining to repair addresses latched during MBIST. It may be updated in MR22:OP[2:0] after either MBIST or mPPR, depending on vendor implementation.

DLL Modes

DLL Reset

DLL reset is performed via an MPC command. Any time the DLL RESET function is used, ^{t}DLLK must be met before functions requiring the DLL can be used, including READ, WRITE, MRR, RD-NT, WR-NT, and MRR-NT.

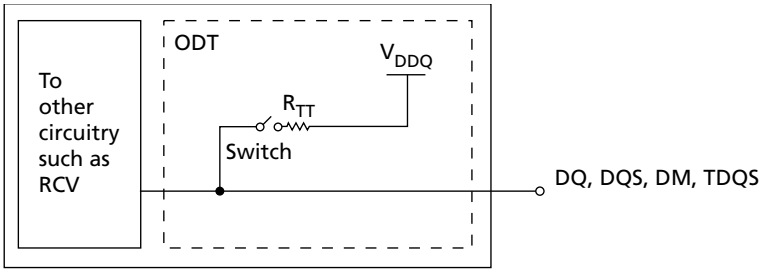
On-Die Termination

On-Die Termination for DQs

On-die termination (ODT) enables the DRAM to change termination resistance for each DQ. Unlike previous DDR technologies, DDR5 no longer has a physical ODT pin, and all ODT-based control is now command- and mode register-based. DQS_t, DQS_c and DM_n for x4 and x8 configurations (and TDQS_t, TDQS_c for x8 configuration), when enabled via READ/WRITE commands (for NT ODT usage) or default parking value with MR setting. For x16 configurations, ODT is applied to each DQU, DQL, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n and DML_n signal. The ODT feature is designed to improve signal integrity of the memory channel by allowing the device controller to independently change termination resistance for any or all devices. In addition to the control capability of the DQ ODT, the DQS ODT is now independently programmed via MPC and held static. All ODT control is targeted for the DQs. This addition allows for adjusting the delay common in an unmatched architecture. DQS RTT offset control mode is enabled via MR39:OP[2:0].

The ODT feature is turned off and not supported in self refresh mode, but does have an optional mode when the device is in power-down mode. The figure below shows a simple functional representation of the ODT feature.

Figure 177: Functional Representation of ODT



The switch is enabled by the internal ODT control logic, which uses command decode, mode register settings and other control information (see below). The value of RTT is determined by the settings of mode register bits.

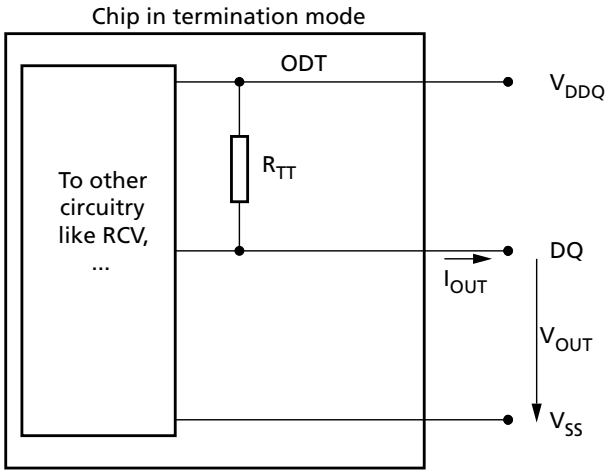
ODT effective resistance RTT is defined by MR bits.

ODT is applied to the DQ, DM_n, DQS_t/DQS_c and TDQS_t,/TDQS_c (x8 devices only) pins.

A functional representation is shown in the figure below.

$$RTT = \frac{V_{DDQ} - V_{OUT}}{|I_{OUT}|}$$

Figure 178: On Die Termination



Note: 1. Supported on die termination effective RTT values are: 240, 120, 80, 60, 48, 40, 34 ohms.

Table 265: ODT Electrical Characteristics R_{ZQ} = 240Ω +/- 1% Entire Temperature Range, After Proper ZQ Calibration

RTT	V_{OUT}	MIN	Nom	MAX	Unit	Notes
240Ω	V_{OLdc} = 0.5* V_{DDQ}	0.9	1	1.25	R_{ZQ}	1,2,3
	V_{OMdc} = 0.8* V_{DDQ}	0.9	1	1.1	R_{ZQ}	1,2,3
	V_{OHdc} = 1.1* V_{DDQ}	0.8	1	1.1	R_{ZQ}	1,2,3
120Ω	V_{OLdc} = 0.5* V_{DDQ}	0.9	1	1.25	$R_{ZQ}/2$	1,2,3
	V_{OMdc} = 0.8* V_{DDQ}	0.9	1	1.1	$R_{ZQ}/2$	1,2,3
	V_{OHdc} = 1.1* V_{DDQ}	0.8	1	1.1	$R_{ZQ}/2$	1,2,3
80Ω	V_{OLdc} = 0.5* V_{DDQ}	0.9	1	1.25	$R_{ZQ}/3$	1,2,3
	V_{OMdc} = 0.8* V_{DDQ}	0.9	1	1.1	$R_{ZQ}/3$	1,2,3
	V_{OHdc} = 1.1* V_{DDQ}	0.8	1	1.1	$R_{ZQ}/3$	1,2,3
60Ω	V_{OLdc} = 0.5* V_{DDQ}	0.9	1	1.25	$R_{ZQ}/4$	1,2,3
	V_{OMdc} = 0.8* V_{DDQ}	0.9	1	1.1	$R_{ZQ}/4$	1,2,3
	V_{OHdc} = 1.1* V_{DDQ}	0.8	1	1.1	$R_{ZQ}/4$	1,2,3
48Ω	V_{OLdc} = 0.5* V_{DDQ}	0.9	1	1.25	$R_{ZQ}/5$	1,2,3
	V_{OMdc} = 0.8* V_{DDQ}	0.9	1	1.1	$R_{ZQ}/5$	1,2,3
	V_{OHdc} = 1.1* V_{DDQ}	0.8	1	1.1	$R_{ZQ}/5$	1,2,3
40Ω	V_{OLdc} = 0.5* V_{DDQ}	0.9	1	1.25	$R_{ZQ}/6$	1,2,3
	V_{OMdc} = 0.8* V_{DDQ}	0.9	1	1.1	$R_{ZQ}/6$	1,2,3
	V_{OHdc} = 1.1* V_{DDQ}	0.8	1	1.1	$R_{ZQ}/6$	1,2,3

Table 265: ODT Electrical Characteristics R_{ZQ} = 240Ω +/- 1% Entire Temperature Range, After Proper ZQ Calibration

RTT	V_{OUT}	MIN	Nom	MAX	Unit	Notes
34Ω	V_{OLdc} = 0.5* V_{DDQ}	0.9	1	1.25	R_{ZQ}/7	1,2,3
	V_{OMdc} = 0.8* V_{DDQ}	0.9	1	1.1	R_{ZQ}/7	1,2,3
	V_{OHdc} = 1.1* V_{DDQ}	0.8	1	1.1	R_{ZQ}/7	1,2,3
DQ-DQ mis-match within byte	V_{OMdc} = 0.8* V_{DDQ}	0	–	8	%	1,2,4,5,6

Notes: 1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. Pull-up ODT resistors are recommended to be calibrated at 0.8*V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5*V_{DDQ} and 0.95*V_{DDQ}.
3. The tolerance limits are specified under the condition that V_{DDQ} = V_{DD} and V_{SS}.
4. DQ to DQ mismatch within byte variation for a given component including DQS_t and DQS_c (characterized).
5. RTT variance range ratio to RTT nominal value in a given component, including DQS_t and DQS_c.

$$\text{DQ-DQ mismatch in a byte} = \frac{R_{TT\_MAX} - R_{TT\_MIN}}{R_{TT\_NOM}} \times 100$$

6. This parameter of x16 device is specified for upper byte and lower byte.

ODT Modes, Timing Diagrams and State Table

ODT mode has five states: data termination disable, RTT_WR, RTT_NOM_RD, RTT_NOM_WR and RTT_PARK. ODT mode is enabled based on mode registers for each RTT listed below. In this case, the value of RTT is determined by the settings of those bits.

After entering self-refresh mode, the device automatically disables ODT termination and sets Hi-Z as termination state regardless of these setting.

Application: Controller can control each RTT condition with WR/RD command use of ODT offset control mode registers.

- RTT_WR: The rank that is being written to provides termination and adjusts timing based on the ODT control mode register settings.
- RTT_NOM_RD: The device turns this on if it sees CS asserted during the second pulse of the READ command (except when ODT is disabled by MR35:OP[5:3]).
- RTT_NOM_WR: The device turns this on if it sees a CS asserted during the second pulse of the WRITE command (except when ODT is disabled by MR35:OP[2:0]).
- RTT_PARK: The default parked value (set via MR34[2:0]) to be enabled when a READ or WRITE is not active.
- DQS_RTT_PARK: The default parked value (set for DQS via MR33:OP[5:3]); it is enabled when a READ or WRITE is not active.
- Data termination disable: The device driving data upon receiving a READ command; disables the termination after CL-1 and stays off for a duration of BL/2.
- Strobe termination disable: The device driving strobe upon receiving a READ command disables the termination after CL-1-^{t}RPRE and stays off for a duration of BL/2+^{t}RPST.

The RTT values have priority as follows:

1. Data termination disable and strobe termination disable
2. RTT_WR
3. RTT_NOM_RD
4. RTT_NOM_WR
5. RTT_PARK

This means if there is WRITE command, the device turns on RTT_WR (not RTT_NOM_WR or RTT_NOM_RD). Additionally, if there is READ command, the device disables data termination and enters driving mode. If during the second pulse of a READ or WRITE command the CS is held LOW, the NT ODT is enabled and the appropriate RTT_NOM_RD or RTT_NOM_WR is enabled for the non-target rank. This provides additional—and potentially different—term options for the other ranks on the channel.

Table 266: Termination State Table

Command	Mode Register Configuration Settings				Results		Notes
	RTT_PARK	RTT_WR	RTT_NOM_WR	RTT_NOM_RD	Target DRAM Term	Non-Target DRAM Term	
Any	Disabled				Hi-Z (ODT off)		3
Any non-term CMD	Enabled	Don't care			RTT_PARK	RTT_PARK	4
WR	Disabled			Don't care	Hi-Z (ODT off)	Hi-Z (ODT off)	
	Disabled		Enabled	Don't care	Hi-Z (ODT off)	RTT_NOM_WR	
	Disabled	Enabled	Disabled	Don't care	RTT_WR	Hi-Z (ODT off)	
	Don't care	Enabled		Don't care	RTT_WR	RTT_NOM_WR	2
	Enabled		Disabled	Don't care	RTT_WR	Hi-Z (ODT off)	2, 5
	Enabled	Disabled	Enabled	Don't care	RTT_PARK	RTT_NOM_WR	
	Enabled	Disabled		Don't care	RTT_PARK	Hi-Z (ODT off)	5
RD/MRR	Enabled	Don't care		Disabled	Hi-Z (ODT off)	Hi-Z (ODT off)	1, 5
	Don't care			Enabled	Hi-Z (ODT off)	RTT_NOM_RD	1

Notes: 1. When a READ command is executed, the termination state of the target rank is Hi-Z for defined period, independent of the MR setting of RTT_PARK / RTT_NOM_RD / RTT_NOM_WR.
2. If RTT_WR is enabled, RTT_WR is activated by a WRITE command for a defined period, independent of the MR setting of RTT_PARK / RTT_NOM_RD / RTT_NOM_WR.
3. If all RTT configurations are disabled, ODT receiver power is turned off to save power.
4. If RTT_PARK is enabled, RTT_PARK termination is enabled while WR / RD / MRR are not being executed.
5. When a non-target ODT command is executed and the RTT_NOM_WR or RTT_NOM_RD is disabled, the termination state of the non-target rank is Hi-Z for a defined period, independent of the MR setting of RTT_PARK.

Dynamic ODT

In certain application cases, and to further enhance signal integrity on the data bus, it is desirable that the device's termination strength can be changed without issuing an MRW command. This is supported by dynamic ODT mode, which is described as follows:

- Five RTT values are available: RTT_NOM_RD, RTT_NOM_WR, RTT_WR, RTT_PARK, and DQS_RTT_PARK.
  - The value for RTT_NOM_RD is preselected via MR35:OP[5:3]
  - The value for RTT_NOM_WR is preselected via MR35:OP[2:0]

  - The value for RTT_WR is preselected via MR34:OP[5:3]
  - The value for RTT_PARK is preselected via MR34:OP[2:0] - Programmed via MPC command
  - The value for DQS_RTT_PARK is preselected via MR33:OP[5:3] - programmed via MPC command

- During operation without commands, termination is controlled as follows;
  - Nominal termination strength for all types (RTT_NOM_RD, RTT_NOM_WR, RTT_WR, RTT_PARK, and DQS_RTT_PARK) are selected
  - RTT_NOM_RD and RTT_NOM_WR on/off timings are controlled via the respective NT READ and NT WRITE command and latencies
  - DQS_RTT_PARK is held static and is based on the value programmed in the MR listed above

- With a WRITE command, termination is controlled as follows:
  - A latency ODTLon_WR after the WRITE command, termination strength RTT_WR is selected
  - A latency ODTLoff_WR after the WRITE command termination strength RTT_WR is deselected

- The termination, RTT_NOM_WR, for the WRITE NT command is selected and de-selected by latencies ODTLon_WR_NT and ODTLoff_WR_NT, respectively
- When a READ command (RD) is registered, termination is controlled as follows:
  - A latency ODTLoff_RD after the READ command, data termination is disabled. Next, ODTLon_RD after the READ command, data termination is enabled.
  - A latency ODTLoff_RD_DQS after the READ command, strobe termination is disabled. ODTLon_RD_DQS after the READ command, strobe termination is enabled.

- The termination, RTT_NOM_RD, for the READ NT command is selected and de-selected by latencies ODTLon_RD_NT and ODTLoff_RD_NT, respectively.

The duration of a WRITE or READ command is a full burst cycle (BL/2). The termination select (ODTLon_...) and de-select (ODTL-off_...) latency settings do not result in an ODT pulse width which violates a burst cycle (BL/2) minimum duration. The equation ODTLoff_X - ODTLon_X >= BL/2 must be met, where X is the termination latency setting associated with a particular command type (WR, WR_NT, RD_NT).

To achieve the minimum write burst duration, ODTLoff_X and ODTLon_X latencies contain independent programmable mode register offsets:

- The values for the WRITE command ODT control offsets are preselected via MR37.
  - MR37:OP[2:0] preselects ODTLon_WR_Offset
  - MR37:OP[5:3] preselects ODTLoff_WR_Offset

- The values for the WRITE NT command ODT control offsets are preselected via MR38.
  - MR38:OP[2:0] preselects ODTLon_WR_NT_Offset
  - MR38:OP[5:3] preselects ODTLoff_WR_NT_Offset

- The values for the READ NT command ODT control offsets are preselected via MR39.
  - MR39:OP[2:0] preselects ODTLon_RD_NT_Offset
  - MR39:OP[5:3] preselects ODTLoff_RD_NT_Offset

The combination of allowable ODT offsets are shown in the table below.

Table 267: Allowable ODTL Offset Combinations

Setting		ODTLon_WR_Offset, ODTLon_WR_NT_Offset, ODTLon_RD_NT_Offset Setting						
		-4	-3	-2	-1	0	1	2
ODTLoff_WR_Offset, ODTLoff_WR_NT_Offset, ODTLoff_RD_NT_Offset	4	Valid	Valid	Valid	Valid	Valid	Valid	Valid
	3	Valid	Valid	Valid	Valid	Valid	Valid	Valid
	2	Valid	Valid	Valid	Valid	Valid	Valid	Valid
	1	Valid	Valid	Valid	Valid	Valid	Valid	Invalid
	0	Valid	Valid	Valid	Valid	Valid	Invalid	Invalid
	-1	Valid	Valid	Valid	Valid	Invalid	Invalid	Invalid
	-2	Valid	Valid	Valid	Invalid	Invalid	Invalid	Invalid

Notes: 1. The offset combinations apply to the ODTLon and ODTLoff independently for each command type (eg, ODTLon_WR_Offset and ODTLoff_WR_Offset are subject to these restrictions, but there are no restrictions on the setting of ODTLon_WR_Offset with respect to ODTLoff_WR_NT_Offset and ODTLoff_ RD_NT_Offset).
2. Although shown in the table, not all offset combinations may be valid for ODTL_WR, ODTL_WR_NT or ODTL_RD_NT. Reference MR37, MR38 or MR39, respectively, for valid offset settings.

See the table below for ODT latency and timing parameter details.

Table 268: Latencies and Timing Parameters Relevant for Dynamic ODT and CRC Disabled

Name and Description	Abbreviation	Defined From	Defined to	Speed Bins		Unit	Note
				3200-6400	6800-8800		
ODT Latency On from WRITE command to R_{TT} Enable	^{t}ODTLon_WR	Registering external WRITE command	Change R_{TT} strength from previous state to R_{TT_WR}	^{t}ODTLon_WR = CWL + ODTLon_WR_offset	TBD	nCK	1
ODT Latency On from WRITE NT command to R_{TT} Enable	^{t}ODTLon_WR_NT	Registering external WRITE command	Change R_{TT} strength from previous state to RTT_NOM_WR	^{t}ODTLon_WR_NT = CWL + ODTLon_WR_NT_offset	TBD		1
ODT Latency Off from WRITE command to R_{TT} Disable	^{t}ODTLoff_WR	Registering external WRITE command	Change RTT strength from RTT_WR to RTT_PARK/ RTT_NOM_RD/ RTT_NOM_WR/ Hi-Z	^{t}ODTLoff_WR = CWL + BL/2 + ODTLoff_WR_offset	TBD	nCK	1
ODT Latency Off from WRITE NT command to R_{TT} Disable	^{t}ODTLoff_WR_NT	Registering external WRITE command	Change R_{TT} strength from RTT_NOM_WR to RTT_PARK/ RTT_NOM_RD/RTT_WR/ Hi-Z	^{t}ODTLoff_WR_NT = CWL + BL/2 + ODTLoff_WR_NT_offset	TBD		1
Data Termination Disable	^{t}ODTLoff_RD	Registering external READ command	Disables termination upon driving data	^{t}ODTLoff_RD = CL - 1	TBD		2

Table 268: Latencies and Timing Parameters Relevant for Dynamic ODT and CRC Disabled

Name and Description	Abbreviation	Defined From	Defined to	Speed Bins		Unit	Note
				3200-6400	6800-8800		
Data Termination Enable	^{t}ODTLon_RD	Registering external READ command	Re-enables termination after driving data	^{t}ODTLon_RD = CL + BL/2	TBD		2
Strobe Termination Disable	^{t}ODTLoff_RD_DQS	Registering external READ command	Disables termination upon driving strobe	^{t}ODTLoff_RD_DQS = CL - 1 - ^{t}RPRE - (Read DQS Offset)	TBD		2
Strobe Termination Enable	^{t}ODTLon_RD_DQS	Registering external READ command	Re-enables termination after driving strobe	^{t}ODTLon_RD_DQS = CL + BL/2 + ^{t}RPST - 0.5 - (Read DQS Offset)	TBD		2
ODT Latency On from READ NT command to R_{TT} Enable	^{t}ODTLon_RD_NT	Registering external READ command	Change R_{TT} strength from previous state to RTT_NOM_RD	^{t}ODTLon_RD_NT = CL + ODTLon_RD_NT_offset	TBD	nCK	1
ODT Latency Off from READ NT command to R_{TT} Disable	^{t}ODTLoff_RD_NT	Registering external READ command	Change R_{TT} strength from RTT_NOM_RD to RTT_PARK/ RTT_NOM_WR/RTT_WR/ HIZ	^{t}ODTLoff_RD_NT = CL + BL/2 + ODTLoff_RD_NT_offset	TBD		1
R_{TT} change skew	^{t}ADC	Transitioning from one R_{TT} state to the next R_{TT} state	R_{TT} valid	^{t}ADC,min = 0.2 ^{t}ADC,max = 0.8	TBD	^{t}CK(avg)	3

Notes: 1. All _offset parameters refer to the ODT Configuration mode registers settings in MR37-MR39.
2. For simplicity, READS are assigned the same type of timing parameter; however, unlike others, it is a fixed timing and does not have an offset mode register to control it. To indicate this, it was named Data (or Strobe) termination Disable and Enable.
3. When transitioning from a value of R_{TT} equal to RA, to a value of R_{TT} equal to RB, the R_{TT} termination resistance during the transition must be constrained from the minimum of (RA,RB) to the maximum of (RA,RB).

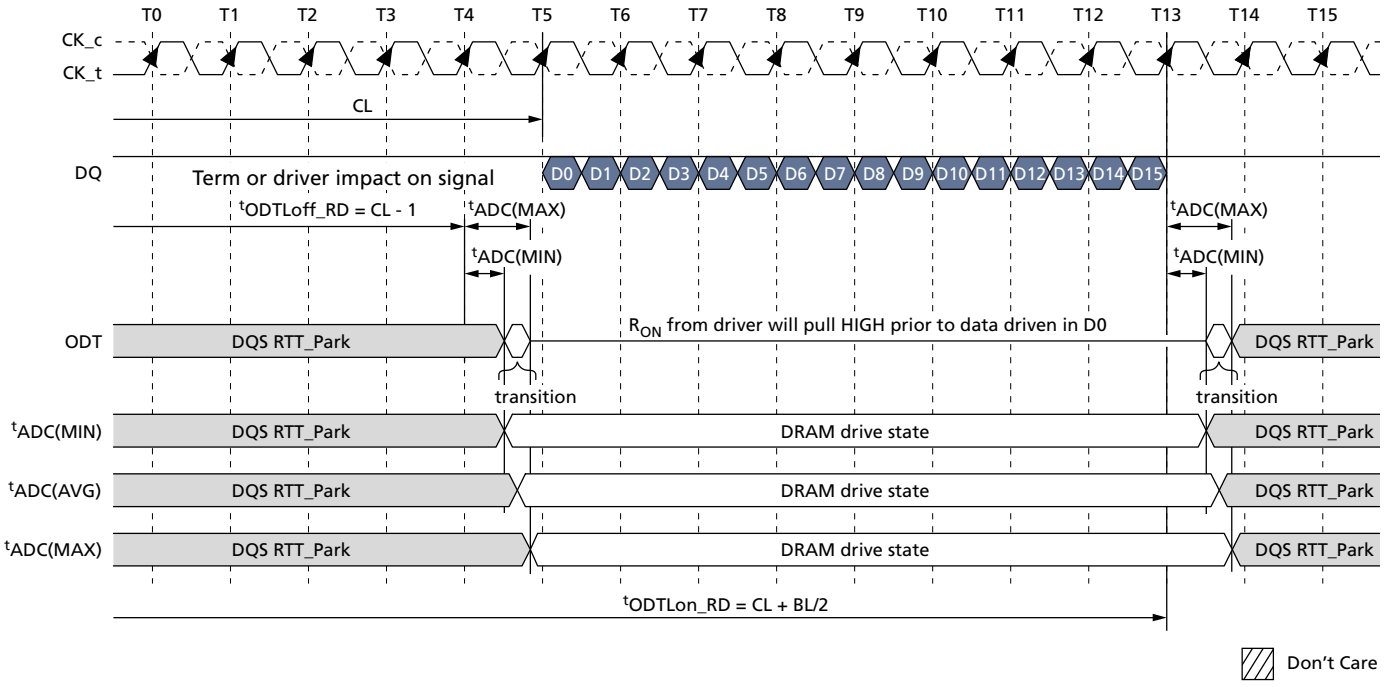
ODT ^{t}ADC Clarifications

^{t}ADC is defined as the time it takes for the device to transition from one RTT state to the next RTT state. In the case of a READ command, it is the time from the current RTT state to the device drive state.

Unless the RTT is specifically disabled, no HIGH-Z state is allowed during ^{t}ADC. During the device drive state, the RON will keep the DQ signal HIGH prior to the first DQ transition. The DFE should assume that 4UI prior to D0 the signal is HIGH.

Below is an example showing the ^{t}ADC (MIN), ^{t}ADC (AVG) and ^{t}ADC (MAX) with respect to the RTT status and effects on the DQ lines prior to the burst.

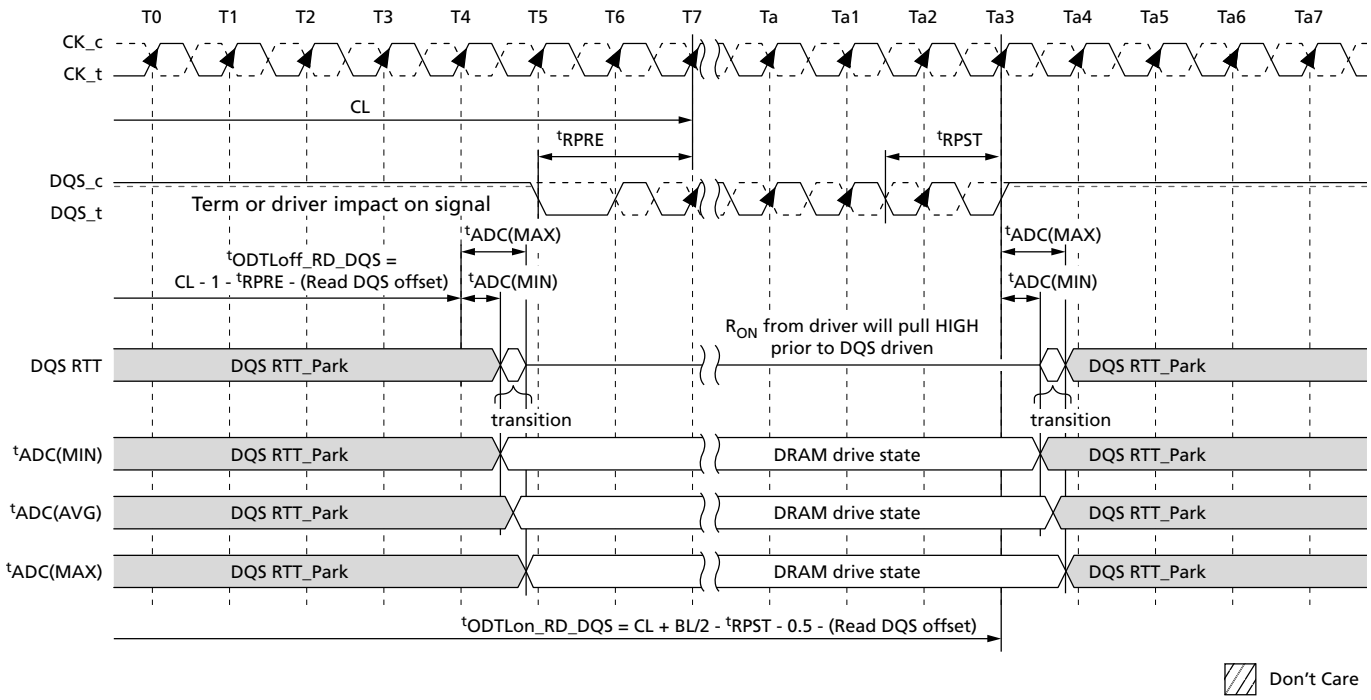
Figure 179: tADC Clarification - Example 1 DQ RTT Park to Read



Notes: 1. The diagram shows a transition from RTT_PARK to READ command enabled drive state. When tADC transitions from RTT to drive state, the R_{ON} from the driver will keep the DQ signal HIGH prior to the data driven in D0. No HIGH-Z time during tADC is allowed in this example.
2. In the case of term to WRITE, the host keeps the DQ signal HIGH 4UI prior to the data driven in D0.
3. The DFE should assume that 4UI prior to D0 the signal is HIGH.

Below is an example showing the tADC (MIN), tADC (AVG) and tADC (MAX) with respect to the RTT status and effects on the DQS lines prior to the burst.

Figure 180: tADC Clarification - Example 1 DQS RTT Park to Read



Note: 1. The diagram shows a transition from DQS_RTT_PARK to READ command enabled drive state. When tADC transitions from RTT to READ command enabled drive state, the RON from the driver keeps the DQS signal HIGH prior to the DQS driven at t5. No HIGH-Z time during tADC is allowed in this example.

ODT Timing Diagrams

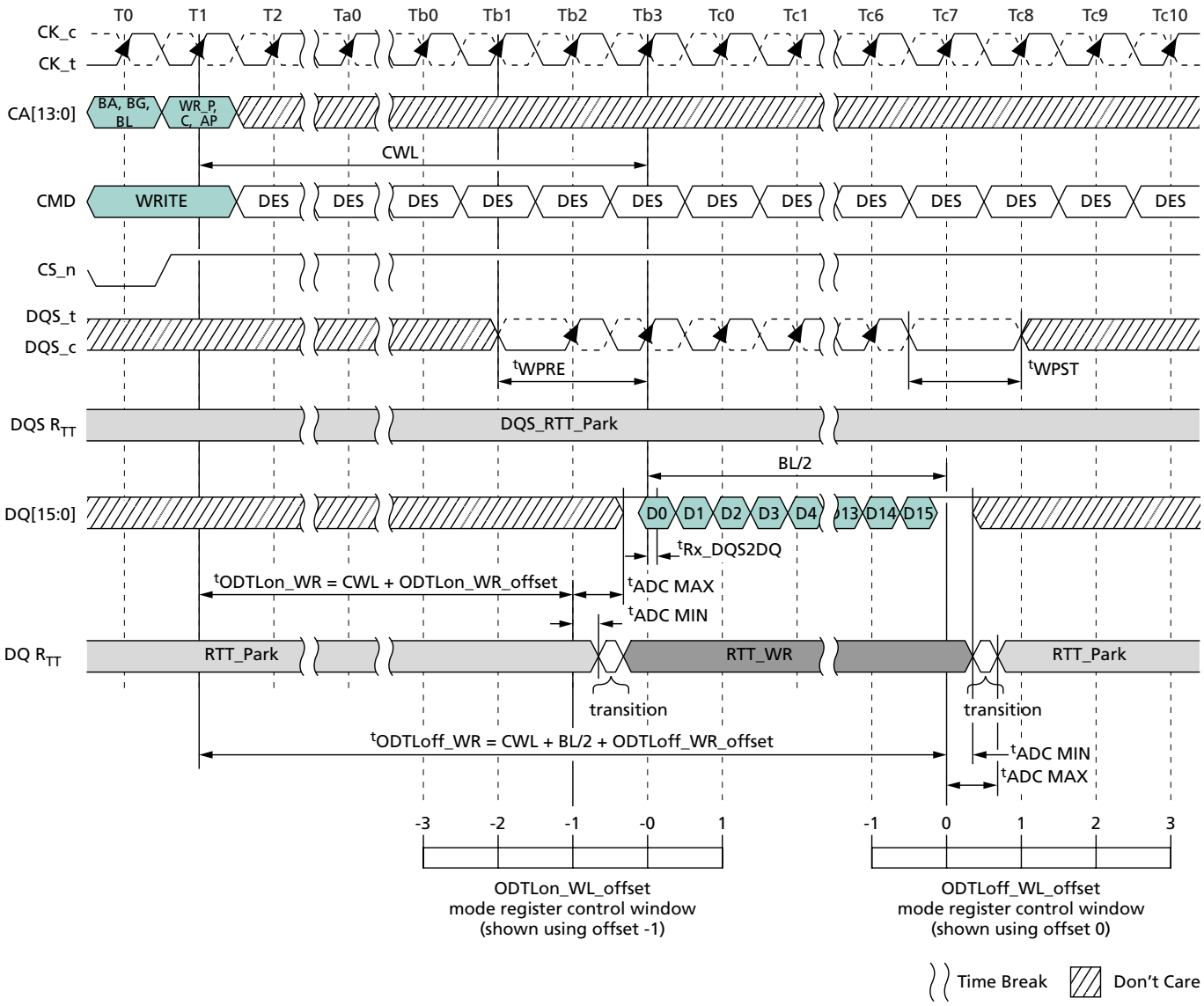
This section provides examples of ODT utilization timing diagrams. Examples of WRITE to WRITE, READ to WRITE and READ to READ are provided for clarification only. Implementations may vary, including termination on other DIMMS.

It is the controller's responsibility to manage command spacing and the programmable aspect of tODLon/off times to ensure that preambles and postambles are included in the RTT ON time.

When a 1 tCK ODT control gap for any ODT operation exists (such as shown in the WRITE (BL16) to WRITE (BL16), Different Bank, 2tCK Gap figure), the gap's RTT value is the same or smaller (weaker termination) than RTT_PARK.

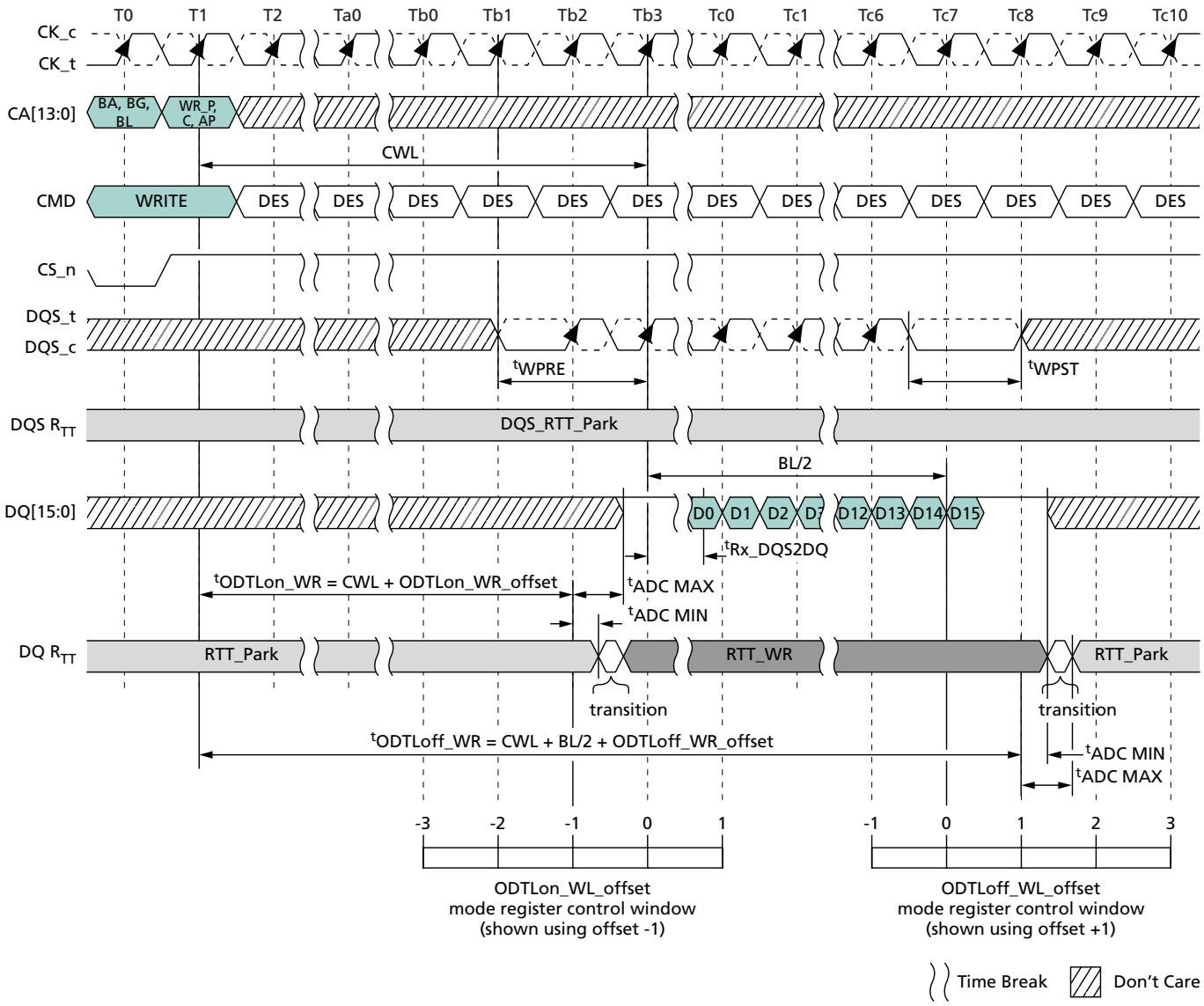
All timings noted in the following figures are for reference only.

Figure 181: Example 1 — Burst WRITE Operation ODT Latencies and Control Diagrams



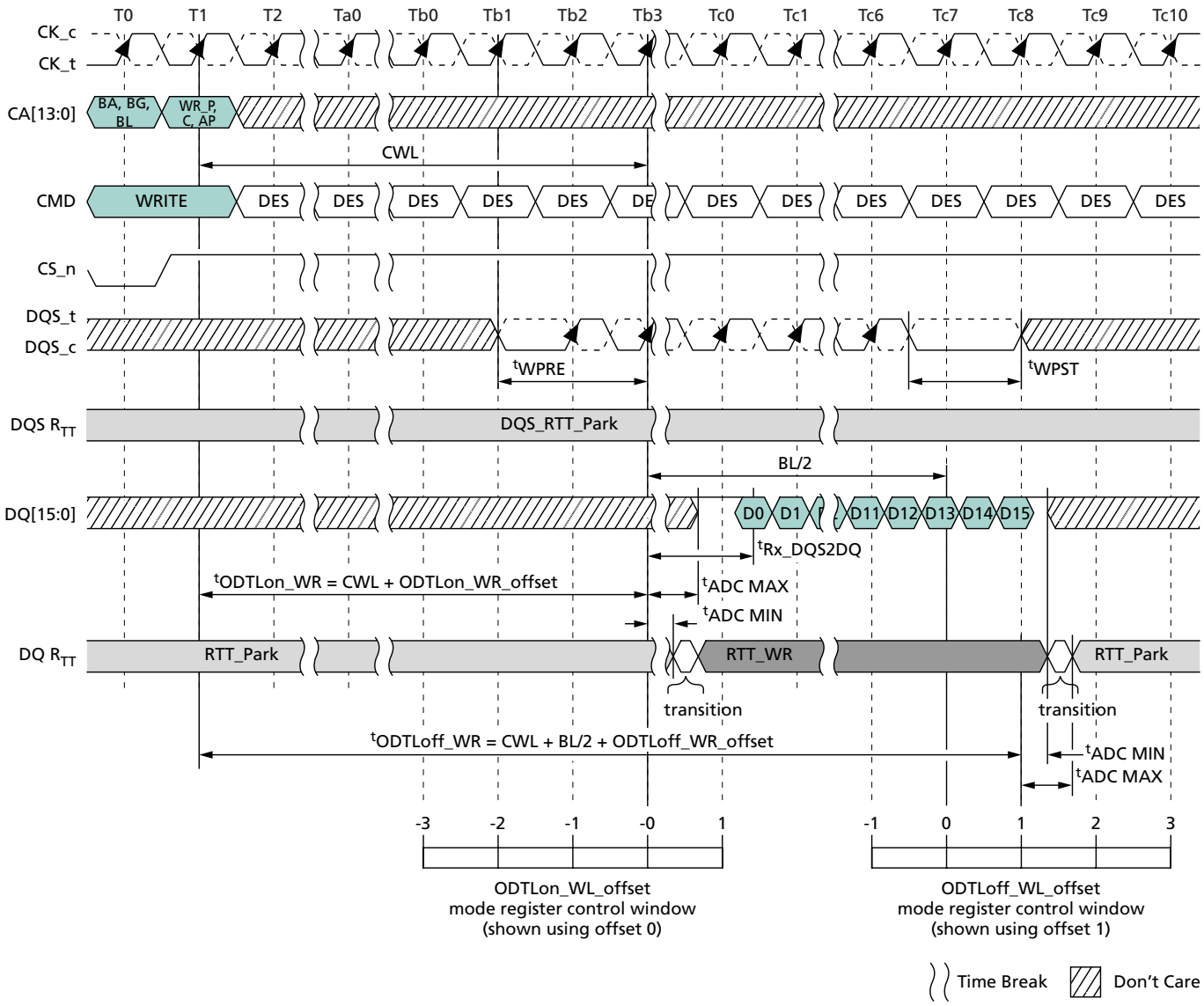
Notes: 1. For simplicity, the entire range of ODTL control is not shown.
2. Example details - 2tCK tWPRE, 1.5tCK tWPST, 0.5UI tRX_DQS2DQ, ODTLon_WL_offset configured for -1. ODTLoff_WL_offset configured for 0. Example shows how the host may aggressively adjust the offset of the tODTLon_WR timing to give tADC the minimum time to settle before data.
3. System designs and margins may vary requiring larger RTT_WR windows.

Figure 182: Example 2 — Burst WRITE Operation ODT Latencies and Control Diagrams



Notes: 1. For simplicity, the entire range of ODTL control is not shown.
2. Example details - 2tCK tWPRE, 1.5tCK tWPST, 1.5UI tRX_DQS2DQ, ODTLon_WL_offset configured for -1. ODTLoff_WL_offset configured for +1. Example shows how the host may want to add an offset to the tODTLoff_WR time so that RTT_WR stays on for the actual burst.
3. System designs and margins may vary requiring larger RTT_WR windows.

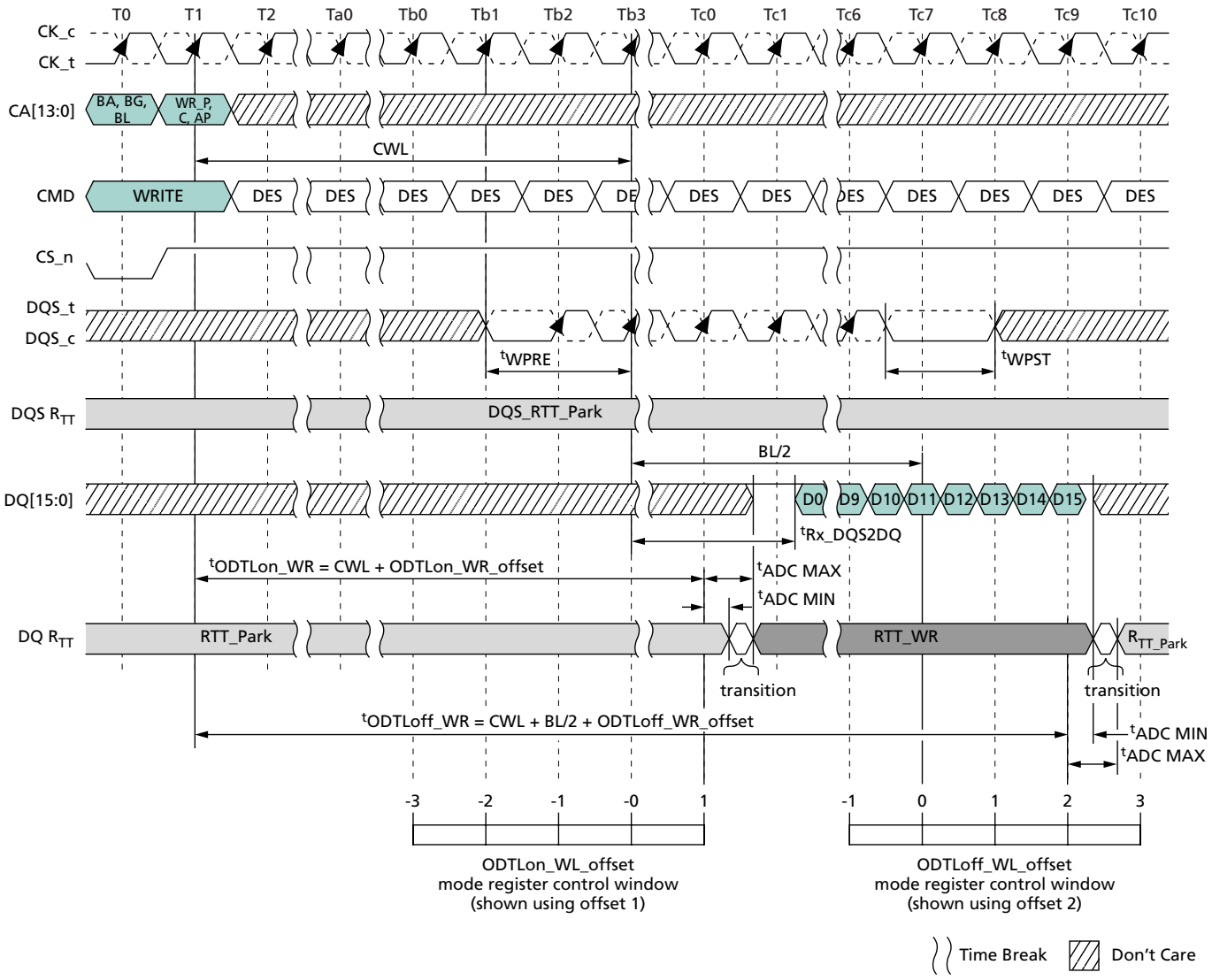
Figure 183: Example 3 — Burst WRITE Operation ODT Latencies and Control Diagrams



Notes: 1. For simplicity, the entire range of ODTL control is not shown.

2. Example details - 2^{t}CK ^{t}WPRE, 1.5^{t}CK ^{t}WPST, 3UI ^{t}RX_DQS2DQ, ODTLon_WL_offset configured for 0. ODTL-off_WL_offset configured for +1. Example shows how the host could leave the RTT_WR ON time to default values with no offset and may want to add an offset to the ^{t}ODTLoff_WR time so that RTT_WR remains ON for the actual burst.
3. System designs and margins may vary requiring larger RTT_WR windows.

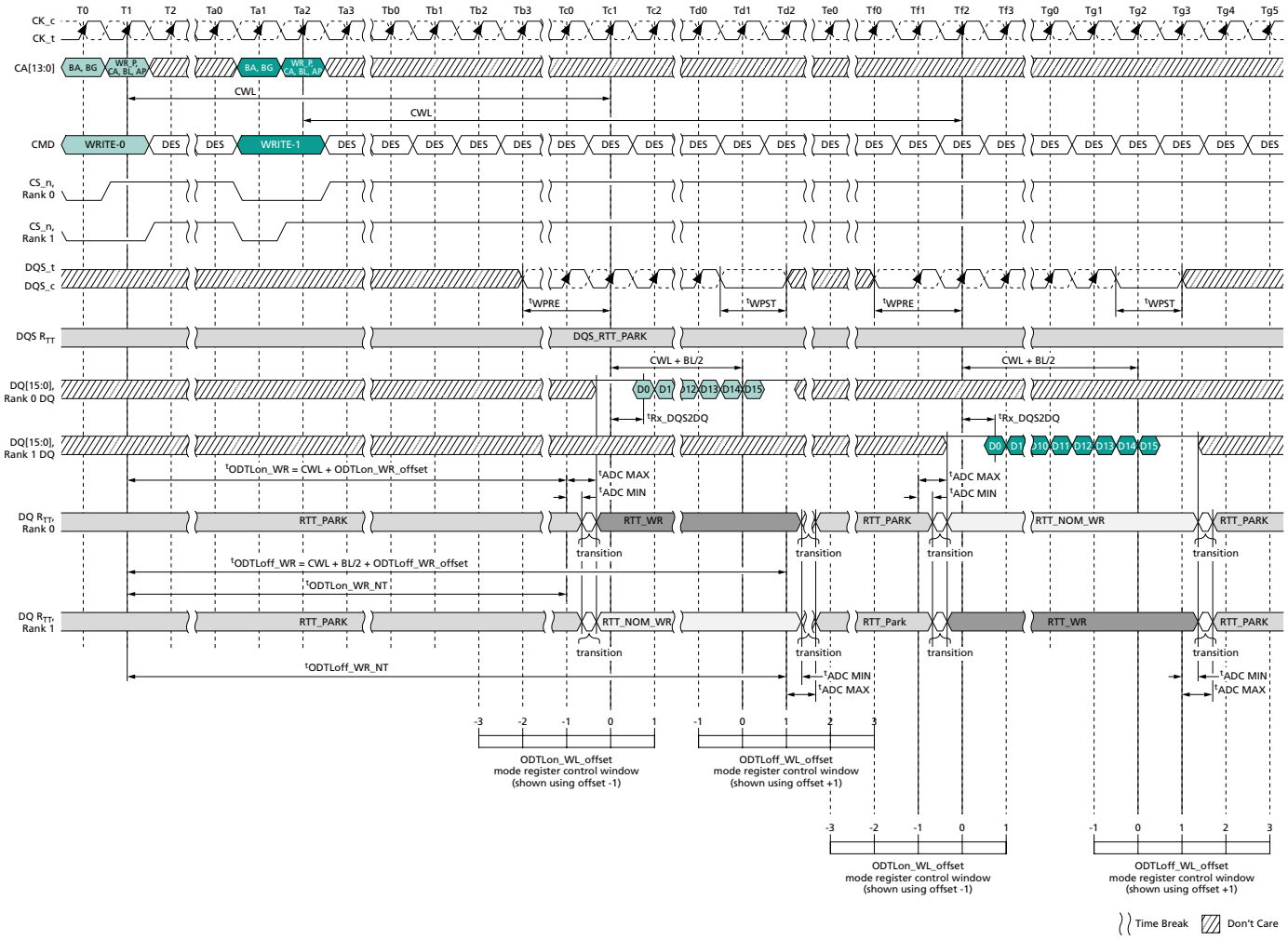
Figure 184: Example 4 — Burst WRITE Operation ODT Latencies and Control Diagrams



Notes: 1. For simplicity, the entire range of ODTL control is not shown.

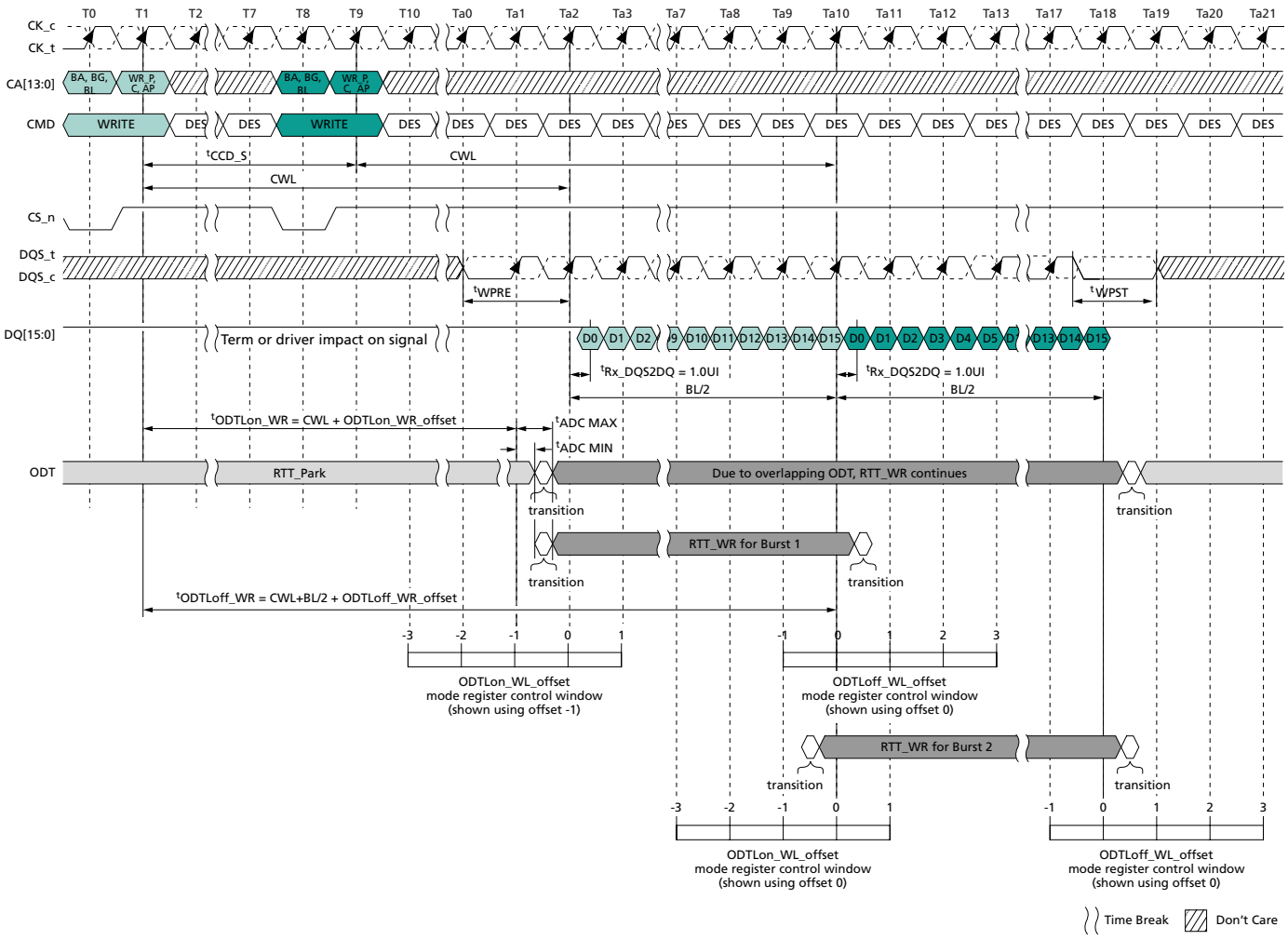
2. Example details - 2tCK tWPRE, 1.5tCK tWPST, 5UI tRX_DQS2DQ, ODTLon_WL_offset configured for +1. ODTLoff_WL_offset configured for +2. Example shows an extreme case where data is significantly delayed from DQS and how the host may want to add an offset to the tODTLon_WR time so that RTT_WR doesn't turn ON too early and how the host may want to delay the tODTLoff_WR time so that it remains ON for the entire burst.
3. System designs and margins may vary requiring larger RTT_WR windows.

Figure 185: Example of WRITE to WRITE Turn Around, Different Ranks



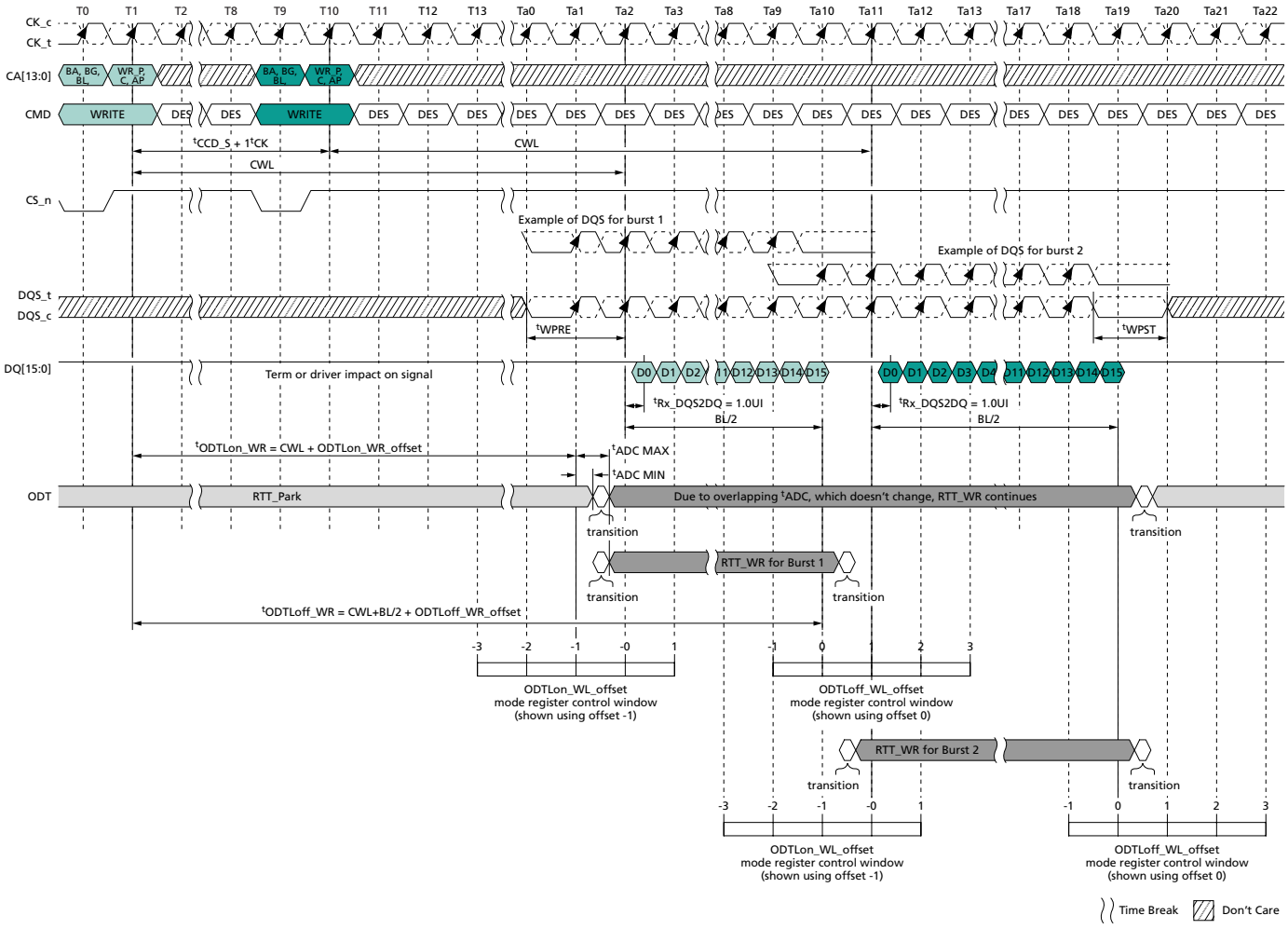
Notes: 1. ODTLon_WR, ODTLon_WR_NT, ODTLoff_WR and ODTLoff_WR_NT are based on mode register settings that can push out or pull in the RTT enable and disable time.
2. For simplicity, the entire range of ODTL control is not shown.

Figure 186: WRITE (BL16) to WRITE (BL16), Different Bank, Seamless Bursts



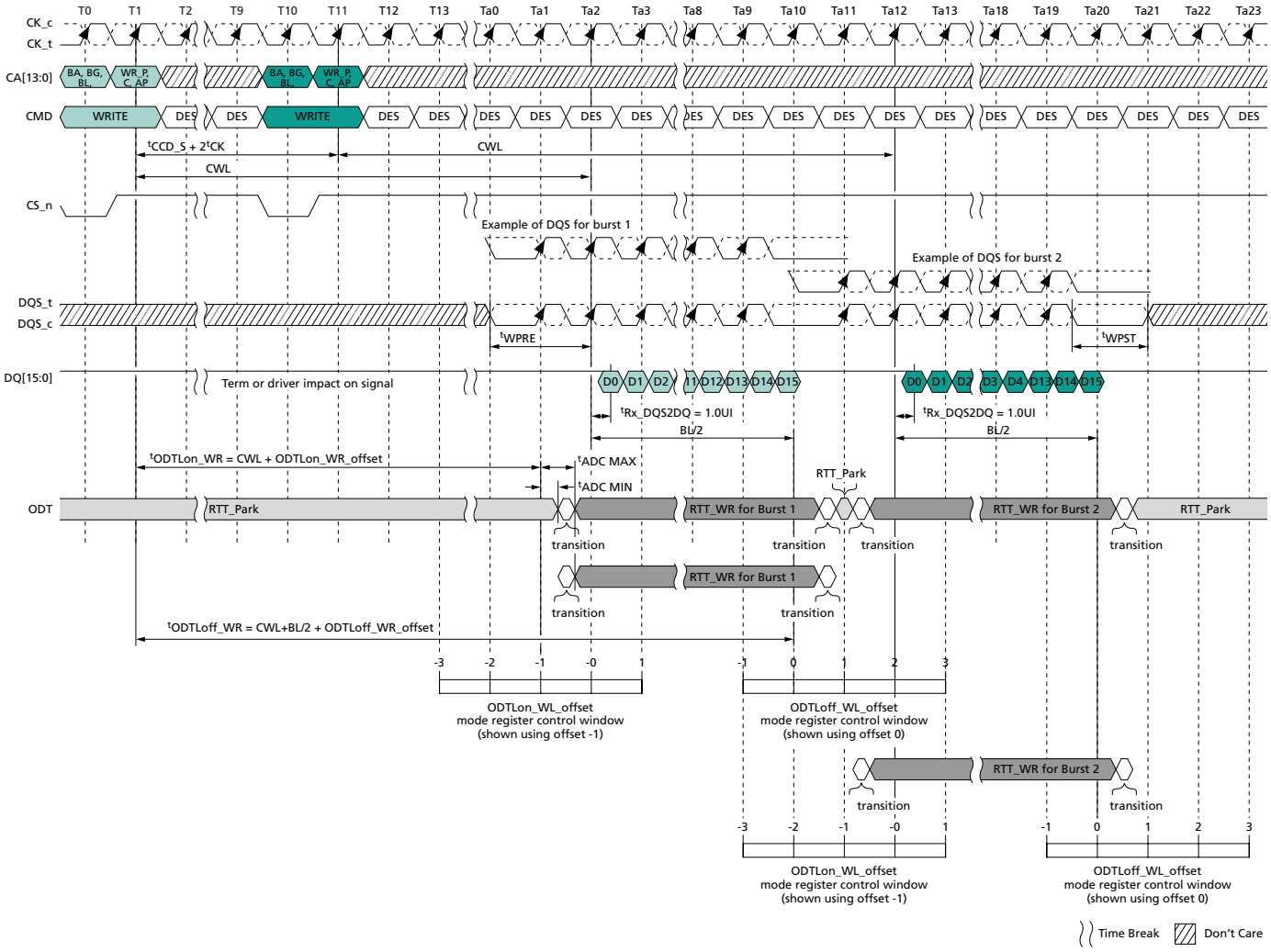
Notes: 1. BL = 16, preamble = 2^{t}CK - 0010 pattern, postamble = 1.5^{t}CK
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. ODTLon_WR_offset = -1, ODTLoff_WR_offset = 0, ^{t}RX_DQS2DQ = 1.0UI
4. In a term-to-WRITE case, the host keeps the DQ signal HIGH 4UI prior to the data being driven in D0.
5. The DFE should assume that 4UI prior to D0 the signal is HIGH.

Figure 187: WRITE (BL16) to WRITE (BL16), Different Bank, 1 tCK Gap



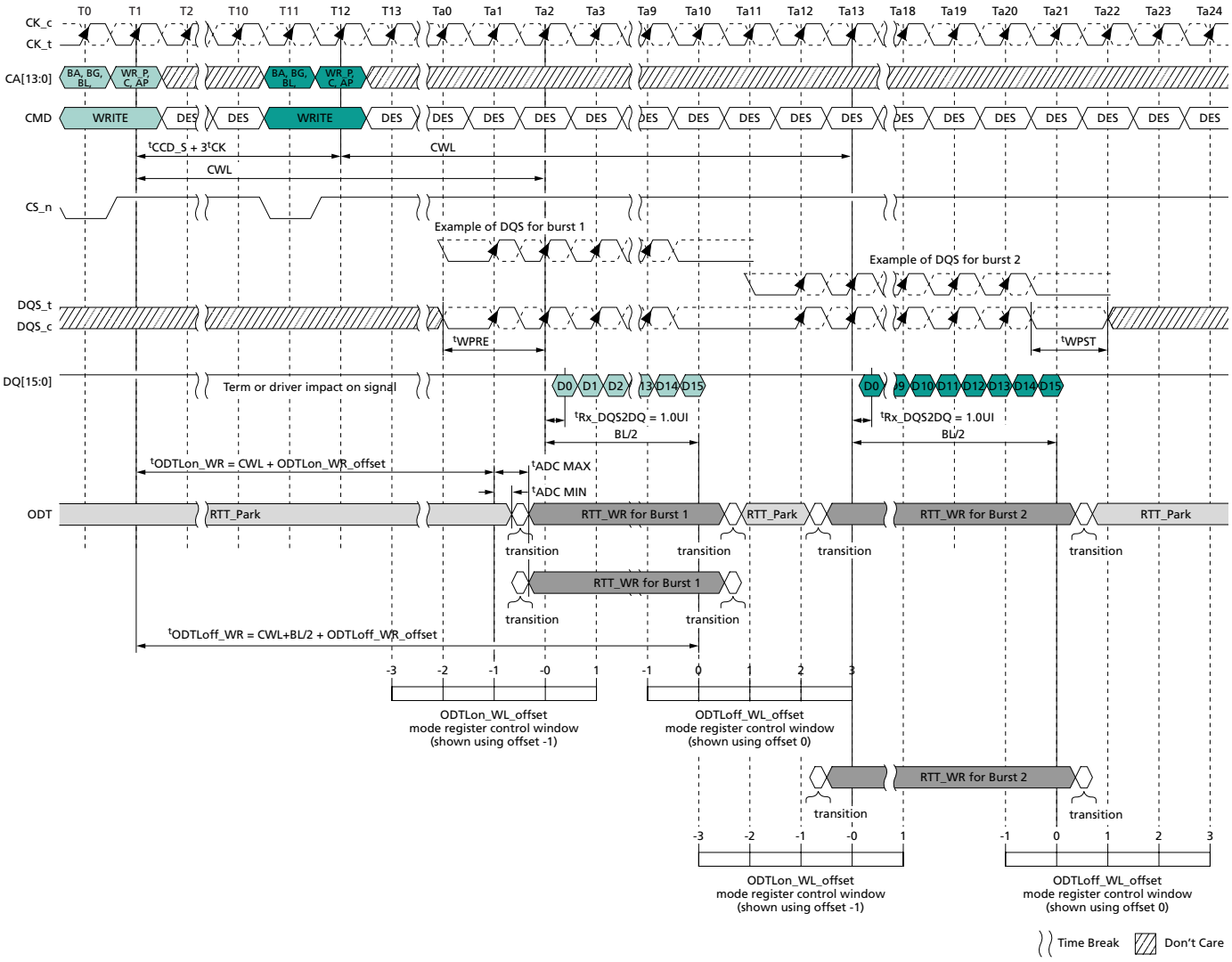
Notes: 1. BL = 16, preamble = 2tCK - 0010 pattern, postamble = 1.5tCK
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. ODTLon_WR_offset = -1, ODTLoff_WR_offset = 0, tRX_DQS2DQ = 1.0UI
4. Example DQS bursts are shown for clarification purposes and are not part of an actual signal.
5. In a term-to-WRITE case, the host keeps the DQ signal HIGH 4UI prior to the data being driven in D0.
6. The DFE should assume that 4UI prior to D0 the signal is HIGH.

Figure 188: WRITE (BL16) to WRITE (BL16), Different Bank, 2 tCK Gap



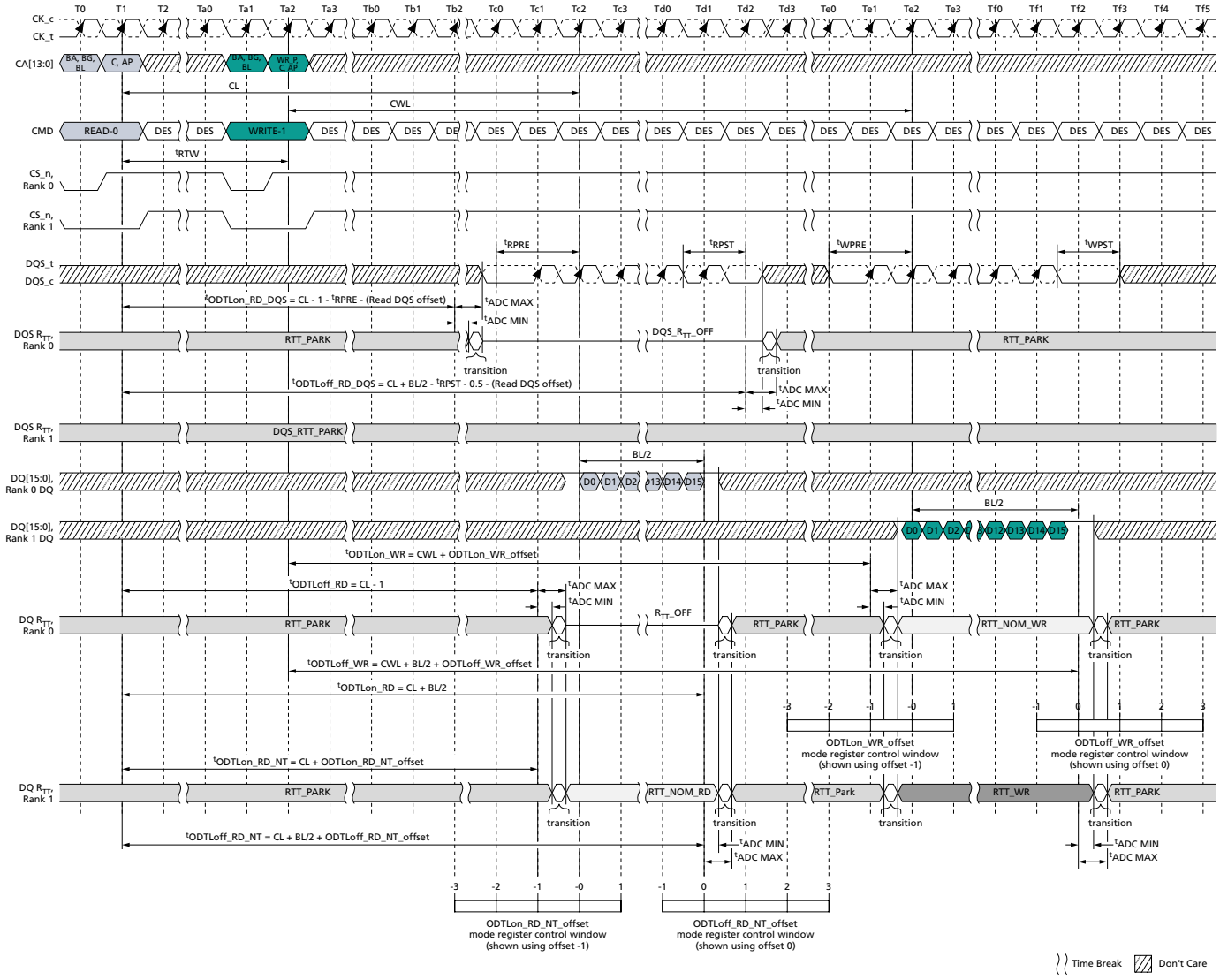
Notes:
1. BL = 16, preamble = 2tCK - 0010 pattern, postamble = 1.5tCK
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. ODTLon_WR_offset = -1, ODTLoff_WR_offset = 0, tRX_DQS2DQ = 1.0UI
4. Example DQS bursts are shown for clarification purposes and are not part of an actual signal.
5. In a term-to-WRITE case, the host keeps the DQ signal HIGH 4UI prior to the data being driven in D0.
6. The DFE should assume that 4UI prior to D0 the signal is HIGH.
7. When a 1 tCK ODT control gap for any ODT operation exists (such as shown in this figure), the gap's RTT value is the same or smaller (weaker termination) than RTT_PARK.

Figure 189: WRITE (BL16) to WRITE (BL16), Different Bank, 3 tCK Gap



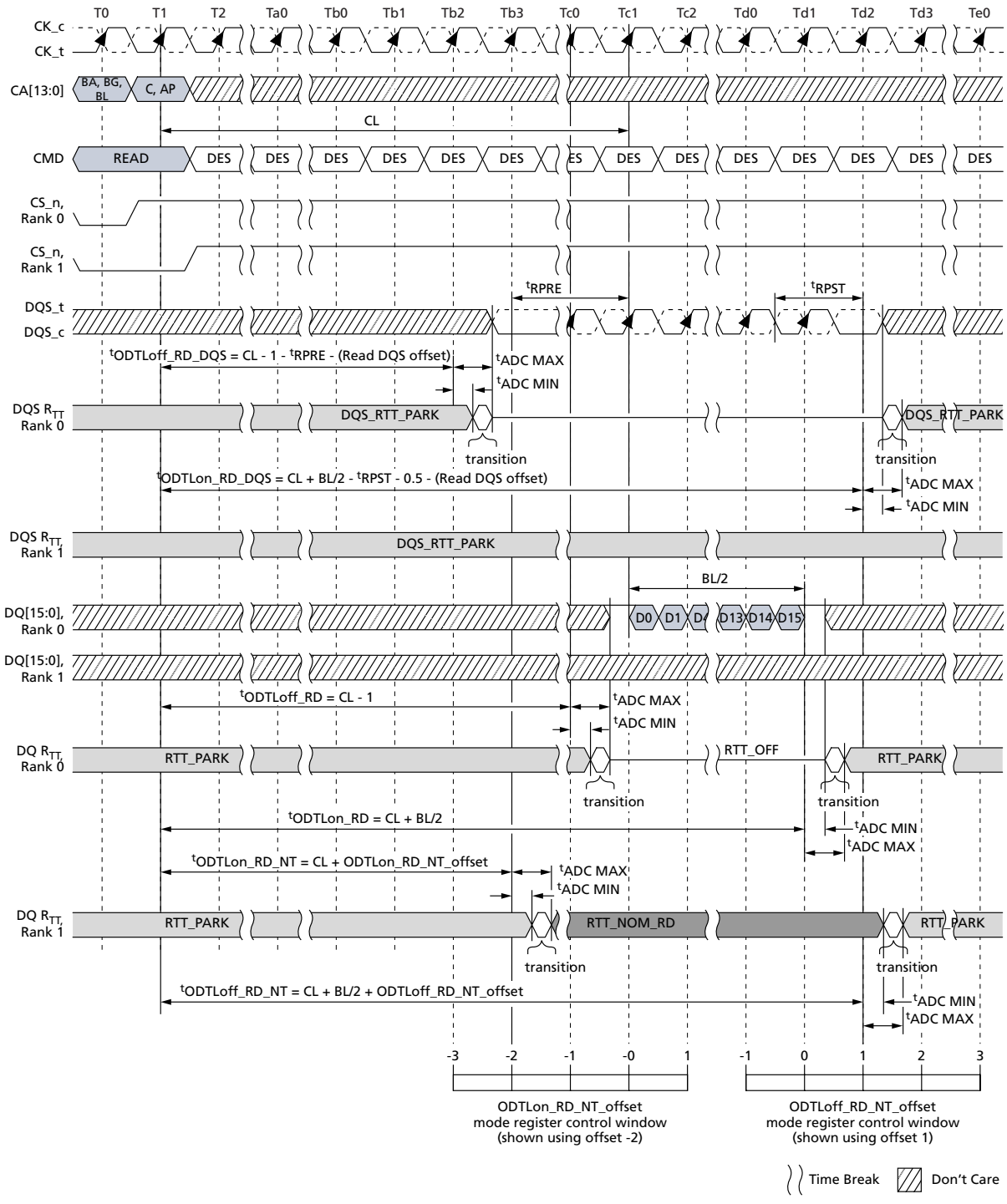
Notes: 1. BL = 16, preamble = 2tCK - 0010 pattern, postamble = 1.5tCK
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. ODTLon_WR_offset = -1, ODTLoff_WR_offset = 0, tRX_DQS2DQ =1.0UI
4. Example DQS bursts are shown for clarification purposes and are not part of an actual signal.
5. In a term-to-WRITE case, the host keeps the DQ signal HIGH 4UI prior to the data being driven in D0.
6. The DFE should assume that 4UI prior to D0 the signal is HIGH.

Figure 190: Example of READ to WRITE turn around, Different Ranks



Notes: 1. ODTLon_WR, ODTLon_WR_NT, ODTLoff_WR and ODTLoff_WR_NT are based on mode register settings that can push out or pull in the RTT enable and disable time.
2. ODTLon_RD_NT and ODTLoff_RD_NT are based on mode register settings that can push out or pull in the RTT enable and disable time.
3. For simplicity, ODTLon_WR_offset and ODTLoff_WR_offset not shown.
4. Example shown with near ideal timings for termination settings, exact offset configurations will vary based on system designs.

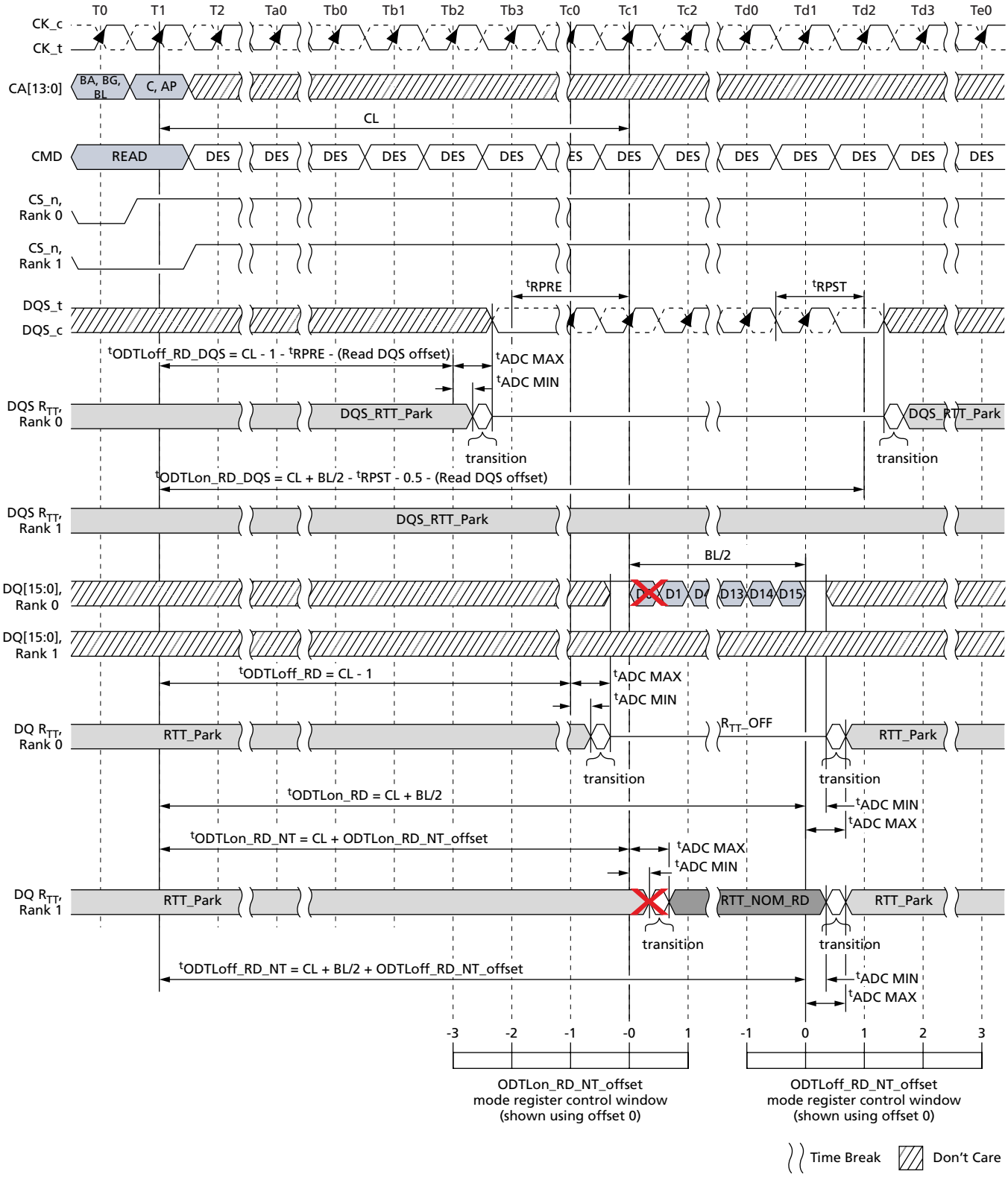
Figure 191: Example of Burst Read Operation ODT Latencies and Control Diagrams



Notes: 1. For simplicity, the entire range of ODTL control is not shown.

2. Example shown with NT_ODT overlapping normal read disable by 1tCK on both sides (ODTLon_RD_NT_offset = -2 and ODTLoff_RD_NT_offset = +1).

Figure 192: Example of Burst Read Operation with ODTLon_RD_NT_offset Set Incorrectly



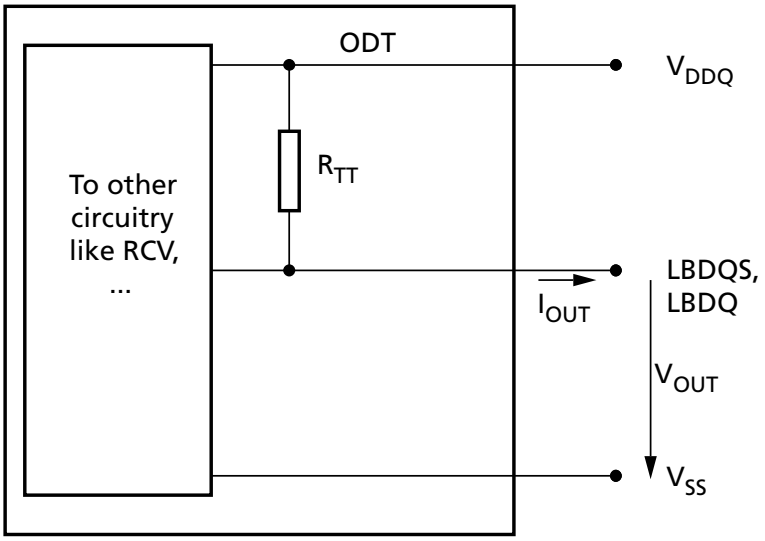
Notes: 1. For simplicity, the entire range of ODTL control is not shown.
2. Since the ODTLon_RD_NT_Offset was left at zero offset and ^{t}ADC still had to be considered, the RTT NT turned on too late for the non-target device. ^{t}ADC is not instantaneous.
3. Since the ^{t}ODTLoff_RD_NT is referenced from the CL, it is not affected by the offset used for the 'on' time and would turn off 1 clock earlier than the read disable RTT if programed to zero offset. ^{t}ODTLon_RD_NT and tODTLoff_RD_NT are independently set and calculated from CL.

On-Die Termination Loopback Signals

The device includes on-die termination (ODT) resistance for the loopback signals LBDQS and LBDQ.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices via MR settings.

Figure 193: Functional Representation of Loopback ODT



The ODT resistance during power up is set to the default values based on TBD. The ODT resistance values can be configured by MR TBD.

The ODT effective resistance R_{TT} is defined by MR bits TBD. ODT is applied to loopback signals LBDQS and LBDQ. ODT effective R_{TT} values supported for the loopback pins is 48 ohms.

$$RTT = \frac{V_{DDQ} - V_{OUT}}{|I_{OUT}|}$$

Table 269: ODT Electrical Characteristics RZQ = 240Ω ± 1% Entire Temperature Operation Range; After Proper ZQ Calibration; $V_{DD} = V_{DDQ}$

R_{TT} (Ohms)	V_{OUT}	Min	Nom	Max	Unit	Notes
48	$V_{OL,DC} = 0.5*V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/5$	1,2,3
	$V_{OM,DC} = 0.8*V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/5$	1,2,3
	$V_{OH,DC} = 0.95*V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/5$	1,2,3
Mismatch LBDQS to LBDQ within Device	$V_{OM,DC} = 0.8*V_{DDQ}$	0	–	8	?	1,2,3,4

Notes: 1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see the following section on voltage and temperature sensitivity.
2. Pull-up ODT resistors are recommended to be calibrated at $0.8*V_{DDQ}$. Other calibration schemes may be used to achieve the linearity spec shown above; that is, calibration at $0.5*V_{DDQ}$ and $0.95*V_{DDQ}$.
3. Measurement definition for R_{TT}: TBD.
4. Loopback ODT mismatch within device variation for a given component including LBDQS and LBDQ.

$$\text{LBDQS - LBDQ mismatch in a device} = \frac{R_{TT\_MAX} - R_{TT\_MIN}}{R_{TT\_NOM}} \times 100$$

CA ODT Strap Operation

With the introduction of on-die termination for CA/CS/CK on DDR5 devices, the setting of the termination values per DRAM is different depending on the configuration of DRAMs on the DIMM or system board.

The CA_ODT pin enables the distinction of two sets of CA/CS/CK ODT settings. When the CA_ODT pin is strapped to a constant V_{SS} setting on the DIMM or board, CA/CS/CK ODT setting is referred to as Group A. When the CA_ODT pin is strapped to a constant V_{DDQ} setting on the DIMM or system board, CA/CS/CK ODT setting is referred to as Group B.

Typical usage is to apply a weak termination setting to Group A devices and a stronger termination setting to Group B devices, which would be at the end of the fly-by routing on the DIMM. To support these different settings, two sets of MPC opcodes are used to target either Group A or Group B devices. In addition to these separate groups of devices based on the CA_ODT pin, PDA commands are also supported. However, the correct combination of the PDA Select ID and MPC opcode must be used according to the CA_ODT pin value.

See CA_ODT pin definition below.

Table 270: CA ODT Pin Definition

Pin Name	Input/Output	Description
CA_ODT	Input	ODT for command and address. Apply group A settings if the pin is connected to V_{SS}. Apply group B settings if the pin is connected to V_{DDQ}.

MR32 and MR33 are defined as follows to show encoding settings for CA,CS,CK and to reflect the need to read the CA_ODT strap value.

Table 271: MR32 Mode Register Settings (For Reference Only)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	CA_ODT Strap Value	CS ODT			CK ODT		

Table 272: MR33 Mode Register Settings (For Reference Only)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		DQS_RTT_PARK			CA ODT		

If CA_ODT Strap Value MR32:OP[6] is 0, the CK ODT, CS ODT, and CA ODT values will reflect the default settings for Group A ODT values, or will reflect what has been written to these mode registers via the MPC opcodes for Set A CK/CS/CA ODT settings.

If CA_ODT Strap Value MR32:OP[6] is 1, the CK ODT, CS ODT, and CA ODT values will reflect the default settings for Group B ODT values, or will reflect what has been written to these mode registers via the MPC opcodes for Set B CK/CS/CA ODT settings.

CA/CS/CK ODT Settings

The following MPC opcodes will be used to set the "Group A" and "Group B" RTT_CA, RTT_CS, and RTT_CK values.

Table 273: ODT MPC Op-Codes (For Reference Only)

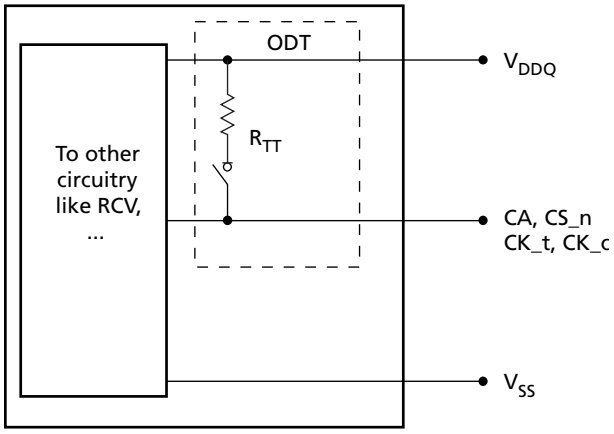
Function	Operand	Data
Initialization and training modes	OP[7:0]	0010 0xxxb: Group A RTT_CK = xxx (See MR32:OP[2:0] for encoding) 0010 1xxxb: Group B RTT_CK = xxx (See MR32:OP[2:0] for encoding) 0011 0xxxb: Group A RTT_CS = xxx (See MR32:OP[5:3] for encoding) 0011 1xxxb: Group B RTT_CS = xxx (See MR32:OP[5:3] for encoding) 0100 0xxxb: Group A RTT_CA = xxx (See MR33:OP[2:0] for encoding) 0100 1xxxb: Group B RTT_CA = xxx (See MR33:OP[2:0] for encoding)

On-Die Termination for CA, CS, CK_t, CK_c

The device includes CA ODT (On-Die Termination) termination resistance for CK_t,CK_c, CS_n and CA signals.

The ODT features are designed to improve signal integrity of the CS, CA, CK_t, and CK_c memory channels by allowing the device controller to turn on and off termination resistance for any target channel on each device via MR settings.

Figure 194: Simple Functional Representation of the CA, CS, CK_t, CK_c ODT Feature



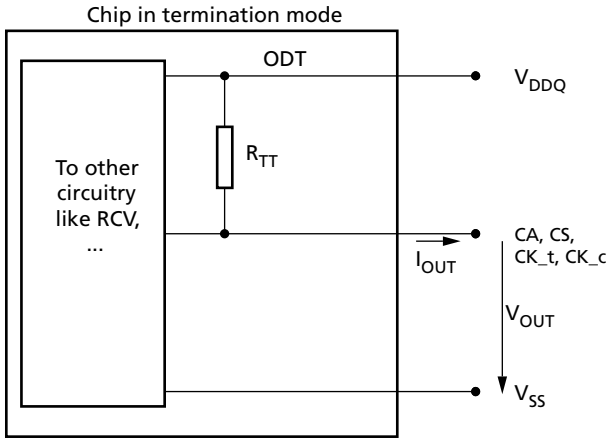
The ODT termination resistance during power up is set to the default values based on MR32 and MR33. The ODT resistance values can be configured using these same registers.

CA On-Die Termination effective resistance RTT is defined by MR bits.

ODT is applied to CK_t, CK_c, CS_n and CA pins. A functional representation is shown below.

$$RTT = \frac{V_{DDQ} - V_{OUT}}{|I_{OUT}|}$$

Figure 195: Simple Functional Representation of the CA, CS, CK_t, CK_c ODT Feature



AC and DC Operating Conditions

Absolute Maximum Ratings

Table 274: Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	–0.3 ~ 1.4	V	1
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	–0.3 ~ 1.4	V	1
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	–0.3 ~ 2.1	V	3
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.3 ~ 1.4	V	1
T_{STG}	Storage temperature	–55 to +100	°C	1, 2

Notes: 1. Stresses greater than those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage temperature is the case surface temperature on the center/top side of the device. For the measurement conditions, refer to JESD51-2 standard.
3. V_{PP} must be equal or greater than V_{DD} /V_{DDQ} at all times during power on and operation of the DRAM device.

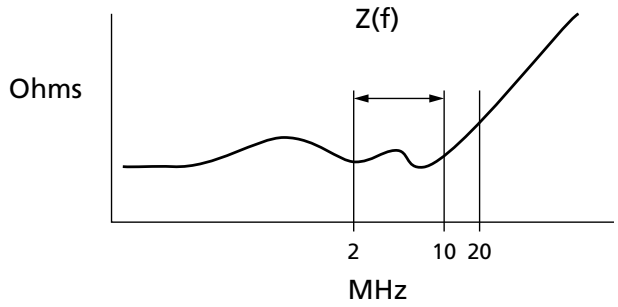
DC Voltage Operating Conditions

Table 275: DC Voltage Operating Conditions

Symbol	Parameter	Low Frequency Voltage Spec				Z(f) Spec Freq: 2–10 MHz		Z(f) Spec Freq: 20 MHz		Notes
		Min	Typ	Max	Unit	Zmax	Unit	Zmax	Unit	
V_{DD}	Supply voltage	1.067 (-3%)	1.1	1.166 (+6%)	V	TBD	mOhms	TBD	mOhms	1, 2, 3, 4
V_{DDQ}	Supply voltage for I/O	1.067 (-3%)	1.1	1.166 (+6%)	V	TBD	mOhms	TBD	mOhms	1, 2, 3, 4
V_{PP}	Pump voltage	1.746 (-3%)	1.8	1.908 (+6%)	V	TBD	mOhms	TBD	mOhms	3, 4

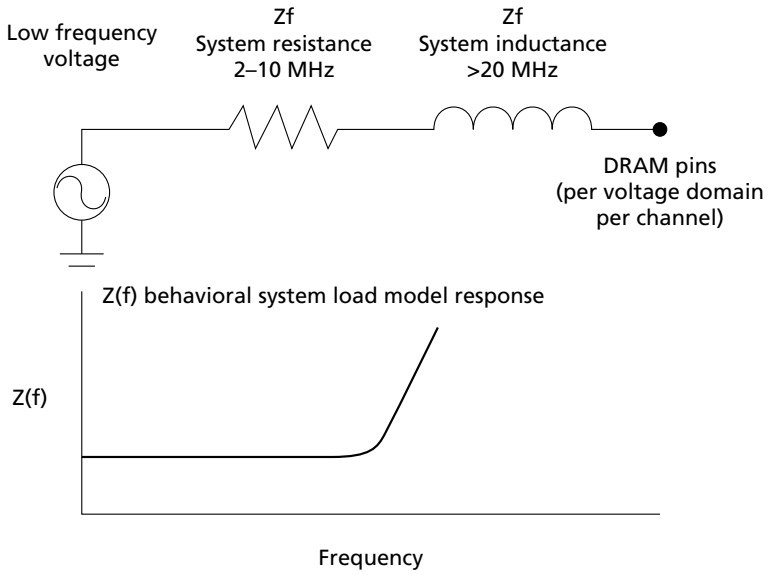
Notes: 1. V_{DD} must be within 66mV of V_{DDQ}.
2. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
3. This includes all voltage noise from DC to 2 MHz at the DRAM package ball.
4. Z(f) is defined for all pins per voltage domain. Z(f) does not include the DRAM package and silicon die.

Figure 196: Zprofile/Z(f) of the System at the DRAM Package Solder Ball (Without DRAM Component)



A simplified electrical system load model for Z(f) with the general frequency response is shown in the figure below. The resistance and inductance can be scaled to generalize the spec response to the DRAM pin.

Figure 197: Simplified Z(f) Electrical Model and Frequency Response of PDN at the DRAM Pin (Without DRAM Component)



Device Component Operating Temperature Range

Table 276: DC Operating Temperature Range

Symbol	Parameter	Temperature Range (Unit °C)		Grade	Notes
		MIN	MAX		
T_{OPER_NORMAL}	Normal operating temperature	0	85	NT	1,2,3,4
$T_{OPER\_EXTENDED}$	Extended operating temperature	0	95	XT	1,2,3,4,5
TOPER_INDUST	Industrial Operating Temperature	-40	95	IT	1,2,3,4,5
TOPER_AUTO	Automotive Operating Temperature	-40	105	AT	1,2,3,4,5

Notes: 1. All operating temperature symbols, ranges, acronyms from JESD402-1.

2. Operating temperature is the case surface temperature on the center/top side of the device. For the measurement conditions, refer to JESD51-2.
3. All devices are required to operate in NT and XT temperature ranges.
4. When operating above 85°C, the host provides appropriate refresh mode controls associated with the increased temperature range. The full description of these settings are defined in the ^{t}REFI parameters for REFab and REFsb Commands by Device Density (including 3DS) table in the Refresh Operation section.
5. Operating temperature for 3DS devices needs to be derated by the number of device dies as: [T_{OPER} – (2.5°C × log2N)], where N is the number of the stacked dies.

AC and DC Global Definitions

This section covers items that are generic across input and output definitions.

Transmitter, Receiver, and Channel Definitions

Transmitter (Tx): Input to the transmitter is the data from the logical portion of the DRAM core and output is at the package pins. The normal components contained in the transmitter are, but not limited to, the pre-driver and the output driver with the transmitter package. The device uses a differential, forwarded strobe-source synchronous system, and single-ended data. The transmitter for a forwarded strobe based source synchronous system must include specification and test methodology for low and high frequency random and deterministic jitter and duty cycle error and must take into account Bounded Uncorrelated Jitter (BUJ), Duty cycle error etc. For single ended signaling cases, crosstalk and Simultaneous switching noise often impact the measurement of the Transmitter. Therefore, the Transmitter's decimated jitter component parameters and the BER must be specified.

Receiver (Rx): The normal components contained in the strobe receiver include a receiver package, an input amplifier (to receive the strobe), and, optionally, a DLL and time adjustment circuitry. Note that although these are typically not present in the DRAM or the data buffer, and distribution circuitry to distribute the strobe to all the receivers. The data input receives the single-ended data and measures it against a reference voltage. The difference between the received signal and reference voltage is then sampled. However, the link may need some form of receiver equalization at the speeds that the device link needs to operate. Because there may not be an input eye margin at the receiver pin, the receiver equalization specification may be defined based on a virtual receive sampler/slicer.

The components of the receiver, which have nothing to do with inter-symbol interference (ISI), must be specified so as to avoid the impact of ISI. Items like receiver jitter, receiver jitter sensitivity, receiver amplitude sensitivity, which are typically orthogonal to ISI, will have to be specified in an ISI-free environment. Either the infrastructure, or the test methodology, will ensure that the correct amount of ISI, or no ISI, for that specific Rx parameter is used. The validation of the receiver is also dependent on either loopback of data being enabled or restricting to receiver testing to be dependent on a pre-specified set of pattern and the accompanying pattern checker and error counters. The receiver equalization will be evaluated in the presence of a set of pre-specified receiver testing golden channels. These receiver testing golden channels will attempt to span the ISI range to which the receiver needs to be designed. The key measurement parameter in this test is the stressed eye and the receiver's error sensitivity to the stressed eye.

Channel: The channel is defined from the transmitter package pin to the receiver package pin and includes all the interconnect topology components included in the channel definition (connectors, sockets, etc.). However, this specification will not specify system platform level channel models, but restrict itself to specifying the golden Tx and Rx evaluation channels.

Applicability

The parameters defined in this section apply to the appropriate sections of the DRAM irrespective of the system, platform, or the topology of the system where the DRAM is situated.

However, the parameters are defined separately for each of the speeds that the device is expected to operate at. (Example speeds are 3.6 Gbps, 4.0 Gbps, 6.4 Gbps etc.)

Source Synchronous Forwarded, Strobe-Based Signaling

The clocking scheme is forwarded, strobe-DQs-based, where an explicit strobe channel is allocated for the strobe edge pattern to be transmitted from one communicating port to the other.

The strobe used is bidirectional; the signaling direction for the data and the strobe reverses when the DRAM transitions from a DRAM read mode to the DRAM write mode.

Tx and Rx Common Specification for DQS and DQ

Each table under the profile dependent specifications contains the following:

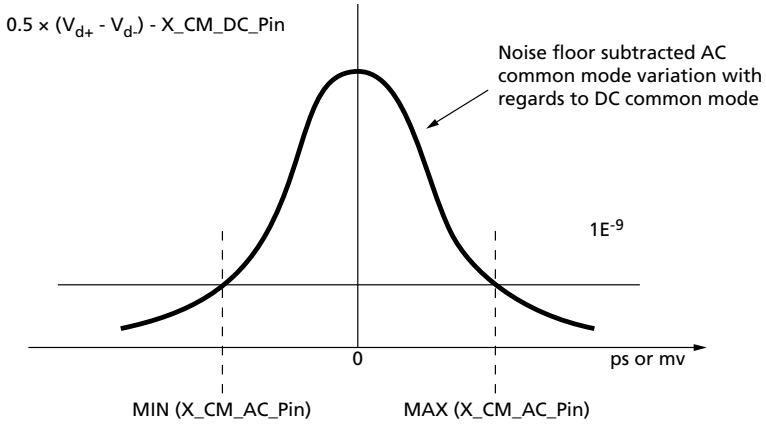
- Parameters for the standalone (individual) transmitter (subscripted with the phrase “Tx”)
- Parameters for the receiver coupled to a test device (subscripted with the phrase “Rx”)

Where possible, the parameters are subscripted with the name of the signal to which the parameter is applied (T for timing; V for voltage).

Distributions For Different Specification Items

The following section describes the statistical methodology typically used (common mode voltage specification is used as an example).

Figure 198: Example of Distribution Profile of AC Common Mode Noise for Either Tx or Rx



Shown here is the statistical distribution (node) for AC common mode around the DC common mode and represents an example of a probability distribution of the common mode parameter. The device parameters must be specified in terms of its statistical distribution. It is assumed that the probability distribution of the parameter is going to be unbounded and uncorrelated unless specifically specified otherwise. The specification for this parameter is defined at BER of E-9 at a prescribed confidence interval.

For DQS Tx, the distribution needs to adhere to the minimum and maximum limits for the parameter VTx_DQS_CM_AC_Pin and the DC common mode VTx_DQS_CM_DC_Pin, as specified in electrical profile dependent tables.

The DQS Rx input compliance and specification validation need to be performed by varying the input DC common mode VRx_DQS_CM_DC_Pin within the prescribed limits and injecting AC common mode noise within the prescribed limits of VRx_DQS_CM_AC_Pin. The number of samples required to

create a distribution to specify any parameter at any BER of interest within a certain Confidence Interval (CI) is evaluated on the basis of the formula described in TBD.

Table 277: Test Conditions Common to All Platforms for Rx and Tx Tests (3200-5200)

Symbol	Parameter	3200-4000		4400-5200		Units	Notes
		Min	Max	Min	Max		
UI_{AVG}	Average UI size[4]	0.999* nominal	1.001* nominal	0.999* nominal	1.001* nominal	ps	
$N_{Min\_UI\_Validation}$	UI number[5]	5.3 x 10^9	-	5.3 x 10^9	-	UI	
BER_{Lane}	BER[6]		1.0 x 10^{-16}		1.0 x 10^{-16}	Events	1, 3

Notes: 1. This is a system parameter. It is the raw BER for every lane before any logical PHY or link layer based correction. It is not possible to have a validation methodology for this parameter for a standalone transmitter or standalone receiver; therefore, this parameter has to be validated in selected systems using a suitable methodology as deemed by the platform.
2. The validation methodologies for these specs are dependent almost solely on the validation hooks built into the silicon itself and thus are determined by the designer and cannot be called out here.
3. BER is uncorrected.
4. Average UI size "f" is data rate in GT/s.
5. # of UI over which the eye mask voltage and timing spec needs to be validated assuming a 99.5% confidence level at 10^{-9} BER.
6. BER per lane. This is a raw BER before any correction. This parameter is primarily used to determine electrical margins during electrical analysis and measurements that are located between two interconnected devices.

Table 278: Test Conditions Common to All Platforms for Rx and Tx Tests (5600-7600)

Symbol	Parameter	5600-6400		6800-7600		Units	Notes
		Min	Max	Min	Max		
UI_{AVG}	Average UI size[4]	TBD	TBD	TBD	TBD	ps	
$N_{Min\_UI\_Validation}$	UI number[5]	TBD	TBD	TBD	TBD	UI	
BER_{Lane}	BER[6]	TBD	TBD	TBD	TBD	Events	1, 3

Notes: 1. This is a system parameter. It is the raw BER for every lane before any logical PHY or link layer based correction. It is not possible to have a validation methodology for this parameter for a standalone transmitter or standalone receiver; therefore, this parameter has to be validated in selected systems using a suitable methodology as deemed by the platform.
2. The validation methodologies for these specs are dependent almost solely on the validation hooks built into the silicon itself and thus are determined by the designer and cannot be called out here.
3. BER is uncorrected.
4. Average UI size "f" is data rate in GT/s.
5. # of UI over which the eye mask voltage and timing spec needs to be validated assuming a 99.5% confidence level at 10^{-9} BER.
6. BER per lane. This is a raw BER before any correction. This parameter is primarily used to determine electrical margins during electrical analysis and measurements that are located between two interconnected devices.

Table 279: Test Conditions Common to All Platforms for Rx and Tx Tests (8000-8800)

Symbol	Parameter	8000-8800		Units	Notes
		Min	Max		
UI_{AVG}	Average UI size[4]	TBD	TBD	ps	
$N_{Min\_UI\_Validation}$	UI number[5]	TBD	TBD	UI	

Table 279: Test Conditions Common to All Platforms for Rx and Tx Tests (8000-8800) (Continued)

Symbol	Parameter	8000-8800		Units	Notes
		Min	Max		
BER_{Lane}	BER[6]	TBD	TBD	Events	1, 3

Notes: 1. This is a system parameter. It is the raw BER for every lane before any logical PHY or link layer based correction. It is not possible to have a validation methodology for this parameter for a standalone transmitter or standalone receiver; therefore, this parameter has to be validated in selected systems using a suitable methodology as deemed by the platform.
2. The validation methodologies for these specs are dependent almost solely on the validation hooks built into the silicon itself and thus are determined by the designer and cannot be called out here.
3. BER is uncorrected.
4. Average UI size "f" is data rate in GT/s.
5. # of UI over which the eye mask voltage and timing spec needs to be validated assuming a 99.5% confidence level at 10^{-9} BER.
6. BER per lane. This is a raw BER before any correction. This parameter is primarily used to determine electrical margins during electrical analysis and measurements that are located between two interconnected devices.

Bit Error Rate

This section provides an overview of the bit error rate (BER) and the desired statistical level of confidence.

Figure 199: General Equation

$$n = \left(\frac{1}{BER}\right)\left[-\ln(1 - SLC) + \ln\left(\sum_{k=0}^{N}\frac{(n \times BER)^k}{k!}\right)\right]$$

Note: 1. Where:
n = number of bits in a trial
SLC = statistical level of confidence
BER = bit error rate
k = intermediate number of specific errors found in trial
N = number of errors recorded during trial

If no errors are assumed in a given test period, the second term drops out and the equation becomes:

$$n = \left(\frac{1}{BER}\right)\left[-\ln(1 - SLC)\right]$$

JEDEC recommends testing to 99.5% confidence levels; however, one may choose a number that is viable for their own manufacturing levels. To determine how many bits of data should be sent (again, assuming zero errors, or N = 0), using BER = $1E^{-9}$and confidence level SLC = 99.5%, the result is n = (1/BER)(-ln(1 - 0.995) = 5.298 x 10^9.

Table 280: Estimated Number of Transmitted Bits (*n*) – Confidence Level of 70–99.5%

Number of Errors	*n* = -ln(1 - SLC)/BER							
	99.5%	99%	95%	90%	85%	80%	75%	70%
0	5.298/BER	4.61/BER	2.99/BER	2.3/BER	1.90/BER	1.61/BER	1.39/BER	1.20/BER

Minimum BER Requirements

The following table specifies the average UI and BER requirements over which certain receiver and transmitter timing and voltage specifications need to be validated assuming a 99.5% confidence level at BER = $1E^{-9}$.

Table 281: Minimum BER Requirements for Rx/Tx Timing and Voltage Tests (3200–6400)

Parameter	Symbol	3200–4800			5200–6400			Unit	Notes
		Min	Nom	Max	Min	Nom	Max		
Average UI	UI_{AVG}	0.999 * nom	1.000/f	1.001 * nom	0.999 * nom	1.000/f	1.001 * nom	ps	1
Number of UI (min)	$N_{Min\_UI\_Validation}$	5.3 x 10^9	–	–	5.3 x 10^9	–	–	UI	2
Bit error rate	BER_{Lane}	–	–	$1E^{-16}$	–	–	$1E^{-16}$	Events	3–6

Notes: 1. Average UI size; "f" is data rate.
2. Number of UI over which certain Rx/Tx timing and voltage specifications need to be validated assuming a 99.5% confidence level at BER=$1E^{-9}$.
3. This is a system parameter. It is the raw BER for every lane before any logical PHY or link layer-based correction. It may not be possible to have a validation methodology for this parameter for a standalone transmitter or standalone receiver; therefore, this parameter has to be validated in selected systems using a suitable methodology as deemed by the platform.
4. This is a raw BER-per-lane before any correction. This parameter is primarily used to determine electrical margins during electrical analysis and measurements that are located between two interconnected devices.
5. This is the minimum BER requirements for testing timing and voltage parameters listed in Input Clock Jitter, Rx DQS & DQ Voltage Sensitivity, Rx DQS Jitter Sensitivity, Rx DQ Stressed Eye, Tx DQS Jitter, Tx DQ Jitter, and Tx DQ Stressed eye height / eye width specifications.
6. The BER for DDR5 during normal operation is $1E^{-16}$. For validation purposes, the BER used is $1E^{-9}$.

Table 282: Minimum BER Requirements for Rx/Tx Timing and Voltage Tests (6800-8800)

Parameter	Symbol	6800-7200			7600-8800			Unit	Notes
		Min	Nom	Max	Min	Nom	Max		
Average UI	UI_{AVG}	TBD	TBD	TBD	TBD	TBD	TBD	ps	1
Number of UI (min)	$N_{Min\_UI\_Validation}$	TBD	–	–	TBD	–	–	UI	2
Bit error rate	BER_{Lane}	–	–	TBD	–	–	TBD	Events	3–6

Notes: 1. Average UI size; "f" is data rate.
2. Number of UI over which certain Rx/Tx timing and voltage specifications need to be validated assuming a 99.5% confidence level at BER=$1E^{-9}$.
3. This is a system parameter. It is the raw BER for every lane before any logical PHY or link layer-based correction. It may not be possible to have a validation methodology for this parameter for a standalone transmitter or standalone receiver; therefore, this parameter has to be validated in selected systems using a suitable methodology as deemed by the platform.
4. This is a raw BER-per-lane before any correction. This parameter is primarily used to determine electrical margins during electrical analysis and measurements that are located between two interconnected devices.
5. This is the minimum BER requirements for testing timing and voltage parameters listed in Input Clock Jitter, Rx DQS & DQ Voltage Sensitivity, Rx DQS Jitter Sensitivity, Rx DQ Stressed Eye, Tx DQS Jitter, Tx DQ Jitter, and Tx DQ Stressed eye height / eye width specifications.
6. The BER for DDR5 during normal operation is $1E^{-16}$. For validation purposes, the BER used is $1E^{-9}$.

Unit Interval and Jitter Definitions

This section describes the UI and NUI jitter definitions associated with the jitter parameters specified in Rx stressed eye, Tx DQS jitter, Tx DQ jitter and input clock jitter specifications.

Unit Interval (UI)

The times at which the differential crossing points of the clock occur are defined at t1, t2, …, tn-1, tn,..., tK. The UI at index *n* is defined below (with *n* = 1,2,…) from an arbitrary time in steady state, where *n* = 0 is chosen as the starting crossing point.

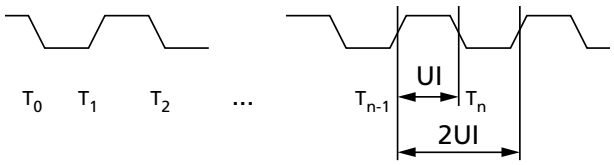
Mathematical definition of UI is shown in the following figures.

Figure 200: UI Definition in Terms of Adjacent Edge Timings

$$UI_n = t_n - t_{n-1}$$

For the single-ended data, the unit interval time starts when the signal crosses a pre-specified reference voltage. For the differential clock, the unit interval time starts when the CK_t and CK_c intersect.

Figure 201: UI Definition Using Clock Waveforms



UI Jitter Definition

If a number of UI edges are computed or measured at times t1, t2, …, tn-1, tn,..., tK, where K is the maximum number of samples, then the UI jitter at any instance *n* is defined below, where T = the ideal UI size.

Figure 202: UI Jitter for "nth" UI Definition (in Terms of Ideal UI)

$$UI(jit)_n = (t_n - t_{n-1}) - T,\ n = 1, 2, 3, \ldots, K$$

In a large sample with random Gaussian-like jitter (very close to symmetric distribution), the average of all UI sizes usually turns out to be very close to the ideal UI size.

The equation described above assumes starting from an instant steady state, where *n* = 0 is chosen as the starting point.

1 UI = one bit, which means 2 UI = one full cycle or time period of the forwarded strobe. Example: For 6.4 GT/s signaling, the forwarded strobe frequency is 3.2 GHz, or 1 UI = 156.25ps.

Deterministic jitter is analyzed in terms of the peak-to-peak value and in terms of specific frequency components present in the jitter, isolating the causes for each frequency. Random jitter is unbounded and analyzed in terms of statistical distribution to convert to a bit error rate (BER) for the link.

UI-UI Jitter Definition

UI-UI (read as "UI to UI") jitter is defined to be the jitter between two consecutive UI, as shown below.

$$\Delta UI_n = UI_n - UI_{n-1},\ n = 2, 3, \ldots, K$$

Accumulated Jitter (Over n UI)

Accumulated jitter is defined as the jitter accumulated over any consecutive "*n*" UI, as shown below.

$$T_{acc}^{N} = \sum_{p=m}^{m+N-1} (UI_p - \overline{UI}) \quad m = 1, 2, 3, \ldots, K–N$$

Definition of UI

$$\overline{UI} = \frac{\sum_{p=1}^{K} UI_p}{K} \quad p = 1, 2, 3, \ldots, N, \ldots, K$$

Differential Input Cross Point Voltage (V_{IX})

Differential Strobe (DQS_t, DQS_c) Input Cross Point Voltage (V_{IX_DQS})

Figure 203: V_{IX_DQS} Definition

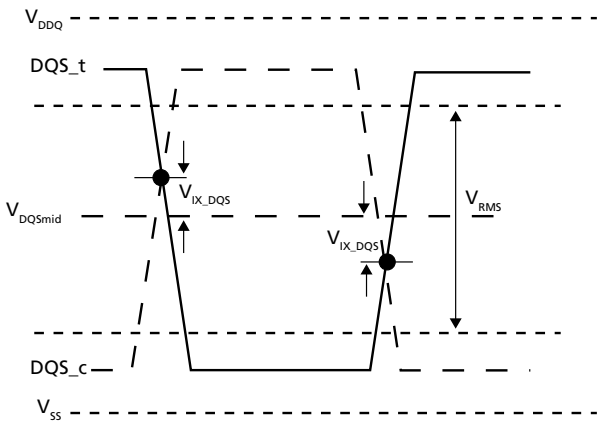


Table 283: Cross Point Voltage for DQS Differential Input Signals (V_{IX_DQS})

Parameter	Symbol	3200-4800		5200-6400		6800-8400		Unit	Notes
		Min	Max	Min	Max	Min	Max		
DQS differential input cross point voltage ratio	$V_{IX\_DQS\_Ratio}$	–	50	–	50	–	TBD	%	1, 2,3

Notes: 1. The V_{IX_DQS} voltage is referenced to VDQSmid(mean) = (DQS_t voltage + DQS_c voltage) /2, where the mean is over 8 UI.
2. $V_{IX\_DQS\_Ratio}$ = ($|V_{IX\_DQS}| / V_{RMS}$) * 100%, where V_{RMS} = |RMS(DQS_t voltage - DQS_c voltage)|.
3. Only applies when both DQS_t and DQS_c are transitioning (including preamble).

Differential Input Clock (CK_t, CK_c) Cross Point Voltage (V_{IX_CK})

Figure 204: V_{IX_CK} Definition

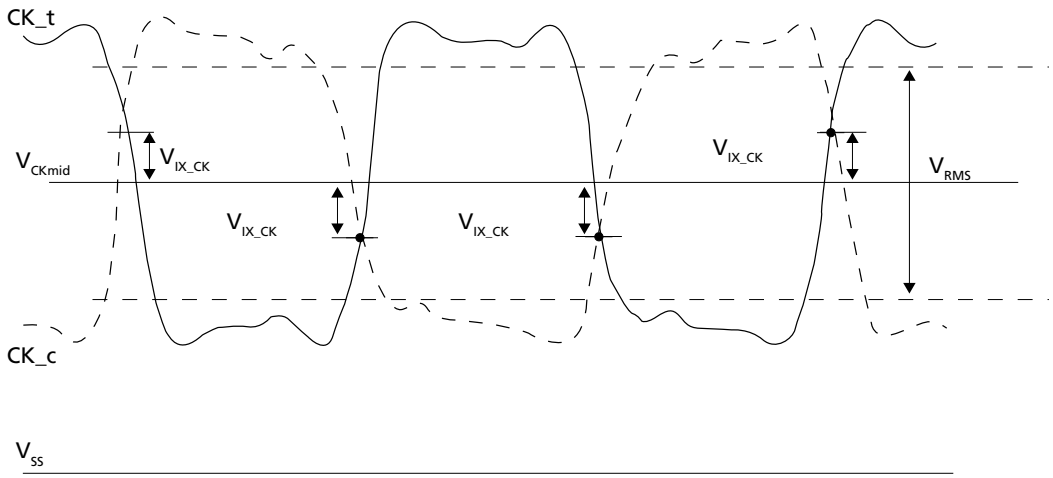


Table 284: Cross Point Voltage for Differential Input Clock (V_{IX_CK})

Parameter	Symbol	3200-4800		5200-6400		6800-8400		Unit	Notes
		Min	Max	Min	Max	Min	Max		
CK differential input cross point voltage ratio	$V_{IX\_CK\_Ratio}$	–	50	–	50	–	TBD	%	1, 2,3

Notes: 1. The V_{IX_CK} voltage is referenced to $V_{CKmid(mean)}$ = (CK_t voltage + CK_c voltage) /2, where the mean is over 8 UI.
2. $V_{IX\_CK\_Ratio}$ = (|V_{IX_CK}| / V_{RMS}) * 100%, where V_{RMS} = RMS (|CK_t voltage - CK_c voltage|).
3. Only applies when both CK_t and CK_c are transitioning.

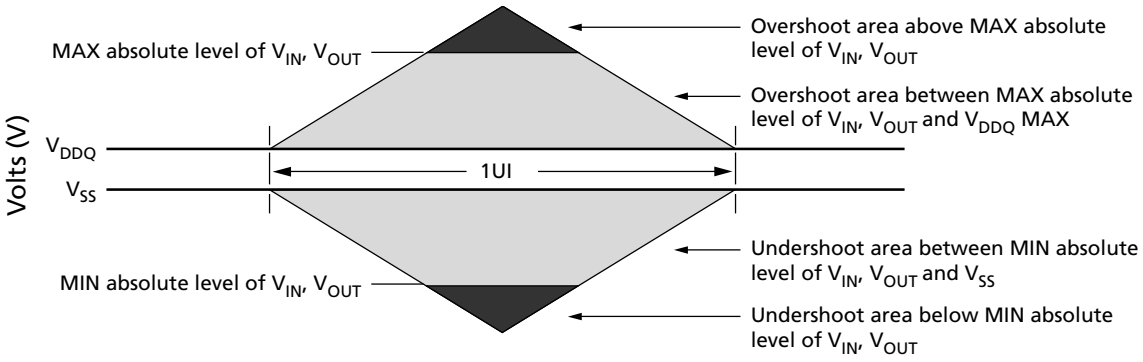
AC and DC Input Measurement Levels

AC and DC Logic Input Levels for Command, Address and Control

Table 285: Overshoot/Undershoot Specifications for Command, Address and Control Pins

Parameter	DDR 5 Specification						Unit
	3200/3600	4000/4400	4800/5200	5600	6000	6400	
Maximum peak amplitude above V_{DDQ} absolute max allowed for overshoot area	TBD	TBD	TBD	TBD	TBD	TBD	V
Delta value between V_{DDQ} absolute max and V_{DDQ} max allowed for overshoot area	TBD	TBD	TBD	TBD	TBD	TBD	V
Maximum peak amplitude allowed for undershoot area	TBD	TBD	TBD	TBD	TBD	TBD	V-ns
Maximum overshoot area per 1tCK above absolute max	TBD	TBD	TBD	TBD	TBD	TBD	V-ns
Maximum overshoot area per 1tCK between absolute max and V_{DDQ} max	TBD	TBD	TBD	TBD	TBD	TBD	V-ns
Maximum undershoot area per 1tCK below V_{SS}	TBD	TBD	TBD	TBD	TBD	TBD	V-ns

Figure 205: Overshoot/Undershoot



CA Rx Voltage and Timings

The command, address and control (including chip select) input receiver compliance mask for voltage and timing is shown in the figure below. All CA and CS_n signals apply the same compliance mask and operate in single data rate mode.

The CA input receiver mask (Rx Mask) for voltage and timing is applied across all CA[13:0] pins and the CS_n pin. For the remainder of this section, the reference to "CA" should be applied to the device CA[13:0] pins as well as the CS_n pin. The Rx Mask defines the area the input signal must not encroach for the device input receiver to successfully capture a valid input signal; it is not the valid data-eye.

Figure 206: CA/CS_n Rx Mask

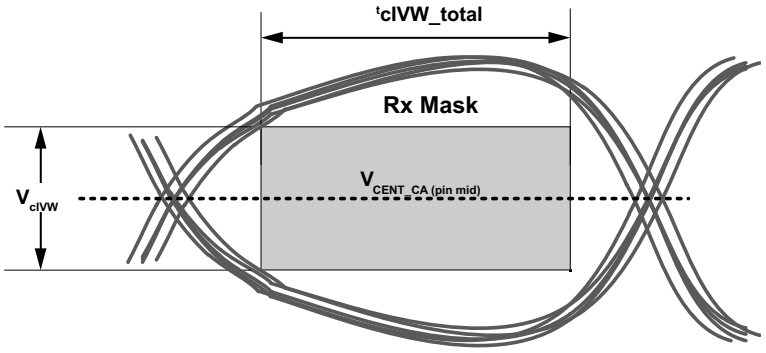
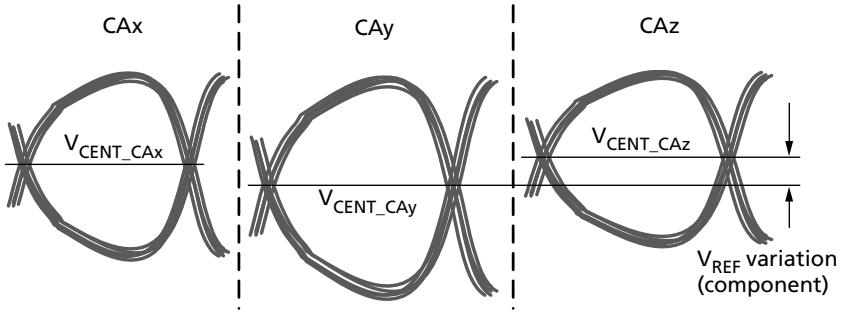


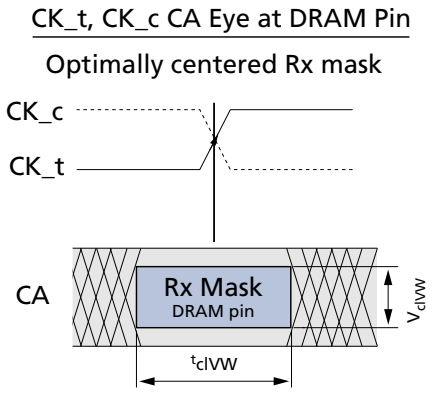
Figure 207: Across-Pin V_{REFCA} Voltage Variation



$V_{cent\_CA(pin\ mid)}$ is defined as the midpoint between the largest V_{cent_CA} voltage level and the smallest V_{cent_CA} voltage level across all CA and CS_n pins for a given device component.

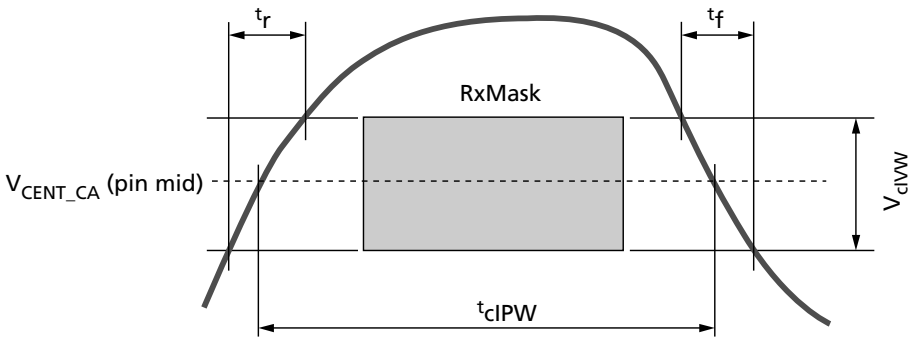
Each CA V_{cent} level is defined by the center (widest opening) of the cumulative data input eye as depicted in the previous figure (Across-Pin V^{REFCA} Voltage Variation). This clarifies any device component level variation must be accounted for within the CA Rx Mask. The component-level V_{REF} is set by the system to account for R_{ON} and ODT settings.

Figure 208: CA/CS_n Timings at the Device Pins



$^{t}cIVW$ is not necessarily center-aligned on CK_t/CK_c crossing at the DRAM pin, but is assumed to be center-aligned at the DRAM latch.

Figure 209: CA T_{clPW} and S_{RIN_clVW} Definition (For Each Input Pulse)



Note: 1. $S_{RIN\_clVW} = V_{clVW\_Total}/({}^{t}r$ or ${}^{t}f)$, signal must be monotonic within ${}^{t}r$ and ${}^{t}f$ range.

Figure 210: CA V_{IHL_AC} Definition (For Each Input Pulse)

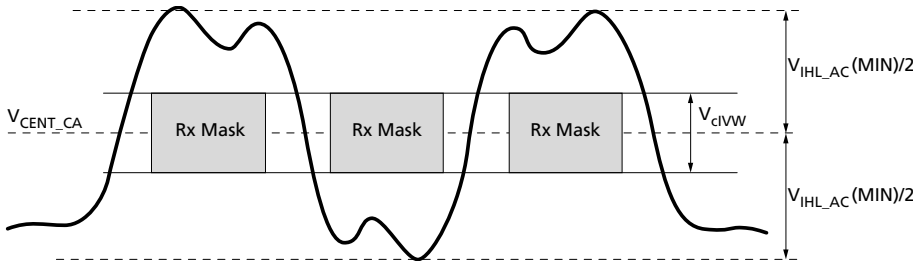


Table 286: DDR5 3200-4800 Command/Address, CS Parametric Values

Symbol	Parameter	3200		3600		4000		4400		4800		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
V_{clVW}	Rx Mask voltage - p-p	-	140	-	140	-	140	-	130	-	130	mV	1,2,4
${}^{t}clVW$	Rx timing window	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	UI*	1,2,3,4,8
V_{IHL_AC}	CA input pulse amplitude	160		160		160		150		150		mV	7
${}^{t}clPW$	CA input pulse width	0.58		0.58		0.58		0.58		0.58		UI*	5,8
S_{RIN_clVW}	Input slew rate over V_{clVW}	1	7	1	7	1	7	1	7	1	7	V/ns	6

Notes: 1. CA Rx Mask voltage and timing parameters at the pin, including voltage and temperature drift.
2. Rx Mask voltage $V_{clVW\ total(MAX)}$ must be centered around $V_{cent\_CA(pin\ mid)}$.
3. Rx differential CA to CK jitter total timing window at the V_{clVW} voltage levels.
4. Defined over the CA internal V_{REF} range. The Rx Mask at the pin must be within the internal V_{REFCA} (or V_{REFCS}) range, irrespective of the input signal common mode.
5. CA only minimum input pulse width defined at the $V_{cent\_CA(pin\ mid)}$.
6. Input slew rate over $V_{clVW\ Mask}$ centered at $V_{cent\_CA(pin\ mid)}$.
7. V_{IHL_AC} does not have to be met when no transitions are occurring.

8. UI=^{t}ck(avg)MIN.

Table 287: DDR5 5200-6400 Command/Address, CS Parametric Values

Symbol	Parameter	5200		5600		6000		6400		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
V_{CIVW}	Rx Mask voltage - p-p	-	100	-	100	-	TBD	-	TBD	mV	1,2,4
$^{t}CIVW$	Rx timing window	-	0.2	-	0.2	-	TBD	-	TBD	UI*	1,2,3,4,8
V_{IHL_AC}	CA input pulse amplitude	115		115		TBD		TBD		mV	7
$^{t}CIPW$	CA input pulse width	0.58		0.58		TBD		TBD		UI*	5,8
$S_{RIN\_CIV\ W}$	Input slew rate over V_{CIVW}	1	7	1	7	TBD	TBD	TBD	TBD	V/ns	6

Notes: 1. CA Rx Mask voltage and timing parameters at the pin, including voltage and temperature drift.
2. Rx Mask voltage $V_{CIVW\ total(MAX)}$ must be centered around $V_{cent\_CA(pin\ mid)}$.
3. Rx differential CA to CK jitter total timing window at the V_{CIVW} voltage levels.
4. Defined over the CA internal V_{REF} range. The Rx Mask at the pin must be within the internal V_{REFCA} (or V_{REFCS}) range, irrespective of the input signal common mode.
5. CA only minimum input pulse width defined at the $V_{cent\_CA(pin\ mid)}$.
6. Input slew rate over $V_{CIVW\ Mask}$ centered at $V_{cent\_CA(pin\ mid)}$.
7. V_{IHL_AC} does not have to be met when no transitions are occurring.
8. UI=^{t}ck(avg)MIN.

Table 288: DDR5 6800-8000 Command/Address, CS Parametric Values

Symbol	Parameter	6800		7200		7600		8000		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
V_{CIVW}	Rx Mask voltage - p-p	-	TBD	-	TBD	-	TBD	-	TBD	mV	1,2,4
$^{t}CIVW$	Rx timing window	-	TBD	-	TBD	-	TBD	-	TBD	UI*	1,2,3,4,8
V_{IHL_AC}	CA input pulse amplitude	TBD		TBD		TBD		TBD		mV	7
$^{t}CIPW$	CA input pulse width	TBD		TBD		TBD		TBD		UI*	5,8
$S_{RIN\_CIV\ W}$	Input slew rate over V_{CIVW}	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	V/ns	6

Notes: 1. CA Rx Mask voltage and timing parameters at the pin, including voltage and temperature drift.
2. Rx Mask voltage $V_{CIVW\ total(MAX)}$ must be centered around $V_{cent\_CA(pin\ mid)}$.
3. Rx differential CA to CK jitter total timing window at the V_{CIVW} voltage levels.
4. Defined over the CA internal V_{REF} range. The Rx Mask at the pin must be within the internal V_{REFCA} (or V_{REFCS}) range, irrespective of the input signal common mode.
5. CA only minimum input pulse width defined at the $V_{cent\_CA(pin\ mid)}$.
6. Input slew rate over $V_{CIVW\ Mask}$ centered at $V_{cent\_CA(pin\ mid)}$.
7. V_{IHL_AC} does not have to be met when no transitions are occurring.

8. UI=^{t}ck(avg)MIN.

Table 289: DDR5 8400-8800 Command/Address, CS Parametric Values

Symbol	Parameter	8400		8800		Unit	Notes
		MIN	MAX	MIN	MAX		
V_{clVW}	Rx Mask voltage - p-p	-	TBD	-	TBD	mV	1,2,4
$^{t}_{clVW}$	Rx timing window	-	TBD	-	TBD	UI*	1,2,3,4,8
V_{IHL_AC}	CA input pulse amplitude	TBD		TBD		mV	7
$^{t}_{clPW}$	CA input pulse width	TBD		TBD		UI*	5,8
$S_{RIN\_clV\ W}$	Input slew rate over V_{clVW}	TBD	TBD	TBD	TBD	V/ns	6

Notes: 1. CA Rx Mask voltage and timing parameters at the pin, including voltage and temperature drift.
2. Rx Mask voltage $V_{clVW\ total(MAX)}$ must be centered around $V_{cent\_CA(pin\ mid)}$.
3. Rx differential CA to CK jitter total timing window at the V_{clVW} voltage levels.
4. Defined over the CA internal V_{REF} range. The Rx Mask at the pin must be within the internal V_{REFCA} (or V_{REFCS}) range, irrespective of the input signal common mode.
5. CA only minimum input pulse width defined at the $V_{cent\_CA(pin\ mid)}$.
6. Input slew rate over $V_{clVW\ Mask}$ centered at $V_{cent\_CA(pin\ mid)}$.
7. V_{IHL_AC} does not have to be met when no transitions are occurring.
8. UI=^{t}ck(avg)MIN.

Differential Input Voltage Levels for Clock

Table 290: Differential Clock (CK_t, CK_c) Input Levels for DDR5 3200-6400

Symbol	Parameter	3200-6400	Note
$V_{IH,diffCK}$	Differential input high measurement level	0.75 x $V_{diff,pk-pk}$	1,2
$V_{IL,diffCK}$	Differential input low measurement level	0.25 x $V_{diff,pk-pk}$	1,2

Notes: 1. $V_{diff,pk-pk}$ defined in the Differential Input Slew Rate Definition for CK_t, CK_c figure (next section).
2. $V_{diff,pk-pk}$ is the mean high voltage minus the mean low voltage over TBD samples.
3. All parameters are defined over the entire clock common mode range.

Differential Input Slew Rate Definition for Clock

Figure 211: Differential Input Slew Rate Definition for Clock (CK_t, CK_c)

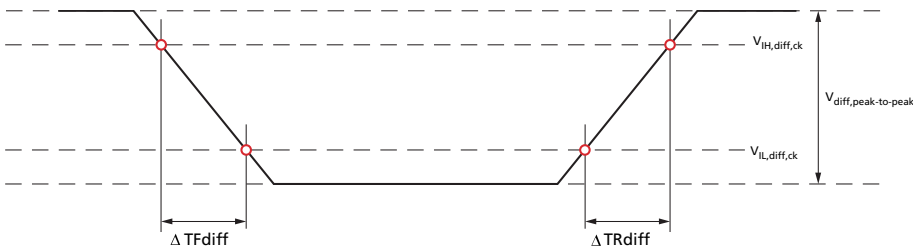


Table 291: Differential Input Slew Rate Definition for Clock (CK_t, CK_c)

Parameter	Measured		Defined By
	From	To	
Differential input slew rate for rising edge (CK_t - CK_c)	$V_{IL,diffCK}$	$V_{IH,diffCK}$	$\lvert(V_{IL,diffCK} - V_{IH,diffCK})\rvert$ / delta TR_{diff}
Differential input slew rate for falling edge (CK_t - CK_c)	$V_{IH,diffCK}$	$V_{IL,diffCK}$	$(V_{IH,diffCK} - V_{IL,diffCK})$ / delta TF_{diff}

Table 292: Differential Input Slew Rate for Clock (CK_t, CK_c) — 3200-6400

Parameter	Symbol	3200-4800		5200-5600		6000-6400		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
Differential input slew rate for CK_t - CK_c	S_{RIdiff_CK}	2	14	TBD	TBD	TBD	TBD	V/ns

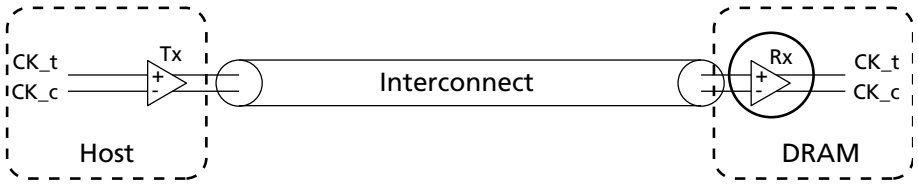
Table 293: Differential Input Slew Rate for Clock (CK_t, CK_c) — 6800-8800

Parameter	Symbol	6800-7200		7600-8000		8400-8800		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
Differential input slew rate for CK_t - CK_c	S_{RIdiff_CK}	TBD	TBD	TBD	TBD	TBD	TBD	V/ns

Input Clock Jitter Specification

The clock is being driven to the device either by the RCD for L/RDIMM modules, or by the host for U/SODIMM modules.

Figure 212: HOST Driving Clock Signals to the device



Specifications for Input Clock Jitter

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. Input clock violating the min/max jitter values may result in malfunction of the device.

NOTE: For the following tables: BUJ = Bounded Uncorrelated Jitter; DCD = Duty Cycle Distortion; Dj = Deterministic Jitter; Rj = Random Jitter; Tj = Total jitter; pp = Peak-to-Peak

Table 294: Input Clock Jitter Specifications for 3200 to 4800

Parameter	Symbol	3200		3600		4000		4400		4800		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Reference clock frequency	^{t}CK	0.9999 * f0	1.0001 * f0	0.9999 * f0	1.0001 * f0	0.9999 * f0	1.0001 * f0	0.9999 * f0	1.0001 * f0	0.9999 * f0	1.0001 * f0	MHz	1,11
Duty Cycle Error	^{t}CK_Duty_UI_Error_Error	-	0.05	-	0.05	-	0.05	-	0.05		0.05	UI	1,4,11
Rj RMS value of 1-UI Jitter	^{t}CK_1UI_Rj__Error	-	0.0037	-	0.0037	-	0.0037	-	0.0037	-	0.0037	UI (RMS)	3,5,11
Dj pp value of 1-UI Jitter	^{t}CK_1UI_Dj_NoBUJ	-	0.03	-	0.03	-	0.03	-	0.03	-	0.03	UI	3,6,11
Tj value of 1-UI Jitter	^{t}CK_1UI_Tj_NoBUJ	-	0.09	-	0.09	-	0.09	-	0.09	-	0.09	UI	3,6,11
Rj RMS value of N-UI Jitter, where N = 2,3	^{t}CK_NUI_Rj_NoBUJ,where N = 2,3	-	0.004	-	0.004	-	0.004	-	0.004	-	0.004	UI (RMS)	3,7,11
Dj pp value of N-UI Jitter, where N = 2,3	^{t}CK_NUI_Dj_NoBUJ,where N = 2,3	-	0.074	-	0.074	-	0.074	-	0.074	-	0.074	UI	3,7,11
Tj value of N-UI Jitter, where N = 2,3	^{t}CK_NUI_Tj_NoBUJ,where N = 2,3	-	0.140	-	0.140	-	0.140	-	0.140	-	0.140	UI	3,8,11
Rj RMS value of N-UI Jitter, where N = 4,5,6,...,30	^{t}CK_NUI_Rj_NoBUJ,where N = 4,5,6,...,30	-	-	-	-	-	-	-	-	-	-	UI (RMS)	3,9,11, 12
Dj pp value of N-UI Jitter, N = 4,5,6,...,30	^{t}CK_NUI_Dj_NoBUJ,where N = 4,5,6,...,30	-	-	-	-	-	-	-	-	-	-	UI	3,10,11 ,12
Tj value of N-UI Jitter, N = 4,5,6,...,30	^{t}CK_NUI_Tj_NoBUJ,where N = 4,5,6,...,30	-	-	-	-	-	-	-	-	-	-	UI	3,10,11 ,12

Notes: 1. f0 = Data Rate/2, example: if data rate is 3200MT/s, then f0 = 1600

2. Rise and fall time slopes (V/ns) are measured between +100 mV and -100 mV of the differential output of reference clock
3. On-die noise is similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being a device component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specifications is met and another violated in which case the signaling analysis should be run to determine link feasibility.
4. Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.
5. Rj RMS value of 1-UI jitter without BUJ, but on-die system-like noise present. This extraction is to be done after software correction of DCD
6. Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
7. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD
8. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
9. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. This extraction is to be done after software correction of DCD
10. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
11. The validation methodology for these parameters will be covered in future ballots
12. If the clock meets total jitter Tj at BER of $1E^{-16}$, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as Dj + 16.2*Rj for BER of $1E^{-16}$

Table 295: Input Clock Jitter Specifications for 5200 to 6400

Parameter	Symbol	5200		5600		6000		6400		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Reference clock frequency	^{t}CK	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	MHz	1,11
Duty Cycle Error	$^{t}CK\_Duty\_UI\_Error\_Error$	-	TBD	-	TBD	-	TBD		TBD	UI	1,4,11
Rj RMS value of 1-UI Jitter	$^{t}CK\_1UI\_Rj\_Error$	-	TBD	-	TBD	-	TBD		TBD	UI (RMS)	3,5,11
Dj pp value of 1-UI Jitter	$^{t}CK\_1UI\_Dj\_NoBUJ$	-	TBD	-	TBD	-	TBD		TBD	UI	3,6,11
Tj value of 1- UI Jitter	$^{t}CK\_1UI\_Tj\_NoBUJ$	-	TBD	-	TBD	-	TBD		TBD	UI	3,6,11
Rj RMS value of N-UI Jitter, where N = 2,3	$^{t}CK\_NUI\_Rj\_NoBUJ$,where N = 2,3	-	TBD	-	TBD	-	TBD	-	TBD	UI (RMS)	3,7,11
Dj pp value of N-UI Jitter, where N = 2,3	$^{t}CK\_NUI\_Dj\_NoBUJ$,where N = 2,3	-	TBD	-	TBD	-	TBD	-	TBD	UI	3,7,11
Tj value of N-UI Jitter, where N = 2,3	$^{t}CK\_NUI\_Tj\_NoBUJ$,where N = 2,3	-	TBD	-	TBD	-	TBD	-	TBD	UI	3,8,11

Table 295: Input Clock Jitter Specifications for 5200 to 6400 (Continued)

Parameter	Symbol	5200		5600		6000		6400		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Rj RMS value of N-UI Jitter, where N = 4,5,6,...,30	^{t}CK_NUI_Rj_NoBUJ,where N = 4,5,6,...,30	-	-	-	-	-	-	-	-	UI (RMS)	3,9,11,12
Dj pp value of N-UI Jitter, N = 4,5,6,...,30	^{t}CK_NUI_Dj_NoBUJ,where N = 4,5,6,...,30	-	-	-	-	-	-	-	-	UI	3,10,11,12
Tj value of N-UI Jitter, N = 4,5,6,...,30	^{t}CK_NUI_Tj_NoBUJ,where N = 4,5,6,...,30	-	-	-	-	-	-	-	-	UI	3,10,11,12

Notes:
1. f0 = Data Rate/2, example: if data rate is 3200MT/s, then f0 = 1600
2. Rise and fall time slopes (V/ns) are measured between +100 mV and -100 mV of the differential output of reference clock
3. On-die noise is similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being a device component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specifications is met and another violated in which case the signaling analysis should be run to determine link feasibility.
4. Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.
5. Rj RMS value of 1-UI jitter without BUJ, but on-die system-like noise present. This extraction is to be done after software correction of DCD
6. Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
7. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD
8. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
9. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. This extraction is to be done after software correction of DCD
10. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
11. The validation methodology for these parameters will be covered in future ballots
12. If the clock meets total jitter Tj at BER of $1E^{-16}$, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as Dj + 16.2*Rj for BER of $1E^{-16}$

Table 296: Input Clock Jitter Specifications for 6800 to 7600

Parameter	Symbol	6800		7200		7600		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Reference clock frequency	^{t}CK	TBD	TBD	TBD	TBD	TBD	TBD	MHz	1,11
Duty Cycle Error	^{t}CK_Duty_UI_Error_Error	-	TBD	-	TBD	-	TBD	UI	1,4,11

Table 296: Input Clock Jitter Specifications for 6800 to 7600 (Continued)

Parameter	Symbol	6800		7200		7600		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Rj RMS value of 1-UI Jitter	^{t}CK_1UI_Rj__Error	-	TBD	-	TBD	-	TBD	UI (RMS)	3,5,11
Dj pp value of 1-UI Jitter	^{t}CK_1UI_Dj_NoBUJ	-	TBD	-	TBD	-	TBD	UI	3,6,11
Tj value of 1- UI Jitter	^{t}CK_1UI_Tj_NoBUJ	-	TBD	-	TBD	-	TBD	UI	3,6,11
Rj RMS value of N-UI Jitter, where N = 2,3	^{t}CK_NUI_R-j_NoBUJ,where N = 2,3	-	TBD	-	TBD	-	TBD	UI (RMS)	3,7,11
Dj pp value of N-UI Jitter, where N = 2,3	^{t}CK_NUI_D-j_NoBUJ,where N = 2,3	-	TBD	-	TBD	-	TBD	UI	3,7,11
Tj value of N- UI Jitter, where N = 2,3	^{t}CK_NUI_T-j_NoBUJ,where N = 2,3	-	TBD	-	TBD	-	TBD	UI	3,8,11
Rj RMS value of N-UI Jitter, where N = 4,5,6,...,30	^{t}CK_NUI_R-j_NoBUJ,where N = 4,5,6,...,30	-	-	-	-	-	-	UI (RMS)	3,9,11,12
Dj pp value of N-UI Jitter, N = 4,5,6,...,30	^{t}CK_NUI_D-j_NoBUJ,where N = 4,5,6,...,30	-	-	-	-	-	-	UI	3,10,11,12
Tj value of N- UI Jitter, N = 4,5,6,...,30	^{t}CK_NUI_T-j_NoBUJ,where N = 4,5,6,...,30	-	-	-	-	-	-	UI	3,10,11,12

Notes: 1. f0 = Data Rate/2, example: if data rate is 3200MT/s, then f0 = 1600
2. Rise and fall time slopes (V/ns) are measured between +100 mV and -100 mV of the differential output of reference clock
3. On-die noise is similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being a device component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specifications is met and another violated in which case the signaling analysis should be run to determine link feasibility.
4. Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.
5. Rj RMS value of 1-UI jitter without BUJ, but on-die system-like noise present. This extraction is to be done after software correction of DCD
6. Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
7. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD
8. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD

9. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. This extraction is to be done after software correction of DCD
10. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
11. The validation methodology for these parameters will be covered in future ballots
12. If the clock meets total jitter Tj at BER of $1E^{-16}$, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as Dj + 16.2*Rj for BER of $1E^{-16}$

Table 297: Input Clock Jitter Specifications for 8000 to 8800

Parameter	Symbol	8000		8400		8800		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Reference clock frequency	^{t}CK	TBD	TBD	TBD	TBD	TBD	TBD	MHz	1,11
Duty Cycle Error	$^{t}CK\_Duty\_UI\_Error\_Error$	-	TBD	-	TBD	-	TBD	UI	1,4,11
Rj RMS value of 1-UI Jitter	$^{t}CK\_1UI\_Rj\_\_Error$	-	TBD	-	TBD	-	TBD	UI (RMS)	3,5,11
Dj pp value of 1-UI Jitter	$^{t}CK\_1UI\_Dj\_NoBUJ$	-	TBD	-	TBD	-	TBD	UI	3,6,11
Tj value of 1- UI Jitter	$^{t}CK\_1UI\_Tj\_NoBUJ$	-	TBD	-	TBD	-	TBD	UI	3,6,11
Rj RMS value of N-UI Jitter, where N = 2,3	$^{t}CK\_NUI\_Rj\_NoBUJ$,where N = 2,3	-	TBD	-	TBD	-	TBD	UI (RMS)	3,7,11
Dj pp value of N-UI Jitter, where N = 2,3	$^{t}CK\_NUI\_Dj\_NoBUJ$,where N = 2,3	-	TBD	-	TBD	-	TBD	UI	3,7,11
Tj value of N- UI Jitter, where N = 2,3	$^{t}CK\_NUI\_Tj\_NoBUJ$,where N = 2,3	-	TBD	-	TBD	-	TBD	UI	3,8,11
Rj RMS value of N-UI Jitter, where N = 4,5,6,...,30	$^{t}CK\_NUI\_Rj\_NoBUJ$,where N = 4,5,6,...,30	-	TBD	-	TBD	-	TBD	UI (RMS)	3,9,11,12
Dj pp value of N-UI Jitter, N = 4,5,6,...,30	$^{t}CK\_NUI\_Dj\_NoBUJ$,where N = 4,5,6,...,30	-	TBD	-	TBD	-	TBD	UI	3,10,11,12
Tj value of N- UI Jitter, N = 4,5,6,...,30	$^{t}CK\_NUI\_Tj\_NoBUJ$,where N = 4,5,6,...,30	-	TBD	-	TBD	-	TBD	UI	3,10,11,12

Notes: 1. f0 = Data Rate/2, example: if data rate is 3200MT/s, then f0 = 1600
2. Rise and fall time slopes (V/ns) are measured between +100 mV and -100 mV of the differential output of reference clock
3. On-die noise is similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being a device component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be

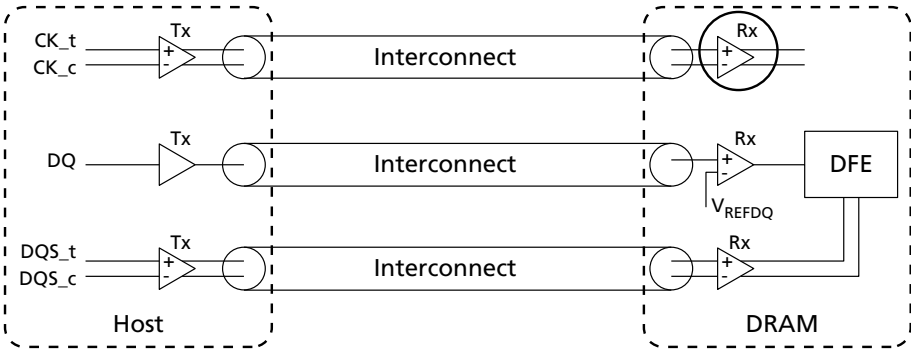
cases when one of Dj and Rj specifications is met and another violated in which case the signaling analysis should be run to determine link feasibility.

4. Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.
5. Rj RMS value of 1-UI jitter without BUJ, but on-die system-like noise present. This extraction is to be done after software correction of DCD
6. Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
7. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD
8. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
9. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. This extraction is to be done after software correction of DCD
10. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
11. The validation methodology for these parameters will be covered in future ballots
12. If the clock meets total jitter Tj at BER of $1E^{-16}$, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as Dj + 16.2*Rj for BER of $1E^{-16}$

Differential Input Clock Voltage Sensitivity

The differential input clock voltage sensitivity test provides the methodology for testing the receiver's sensitivity to clock varying input voltage in the absence of inter-symbol interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise. This specifies the clock input voltage sensitivity requirement.

Figure 213: Device Memory Interconnect Example



Differential Input Clock Voltage Sensitivity Parameter

Differential input clock (CK_t, CK_c) VRx_CK is defined and measured as shown below. These parameters are tested on the CTC2 card.

Table 298: Differential Input Clock Voltage Sensitivity Parameter for 3200 to 4800

Parameter	Symbol	3200		3600		4000		4400		4800		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Minimum input clock voltage sensitivity (differential)	VRx_CK	-	200	-	200	-	180	-	180	-	160	mV	1

Notes: 1. The validation methodology for this parameter will be covered in future ballot(s).

Table 299: Differential Input Clock Voltage Sensitivity Parameter for 5200 to 6400

Parameter	Symbol	5200		5600		6000		6400		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Minimum input clock voltage sensitivity (differential)	VRx_CK	-	140	-	120	-	TBD	-	TBD	mV	1

Notes: 1. The validation methodology for this parameter will be covered in future ballot(s).

Table 300: Differential Input Clock Voltage Sensitivity Parameter for 6800 to 7600

Parameter	Symbol	6800		7200		7600		Unit	Note
		Min	Max	Min	Max	Min	Max		
Minimum input clock voltage sensitivity (differential)	VRx_CK	-	TBD	-	TBD	-	TBD	mV	1

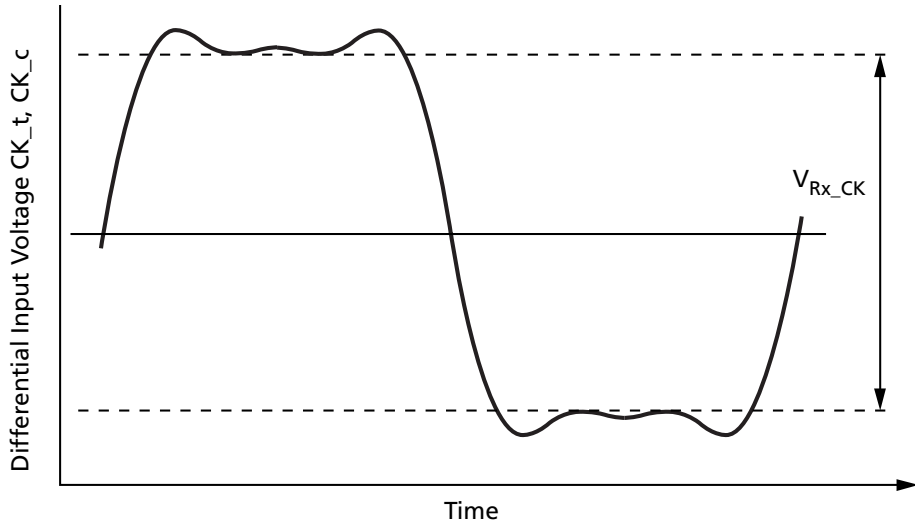
Notes: 1. The validation methodology for this parameter will be covered in future ballot(s).

Table 301: Differential Input Clock Voltage Sensitivity Parameter for 8000 to 8800

Parameter	Symbol	8000		8400		8800		Unit	Note
		Min	Max	Min	Max	Min	Max		
Minimum input clock voltage sensitivity (differential)	VRx_CK	-	TBD	-	TBD	-	TBD	mV	1

Notes: 1. The validation methodology for this parameter will be covered in future ballot(s).

Figure 214: VRx_CK



Differential Input Voltage Levels for DQS

Table 302: Differential Input Levels for DQS (DQS_t, DQS_c) — 3200-6400

Parameter	Symbol	3200-6400	Notes
Differential input high measurement level (DQS_t, DQS_c)	$V_{IH,diff}DQS$	0.75 x $V_{diff,pk-pk}$	1,2,3
Differential input low measurement level (DQS_t, DQS_c)	$V_{IL,diff}DQS$	0.25 x $V_{diff,pk-pk}$	1,2,3

Notes: 1. $V_{diff,pk-pk}$ defined in the following Differential Input Slew Rate Definition for DQS_t, DQS_c figure.
2. $V_{diff,pk-pk}$ is the mean high voltage minus the mean low voltage over TBD samples.
3. All parameters are defined over the entire clock common mode range.

Table 303: Differential Input Levels for DQS (DQS_t, DQS_c) — 6800-8800

Parameter	Symbol	6800-8800	Notes
Differential input high measurement level (DQS_t, DQS_c)	$V_{IH,diff}DQS$	TBD	1,2,3
Differential input low measurement level (DQS_t, DQS_c)	$V_{IL,diff}DQS$	TBD	1,2,3

Notes: 1. $V_{diff,pk-pk}$ defined in the following Differential Input Slew Rate Definition for DQS_t, DQS_c figure.
2. $V_{diff,pk-pk}$ is the mean high voltage minus the mean low voltage over TBD samples.
3. All parameters are defined over the entire clock common mode range.

Differential Input Slew Rate for DQS_t, DQS_c

Input slew rate for differential signals DQS_t, DQS_c are defined and measured as shown below.

Figure 215: Differential Input Slew Rate for DQS_t, DQS_c

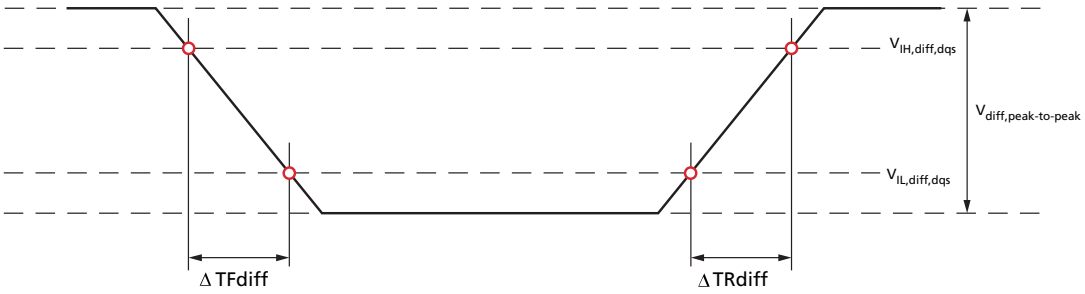


Table 304: Differential Input Slew Rate Definition for DQS_t, DQS_c

Parameter	Measured		Defined By
	From	To	
Differential input slew rate for rising edge (DQS_t - DQS_c)	$V_{IL,diff}DQS$	$V_{IH,diff}DQS$	$\lvert(V_{IL,diff}DQS - V_{IH,diff}DQS)\rvert$ / $deltaTR_{diff}$
Differential input slew rate for falling edge (DQS_t - DQS_c)	$V_{IH,diff}DQS$	$V_{IL,diff}DQS$	($V_{IH\ ,diff}DQS$ - $V_{IL,diff}DQS$) / $deltaTF_{diff}$

Table 305: Differential Input Slew Rate for DQS_t, DQS_c — 3200-7200

Parameter	Symbol	3200-4800		5200-6400		6800-7200		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
Differential input slew rate for rising edge (DQS_t - DQS_c)	S_{RIdiff_DQS}	TBD	TBD	TBD	TBD	TBD	TBD	V/ns

Notes: 1. Applies only when both DQS_t and DQS_c are transitioning.

Table 306: Differential Input Slew Rate for DQS_t, DQS_c — 8000-8800

Parameter	Symbol	7600-8000		8400-8800		Unit
		MIN	MAX	MIN	MAX	
Differential input slew rate for rising edge (DQS_t - DQS_c)	S_{RIdiff_DQS}	TBD	TBD	TBD	TBD	V/ns

Notes: 1. Applies only when both DQS_t and DQS_c are transitioning.

Rx DQS Jitter Sensitivity

The receiver strobe jitter sensitivity test provides the methodology for testing the receiver's strobe sensitivity to an applied duty cycle distortion (DCD) and/or random jitter (Rj) at the forwarded strobe input without adding jitter, noise and ISI to the data. The receiver must pass the appropriate BER rate when no crosstalk or ISI is applied and it must pass through the combination of applied DCD and Rj.

Specifications

The following tables provide Rx DQS jitter sensitivity specifications for the receivers when operating at various transfer rates. These parameters are tested on the CTC2 card without Rx equalization set. Additive DFE Gain Bias can be set.

Also note:

- BER = bit error rate; DCD = duty cycle distortion; Rj = random jitter
- Validation methodology will be defined in future ballots. 2UI is defined ast 1^{t}CK for the parameters.
- All measurements at BER=$1E^{-9}$.
- The test should be done after the DQS and DQ voltage sensitivity tests are complete and passing.
- Voltage swings and slew rates for strobe and DQ signals can be set as long as they meet specifications. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

Table 307: Rx DQS Jitter Sensitivity — 3200-4800

Parameter	Symbol	3200		3600		4000		4400		4800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
DQ timing width	^{t}RX_DQ_tMargin	0.900	-	0.875	-	0.825	-	0.825	-	0.825	-	UI	1,2

Table 307: Rx DQS Jitter Sensitivity — 3200-4800

Parameter	Symbol	3200		3600		4000		4400		4800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Degradation of timing width compared to tRX_DQ_tMargin with DCD injection in DQS	$^{\Delta t}$RX_DQ_t-Margin_D-QS_DCD	-	0.060	-	0.060	-	0.060	-	0.060	-	0.060	UI	3
Degradation of timing width compared to tRX_DQ_tMargin with Rj injection in DQS	$^{\Delta t}$RX_DQ_t-Margin_D-QS_Rj	-	0.090	-	0.090	-	0.090	-	0.090	-	0.090	UI	4
Degradation of timing width compared to tRX_DQ_tMargin with DCD and Rj injection in DQS	$^{\Delta t}$RX_DQ_t-Margin_D-QS_DCD_Rj	-	0.150	-	0.150	-	0.150	-	0.150	-	0.150	UI	1,5
Delay of any data lane relative to DQS_t/DQS_c crossing	tRx_DQS2DQ	1	3	1	3	1	3	1	3.25	1	3.5	UI	6

Notes: 1. Each of $^{\Delta t}$Rx_DQ_tMargin_DQS_DCD, $^{\Delta t}$Rx_DQ_tMargin_DQS_Rj, and $^{\Delta t}$Rx_DQ_tMargin_DQS_DCD_Rj can be relaxed by up to 5% if tRx_DQ_tMargin exceeds the spec by 5% or more.
2. DQ timing width: timing width for any data lane using repetitive patterns (check note 3 for the pattern) measured at BER=1E^{-9}.
3. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded strobe DQS compared to tRx_DQ_tMargin, measured at BER=1E^{-9}. The magnitude of DCD is specified in Test Conditions for Rx DQS Jitter Sensitivity Testing. Test using clock-like pattern of repeating three 1s and three 0s.
4. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded strobe DQS measured at BER=1E^{-9}, compared to tRx_DQ_tMargin. The magnitude of Rj is specified in Test Conditions for Rx DQS Jitter Sensitivity Testing.
5. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded strobe DQS measured at BER=1E^{-9}, compared to tRx_DQ_tMargin. The magnitudes of DCD and Rj are specified in Test Conditions for Rx DQS Jitter Sensitivity Testing.

6. Delay of any data lane relative to the strobe lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.

Table 308: Rx DQS Jitter Sensitivity — 5200-6400

Parameter	Symbol	5200		5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
DQ timing width	^{t}RX_DQ_tMargin	0.835	-	0.835	-	TBD	-	TBD	-	UI	1,2
Degradation of timing width compared to ^{t}RX_DQ_tMargin with DCD injection in DQS	$^{\Delta t}$RX_DQ_tMargin_DQS_DCD	-	0.06	-	0.06	-	TBD	-	TBD	UI	3
Degradation of timing width compared to ^{t}RX_DQ_tMargin with Rj injection in DQS	$^{\Delta t}$RX_DQ_tMargin_DQS_Rj	-	0.09	-	0.09	-	TBD	-	TBD	UI	4
Degradation of timing width compared to ^{t}RX_DQ_tMargin with DCD and Rj injection in DQS	$^{\Delta t}$RX_DQ_tMargin_DQS_DCD_Rj	-	0.15	-	0.15	-	TBD	-	TBD	UI	1,5
Delay of any data lane relative to DQS_t/DQS_c crossing	^{t}Rx_DQS2DQ	1	3.75	1	4.00	TBD	TBD	TBD	TBD	UI	6

Notes: 1. Each of $^{\Delta t}$Rx_DQ_tMargin_DQS_DCD, $^{\Delta t}$Rx_DQ_tMargin_DQS_Rj, and $^{\Delta t}$Rx_DQ_tMargin_DQS_DCD_Rj can be relaxed by up to 5% if ^{t}Rx_DQ_tMargin exceeds the spec by 5% or more.
2. DQ timing width: timing width for any data lane using repetitive patterns (check note 3 for the pattern) measured at BER=E-9.
3. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded strobe DQS compared to ^{t}Rx_DQ_tMargin, measured at BER=E-9. The magnitude of DCD is specified in Test Conditions for Rx DQS Jitter Sensitivity Testing. Test using clock-like pattern of repeating three 1s and three 0s.
4. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded strobe DQS measured at BER=E-9, compared to ^{t}Rx_DQ_tMargin. The magnitude of Rj is specified in Test Conditions for Rx DQS Jitter Sensitivity Testing.
5. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded strobe DQS measured at BER=E-9, compared to ^{t}Rx_DQ_tMargin. The magnitudes of DCD and Rj are specified in Test Conditions for Rx DQS Jitter Sensitivity Testing.

6. Delay of any data lane relative to the strobe lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.

Table 309: Rx DQS Jitter Sensitivity — 6800-7600

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQ timing width	^{t}RX_DQ_tMargin	TBD	-	TBD	-	TBD	-	UI	1,2
Degradation of timing width compared to ^{t}RX_DQ_tMargin with DCD injection in DQS	$^{\Delta t}$RX_DQ_tMargin_DQS_DCD	-	TBD	-	TBD	-	TBD	UI	3
Degradation of timing width compared to ^{t}RX_DQ_tMargin with Rj injection in DQS	$^{\Delta t}$RX_DQ_tMargin_DQS_Rj	-	TBD	-	TBD	-	TBD	UI	4
Degradation of timing width compared to ^{t}RX_DQ_tMargin with DCD and Rj injection in DQS	$^{\Delta t}$RX_DQ_tMargin_DQS_DCD_Rj	-	TBD	-	TBD	-	TBD	UI	1,5
Delay of any data lane relative to DQS_t/DQS_c crossing	^{t}Rx_DQS2DQ	TBD	TBD	TBD	TBD	TBD	TBD	TBD	6

Notes: 1. Each of $^{\Delta t}$Rx_DQ_tMargin_DQS_DCD, $^{\Delta t}$Rx_DQ_tMargin_DQS_Rj, and $^{\Delta t}$Rx_DQ_tMargin_DQS_DCD_Rj can be relaxed by up to 5% if ^{t}Rx_DQ_tMargin exceeds the spec by 5% or more.
2. DQ timing width: timing width for any data lane using repetitive patterns (check note 3 for the pattern) measured at BER=E-9.
3. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded strobe DQS compared to ^{t}Rx_DQ_tMargin, measured at BER=E-9. The magnitude of DCD is specified in Test Conditions for Rx DQS Jitter Sensitivity Testing. Test using clock-like pattern of repeating three 1s and three 0s.
4. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded strobe DQS measured at BER=E-9, compared to ^{t}Rx_DQ_tMargin. The magnitude of Rj is specified in Test Conditions for Rx DQS Jitter Sensitivity Testing.
5. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded strobe DQS measured at BER=E-9, compared to ^{t}Rx_DQ_tMargin. The magnitudes of DCD and Rj are specified in Test Conditions for Rx DQS Jitter Sensitivity Testing.

6. Delay of any data lane relative to the strobe lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.

Table 310: Rx DQS Jitter Sensitivity — 8000-8800

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQ timing width	^{t}RX_DQ_tMargin	TBD	-	TBD	-	TBD	-	UI	1,2
Degradation of timing width compared to ^{t}RX_DQ_tMargin with DCD injection in DQS	$^{\Delta t}$RX_DQ_tMargin_DQS_DCD	-	TBD	-	TBD	-	TBD	UI	3
Degradation of timing width compared to ^{t}RX_DQ_tMargin with Rj injection in DQS	$^{\Delta t}$RX_DQ_tMargin_DQS_Rj	-	TBD	-	TBD	-	TBD	UI	4
Degradation of timing width compared to ^{t}RX_DQ_tMargin with DCD and Rj injection in DQS	$^{\Delta t}$RX_DQ_tMargin_DQS_DCD_Rj	-	TBD	-	TBD	-	TBD	UI	1,5
Delay of any data lane relative to DQS_t/DQS_c crossing	^{t}Rx_DQS2DQ	TBD	TBD	TBD	TBD	TBD	TBD	TBD	6

Notes: 1. Each of $^{?t}$Rx_DQ_tMargin_DQS_DCD, $^{?t}$Rx_DQ_tMargin_DQS_Rj, and $^{?t}$Rx_DQ_tMargin_DQS_DCD_Rj can be relaxed by up to 5% if ^{t}Rx_DQ_tMargin exceeds the spec by 5% or more.
2. DQ timing width: timing width for any data lane using repetitive patterns (check note 3 for the pattern) measured at BER=E-9.
3. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded strobe DQS compared to ^{t}Rx_DQ_tMargin, measured at BER=E-9. The magnitude of DCD is specified in Test Conditions for Rx DQS Jitter Sensitivity Testing. Test using clock-like pattern of repeating three 1s and three 0s.
4. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded strobe DQS measured at BER=E-9, compared to ^{t}Rx_DQ_tMargin. The magnitude of Rj is specified in Test Conditions for Rx DQS Jitter Sensitivity Testing.
5. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded strobe DQS measured at BER=E-9, compared to ^{t}Rx_DQ_tMargin. The magnitudes of DCD and Rj are specified in Test Conditions for Rx DQS Jitter Sensitivity Testing.
6. Delay of any data lane relative to the strobe lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.

Test Conditions

The following table lists the amount of duty cycle distortion (DCD) and/or random jitter (Rj) that must be applied to the forwarded strobe when measuring the Rx strobe jitter sensitivity parameters specified in the previous tables. Also note:

- While imposing these specifications, the strobe lane is stressed, but the data input is kept large amplitude and no jitter or ISI injection. The specified voltages are at the Rx input pin. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.
- The jitter response of the forwarded strobe channel depends on the input voltage, primarily due to bandwidth limitations of the clock receiver. For this revision, no separate specification of jitter as a function of input amplitude is specified; instead, the response characterization is done at the specified clock amplitude only. The specified voltages are at the Rx input pin.
- Although the device has bursty traffic, current available BERTs that can be used for this test do not support burst traffic patterns. A continuous strobe and continuous DQ are used for this parameter. The clock-like pattern repeating three 1s and three 0s is used for this test.
- Voltage swing and slew rates can be set for strobe and DQ signals as long as they meet the specification. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

Table 311: Test Conditions for Rx DQS Jitter Sensitivity Testing — 3200-4800

Parameter	Symbol	3200		3600		4000		4400		4800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Applied DCD to the DQS	^{t}RX_DQS_DCD	-	0.0045	-	0.0045	-	0.0045	-	0.0045	-	0.0045	UI	1,4
Applied to Rj RMS to the DQS	^{t}RX_DQS_Rj	-	0.0075	-	0.0075	-	0.0075	-	0.0075	-	0.0075	UI (RMS)	2,5
Applied DCD and Rj RMS to the DQS	^{t}RX_DQS_DCD_Rj	-	0.045 UI DCD + 0.0075 UI Rj RMS	-	0.045 UI DCD + 0.0075 UI Rj RMS	-	0.045 UI DCD + 0.0075 UI Rj RMS	-	0.045 UI DCD + 0.0075 UI Rj RMS	-	0.045 UI DCD + 0.0075 UI Rj RMS	UI	3,4,6

Notes: 1. Various DCD values should be tested, complying within the maximum limits.
2. Various Rj values should be tested, complying within the maximum limits.
3. Various combinations of DCD and Rj values should be tested, complying within the maximum limits. The maximum timing margin degradation as a result of the injected jitter is specified in a separate table.
4. Duty cycle distortion (in UI DCD) as applied to the input forwarded DQS from BERT (UI).
5. RMS value of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI).
6. Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI).

7. Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI).

Table 312: Test Conditions for Rx DQS Jitter Sensitivity Testing — 5200-6400

Parameter	Symbol	5200		5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Applied DCD to the DQS	^{t}RX_DQS_DCD	-	TBD	-	TBD	-	TBD	-	TBD	UI	1,4
Applied to Rj RMS to the DQS	^{t}RX_DQS_Rj	-	TBD	-	TBD	-	TBD	-	TBD	UI (RMS)	2,5
Applied DCD and Rj RMS to the DQS	^{t}RX_DQS_DC-D_Rj	-	TBD	-	TBD	-	TBD	-	TBD	UI	3,4,6

Notes: 1. Various DCD values should be tested, complying within the maximum limits.
2. Various Rj values should be tested, complying within the maximum limits.
3. Various combinations of DCD and Rj values should be tested, complying within the maximum limits. The maximum timing margin degradation as a result of the injected jitter is specified in a separate table.
4. Duty cycle distortion (in UI DCD) as applied to the input forwarded DQS from BERT (UI).
5. RMS value of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI).
6. Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI).
7. Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI).

Table 313: Test Conditions for Rx Strobe Jitter Sensitivity Testing — 6800-7600

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Applied DCD to the DQS	^{t}RX_DQS_DCD	-	TBD	-	TBD	-	TBD	UI	1,4
Applied to Rj RMS to the DQS	^{t}RX_DQS_Rj	-	TBD	-	TBD	-	TBD	UI (RMS)	2,5
Applied DCD and Rj RMS to the DQS	^{t}RX_DQS_DCD_Rj	-	TBD	-	TBD	-	TBD	UI	3,4,6

Notes: 1. Various DCD values should be tested, complying within the maximum limits.
2. Various Rj values should be tested, complying within the maximum limits.
3. Various combinations of DCD and Rj values should be tested, complying within the maximum limits. The maximum timing margin degradation as a result of the injected jitter is specified in a separate table.
4. Duty cycle distortion (in UI DCD) as applied to the input forwarded DQS from BERT (UI).
5. RMS value of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI).
6. Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI).

7. Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI).

Table 314: Test Conditions for Rx Strobe Jitter Sensitivity Testing — 8000-8800

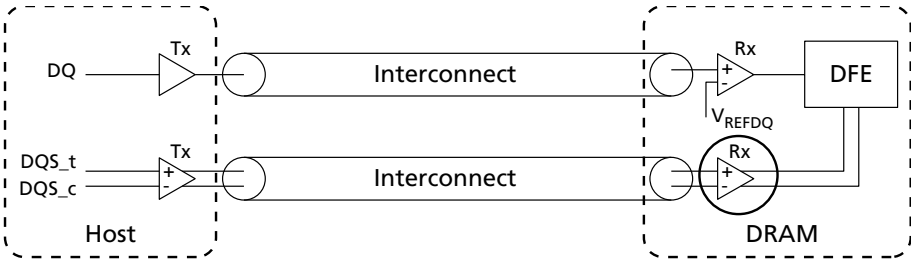
Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Applied DCD to the DQS	^{t}RX_DQS_DCD	-	TBD	-	TBD	-	TBD	UI	1,4
Applied to Rj RMS to the DQS	^{t}RX_DQS_Rj	-	TBD	-	TBD	-	TBD	UI (RMS)	2,5
Applied DCD and Rj RMS to the DQS	^{t}RX_DQS_DCD_Rj	-	TBD	-	TBD	-	TBD	UI	3,4,6

Notes: 1. Various DCD values should be tested, complying within the maximum limits.
2. Various Rj values should be tested, complying within the maximum limits.
3. Various combinations of DCD and Rj values should be tested, complying within the maximum limits. The maximum timing margin degradation as a result of the injected jitter is specified in a separate table.
4. Duty cycle distortion (in UI DCD) as applied to the input forwarded DQS from BERT (UI).
5. RMS value of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI).
6. Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI).
7. Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI).

Rx DQS Voltage Sensitivity

The receiver strobe input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of inter-symbol interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

Figure 216: Example of DDR5 Memory Interconnect



Receiver Strobe Voltage Sensitivity Parameters

The table below shows how input differential (DQS_t, DQS_c) V_{Rx_DQS} is defined and measured. The receiver must pass the minimum BER requirements for the device. These parameters are tested on the CTC2 card with neither additive gain nor Rx equalization set.

Table 315: Rx DQS Input Voltage Sensitivity Parameter — 3200-4800

Parameter	Symbol	3200		3600		4000		4400		4800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Minimum DQS Rx input voltage sensitivity (differential)	V_{Rx_DQS}	-	130	-	115	-	105	-	100	-	100	mV	1, 2, 3

Notes: 1. Refer to the minimum BER requirements for DDR5.
2. The validation methodology for this parameter will be covered in future ballot(s).
3. Test using clock-like pattern of repeating three 1s and three 0s

Table 316: Rx DQS Input Voltage Sensitivity Parameter — 5200-6400

Parameter	Symbol	5200		5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Minimum DQS Rx input voltage sensitivity (differential)	V_{Rx_DQS}	-	90	-	90	-	TBD	-	TBD	mV	1, 2, 3

Notes: 1. Refer to the minimum BER requirements for DDR5.
2. The validation methodology for this parameter will be covered in future ballot(s).
3. Test using clock-like pattern of repeating three 1s and three 0s

Table 317: Rx DQS Input Voltage Sensitivity Parameter — 6800-7600

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum DQS Rx input voltage sensitivity (differential)	V_{Rx_DQS}	-	TBD	-	TBD	-	TBD	mV	1, 2, 3

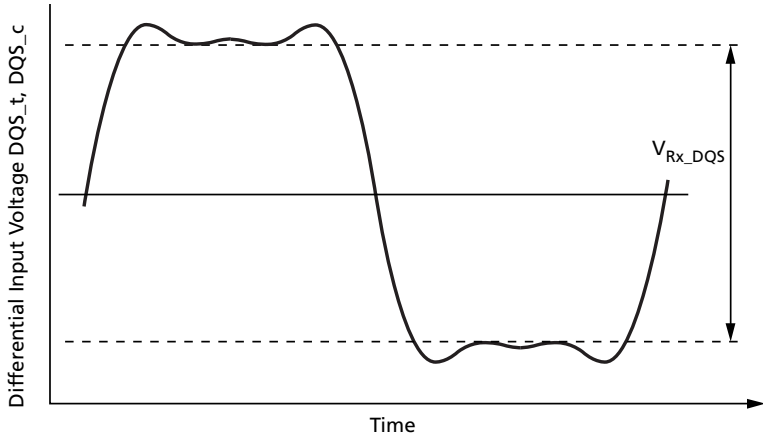
Notes: 1. Refer to the minimum BER requirements for DDR5.
2. The validation methodology for this parameter will be covered in future ballot(s).
3. Test using clock-like pattern of repeating three 1s and three 0s

Table 318: Rx DQS Input Voltage Sensitivity Parameter — 8000-8800

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum DQS Rx input voltage sensitivity (differential)	V_{Rx_DQS}	-	TBD	-	TBD	-	TBD	mV	1, 2, 3

Notes: 1. Refer to the minimum BER requirements for DDR5.
2. The validation methodology for this parameter will be covered in future ballot(s).
3. Test using clock-like pattern of repeating three 1s and three 0s

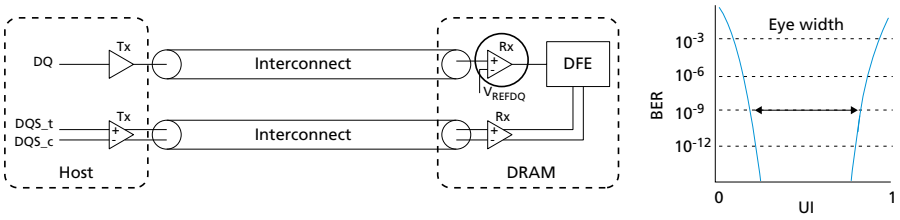
Figure 217: V_{Rx_DQS}



Rx DQ Voltage Sensitivity

The receiver data input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of inter-symbol interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

Figure 218: Example of DDR5 Memory Interconnect



Receiver DQ Input Voltage Sensitivity Parameters

Input single-ended V_{Rx_DQ} is defined and measured as shown below. The receiver must pass the minimum BER requirements for DDR5. These parameters are tested on the CTC2 card with neither additive gain nor Rx Equalization set.

Table 319: Rx DQ Input Voltage Sensitivity Parameter for DDR5 3200-4800

Parameter	Symbol	3200		3600		4000		4400		4800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Minimum DQ Rx input voltage sensitivity applied around V_{REF}	V_{Rx_DQ}	-	85	-	75	-	70	-	65	-	65	mV	1, 2, 3

Notes: 1. Refer to the minimum BER requirements for DDR5.
2. The validation methodology for this parameter will be covered in future ballot(s).

3. Test using clock-like pattern of repeating three 1s and three 0s

Table 320: Rx DQ Input Voltage Sensitivity Parameter for DDR5 5200-6400

Parameter	Symbol	5200		5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Minimum DQ Rx input voltage sensitivity applied around V_{REF}	V_{Rx_DQ}	-	60	-	60	-	TBD	-	TBD	mV	1, 2, 3

Notes: 1. Refer to the minimum BER requirements for DDR5.
2. The validation methodology for this parameter will be covered in future ballot(s).
3. Test using clock-like pattern of repeating three 1s and three 0s

Table 321: Rx Strobe Input Voltage Sensitivity Parameter for DDR5 6800-7600

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum DQ Rx input voltage sensitivity applied around V_{REF}	V_{Rx_DQS}	-	TBD	-	TBD	-	TBD	mV	1, 2, 3

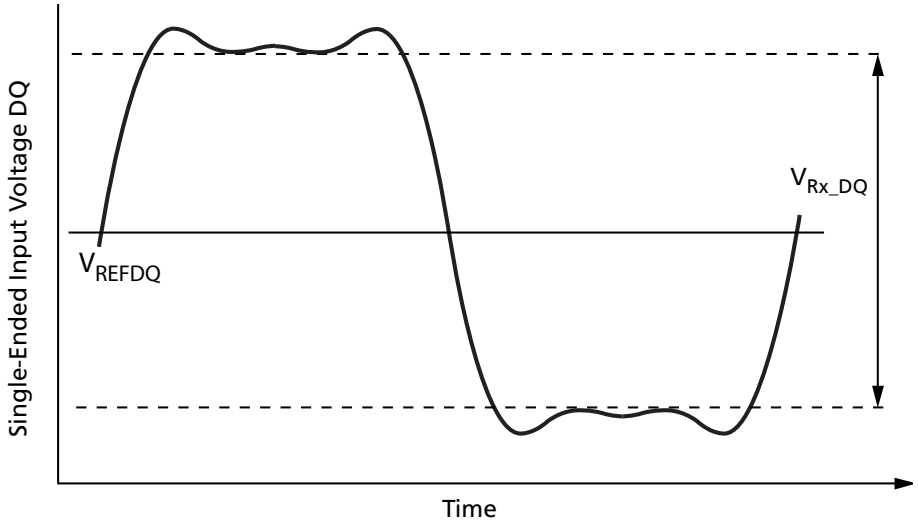
Notes: 1. Refer to the minimum BER requirements for DDR5.
2. The validation methodology for this parameter will be covered in future ballot(s).
3. Test using clock-like pattern of repeating three 1s and three 0s

Table 322: Rx Strobe Input Voltage Sensitivity Parameter for DDR5 8000-8800

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum DQ Rx input voltage sensitivity applied around V_{REF}	V_{Rx_DQS}	-	TBD	-	TBD	-	TBD	mV	1, 2, 3

Notes: 1. Refer to the minimum BER requirements for DDR5.
2. The validation methodology for this parameter will be covered in future ballot(s).
3. Test using clock-like pattern of repeating three 1s and three 0s

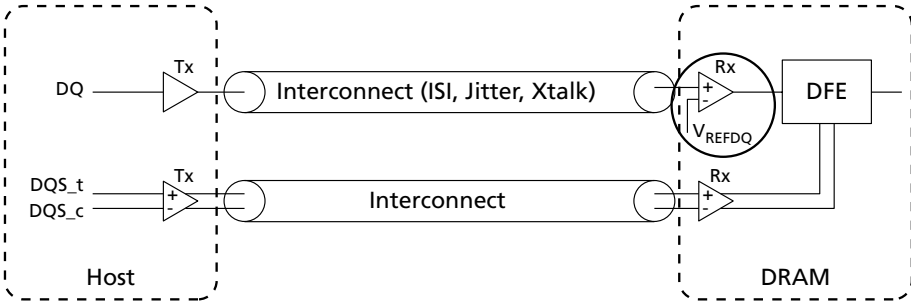
Figure 219: V_{Rx_DQS}



Rx Stressed Eye

The stressed eye tests provide a methodology for creating the appropriate stress for the device's receiver with the combination of ISI (both loss and reflective), jitter (Rj, Dj, DCD), and crosstalk noise. The receiver must pass the appropriate BER rate when the equivalent stressed eye is applied through the combination of ISI, jitter and crosstalk.

Figure 220: Example: RX Stressed Test Setup in the Presence of ISI, Jitter and Crosstalk



Parameters

In the following tables, BER = bit error rate, DCD = duty cycle distortion, Rj = random jitter, Sj = sinusoidal jitter, p-p = peak to peak.

Table 323: Test Conditions for Rx Stressed Eye Tests for DDR5 3200-4800

Parameter	Symbol	3200		3600		4000		4400		4800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Eye height of stressed eye for golden reference channel 1	RxEH_Stressed_Eye_Golden_Ref_Channel_1	-	95	-	85	-	80	-	75	-	70	mV	1,2,3,4,5,6,7,8,9

Table 323: Test Conditions for Rx Stressed Eye Tests for DDR5 3200-4800 (Continued)

Parameter	Symbol	3200		3600		4000		4400		4800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Eye width of stressed eye golden reference channel 1	RxEW_Stressed_Eye_Golden_Ref_Channel_1	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	UI	1,2,3,4,5,6,7,8,9
Vswing stress to meet above data eye	Vswing_Stressed_Eye_Golden_Ref_Channel_1	-	600	-	600	-	600	-	600	-	600	mV	1,2
Injected sinusoidal jitter at 200 MHz to meet above data eye	Sj_Stressed_Eye_Golden_Ref_Channel_1	0	0.45	0	0.45	0	0.45	0	0.45	0	0.45	UI p-p	1,2
Injected random wide band (10 MHz-1 GHz) jitter to meet above data eye	Rj_Stressed_Eye_Golden_Ref_Channel_1	0	0.04	0	0.04	0	0.04	0	0.04	0	0.04	UI RMS	1,2
Injected voltage noise as PRBS23, or injected voltage noise at 2.1 GHz	Vnoise_Stressed_Eye_Golden_Ref_Channel_1	0	125	0	125	0	125	0	125	0	125	mV p-p	1,2
Golden reference channel 1 characteristics as measured at TBD	Golden_Ref_Channel_1_Characteristics	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	3

Notes:
1. Must meet minimum BER of IE^{-16} or better requirements with the stressed eye at the slicer of the receiver (after equalization is applied in the summer). The eye shape is verified by measuring to BER $1E^{-9}$ and extrapolating to BER $1E^{-16}$.
2. These parameters are applied on the defined golden reference channel with parameters TBD.
3. DFE tap 1-4 bias settings that give the best eye margin are used and referr to the values in the DFE Tap Coefficients MIN/MAX Ranges table. DFE tap range limits apply: sum of absolute values of Tap-2, Tap-3, and Tap-4 should be less than 60mV (|Tap-2| + |Tap-3| + |Tap-4| < 60mV) after the tap multiplier is applied.
4. Evaluated with no DC supply voltage drift.
5. Evaluated with no temperature drift.
6. Supply voltage noise limited according to DC bandwidth specifications (see DC Operating Conditions).
7. The stressed eye is assumed to have a diamond shape.
8. For this test, the following can be adjusted as needed without exceeding the specifications, including the limits described in note 1: V_{REFDQ}, DFE gain bias step, and DFE Taps 1, 2, 3, 4 bias step.
9. The stressed eye is defined as centered on the DQS_t/DQS_c crossing during the calibration. Measurement includes an optimal set of DQS_t/DQS_c location, V_{REFDQ}, and DFE solution to give the best eye margin.
10. The Rx stressed eye specification applies at 2933 and faster data rates.

11. EH/EW are measured at the slicer of the receiver.

Table 324: Test Conditions for Rx Stressed Eye Tests for DDR5 5200-6400

Parameter	Symbol	5200		5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Eye height of stressed eye for golden reference channel 1	RxEH_Stressed_Eye_Golden_Ref_Channel_1	-	65	-	60	-	TBD	-	TBD	mV	1,2,3,4,5,6,7,8,9
Eye width of stressed eye golden reference channel 1	RxEW_Stressed_Eye_Golden_Ref_Channel_1	-	0.235	-	0.235	-	TBD	-	TBD	UI	1,2,3,4,5,6,7,8,9
Vswing stress to meet above data eye	Vswing_Stressed_Eye_Golden_Ref_Channel_1	-	600	-	600	-	TBD	-	TBD	mV	1,2
Injected sinusoidal jitter at 200 MHz to meet above data eye	Sj_Stressed_Eye_Golden_Ref_Channel_1	-	0.45	-	0.45	TBD	TBD	TBD	TBD	UI p-p	1,2
Injected random wide band (10 MHz-1 GHz) jitter to meet above data eye	Rj_Stressed_Eye_Golden_Ref_Channel_1	-	0.04	-	0.04	TBD	TBD	TBD	TBD	UI RMS	1,2
Injected voltage noise as PRBS23, or injected voltage noise at 2.1 GHz	Vnoise_Stressed_Eye_Golden_Ref_Channel_1	-	125	-	125	TBD	TBD	TBD	TBD	mV p-p	1,2
Golden reference channel 1 characteristics as measured at TBD	Golden_Ref_Channel_1_Characteristics	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	3

Notes: 1. Must meet minimum BER of IE^{-16} or better requirements with the stressed eye at the slicer of the receiver (after equalization is applied in the summer). The eye shape is verified by measuring to BER $1E^{-9}$ and extrapolating to BER $1E^{-16}$.
2. These parameters are applied on the defined golden reference channel with parameters TBD.
3. DFE tap 1-4 bias settings that give the best eye margin are used and refer to the values in the DFE Tap Coefficients MIN/MAX Ranges table. DFE tap range limits apply: sum of absolute values of Tap-2, Tap-3, and Tap-4 should be less than 60mV (|Tap-2| + |Tap-3| + |Tap-4| < 60mV) after the tap multiplier is applied.
4. Evaluated with no DC supply voltage drift.
5. Evaluated with no temperature drift.
6. Supply voltage noise limited according to DC bandwidth specifications (see DC Operating Conditions).
7. The stressed eye is assumed to have a diamond shape.
8. For this test, the following can be adjusted as needed without exceeding the specifications, including the limits described in note 1: V_{REFDQ}, DFE gain bias step, and DFE Taps 1, 2, 3, 4 bias step.

9. The stressed eye is defined as centered on the DQS_t/DQS_c crossing during the calibration. Measurement includes an optimal set of DQS_t/DQS_c location, V_{REFDQ}, and DFE solution to give the best eye margin.
10. The Rx stressed eye specification applies at 2933 and faster data rates.
11. EH/EW are measured at the slicer of the receiver.

Table 325: Test Conditions for Rx Stressed Eye Tests for DDR5 6800-7600

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Eye height of stressed eye for golden reference channel 1	RxE-H_Stressed_Eye_-Golden_Ref_Channel_1	-	TBD	-	TBD	-	TBD	mV	1,2,3,4,5,6,7,8,9
Eye width of stressed eye golden reference channel 1	RxEW_Stressed_Eye_Golden_Ref_Chan-nel_1	-	TBD	-	TBD	-	TBD	UI	2,3,4,5,6,7,8
Vswing stress to meet above data eye	Vswing_Stressed_Eye_Gold-en_Ref_Channel_1	-	TBD	-	TBD	-	TBD	mV	1,2
Injected sinusoidal jitter at 200 MHz to meet above data eye	Sj_Stressed_Eye_-Golden_Ref_Chan-nel_1	TBD	TBD	TBD	TBD	TBD	TBD	UI p-p	1,2
Injected random wide band (10 MHz-1 GHz) jitter to meet above data eye	Rj_Stressed_Eye_-Golden_Ref_Chan-nel_1	TBD	TBD	TBD	TBD	TBD	TBD	UI RMS	1,2
Injected voltage noise as PRBS23, or injected voltage noise at 2.1 GHz	Vnoise_Stressed_Eye_Gold-en_Ref_Channel_1	TBD	TBD	TBD	TBD	TBD	TBD	mV p-p	1,2
Golden reference channel 1 characteristics as measured at TBD	Golden_Ref_Chan-nel_1_Characteris-tics	TBD	TBD	TBD	TBD	TBD	TBD	TBD	3

Notes: 1. Must meet minimum BER of IE^{-16} or better requirements with the stressed eye at the slicer of the receiver (after equalization is applied in the summer). The eye shape is verified by measuring to BER $1E^{-9}$ and extrapolating to BER $1E^{-16}$.
2. These parameters are applied on the defined golden reference channel with parameters TBD.
3. DFE tap 1-4 bias settings that give the best eye margin are used and refer to the values in the DFE Tap Coefficients MIN/MAX Ranges table. DFE tap range limits apply: sum of absolute values of Tap-2, Tap-3, and Tap-4 should be less than 60mV (|Tap-2| + |Tap-3| + |Tap-4| < 60mV) after the tap multiplier is applied.
4. Evaluated with no DC supply voltage drift.
5. Evaluated with no temperature drift.
6. Supply voltage noise limited according to DC bandwidth specifications (see DC Operating Conditions).
7. The stressed eye is assumed to have a diamond shape.
8. For this test, the following can be adjusted as needed without exceeding the specifications, including the limits described in note 1: V_{REFDQ}, DFE gain bias step, and DFE Taps 1, 2, 3, 4 bias step.
9. The stressed eye is defined as centered on the DQS_t/DQS_c crossing during the calibration. Measurement includes an optimal set of DQS_t/DQS_c location, V_{REFDQ} and DFE solution to give the best eye margin..
10. The Rx stressed eye specification applies at 2933 and faster data rates.

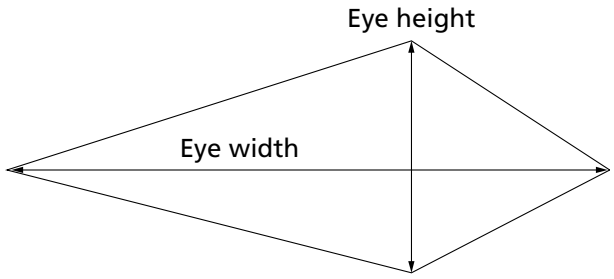
11. EH/EW are measured at the slicer of the receiver.

Table 326: Test Conditions for Rx Stressed Eye Tests for DDR5 8000-8800

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Eye height of stressed eye for golden reference channel 1	RxEH_Stressed_Eye_Golden_Ref_Channel_1	-	TBD	-	TBD	-	TBD	mV	1,2,3,4,5,6,7,8,9
Eye width of stressed eye golden reference channel 1	RxEW_Stressed_Eye_Golden_Ref_Channel_1	-	TBD	-	TBD	-	TBD	UI	2,3,4,5,6,7,8
Vswing stress to meet above data eye	Vswing_Stressed_Eye_Golden_Ref_Channel_1	-	TBD	-	TBD	-	TBD	mV	1,2
Injected sinusoidal jitter at 200 MHz to meet above data eye	Sj_Stressed_Eye_Golden_Ref_Channel_1	TBD	TBD	TBD	TBD	TBD	TBD	UI p-p	1,2
Injected random wide band (10 MHz-1 GHz) jitter to meet above data eye	Rj_Stressed_Eye_Golden_Ref_Channel_1	TBD	TBD	TBD	TBD	TBD	TBD	UI RMS	1,2
Injected voltage noise as PRBS23, or injected voltage noise at 2.1 GHz	Vnoise_Stressed_Eye_Golden_Ref_Channel_1	TBD	TBD	TBD	TBD	TBD	TBD	mV p-p	1,2
Golden reference channel 1 characteristics as measured at TBD	Golden_Ref_Channel_1_Characteristics	TBD	TBD	TBD	TBD	TBD	TBD	TBD	3

Notes: 1. Must meet minimum BER of IE^{-16} or better requirements with the stressed eye at the slicer of the receiver (after equalization is applied in the summer). The eye shape is verified by measuring to BER $1E^{-9}$ and extrapolating to BER $1E^{-16}$.
2. These parameters are applied on the defined golden reference channel with parameters TBD.
3. DFE tap 1-4 bias settings that give the best eye margin are used and refer to the values in the DFE Tap Coefficients MIN/MAX Ranges table. DFE tap range limits apply: sum of absolute values of Tap-2, Tap-3, and Tap-4 should be less than 60mV (|Tap-2| + |Tap-3| + |Tap-4| < 60mV) after the tap multiplier is applied.
4. Evaluated with no DC supply voltage drift.
5. Evaluated with no temperature drift.
6. Supply voltage noise limited according to DC bandwidth specifications (see DC Operating Conditions).
7. The stressed eye is assumed to have a diamond shape.
8. For this test, the following can be adjusted as needed without exceeding the specifications, including the limits described in note 1: V_{REFDQ}, DFE gain bias step, and DFE Taps 1, 2, 3, 4 bias step.
9. The stressed eye is defined as centered on the DQS_t/DQS_c crossing during the calibration. Measurement includes an optimal set of DQS_t/DQS_c location, V_{REFDQ} and DFE solution to give the best eye margin..
10. The Rx stressed eye specification applies at 2933 and faster data rates.
11. EH/EW are measured at the slicer of the receiver.

Figure 221: Example of Rx Stressed Eye Height and Eye Width



AC and DC Logic Output Levels and Timing

Output Driver DC Electrical Characteristics for DQS and DQ

The DDR5 driver supports two different R_{ON} values. These R_{ON} values are referred as strong (low R_{ON}) and weak (high R_{ON}) modes. A functional representation of the output buffer is shown in the figure below.

A low voltage V_{DDQ} rail is under investigation and may be added in the future. Output driver impedance R_{ON} is defined as follows:

The individual pull-up and pull-down resistors ($R_{ON,Pu}$ and $R_{ON,Pd}$) are defined as follows:

$$R_{ON,Pu} = \frac{V_{DDQ} - V_{OUT}}{|I_{OUT}|} \text{ under the condition that } R_{ONPd} \text{ is off}$$

$$R_{ON,Pd} = \frac{V_{OUT}}{|I_{OUT}|} \text{ under the condition that } R_{ONPu} \text{ is off}$$

Figure 222: Output Driver

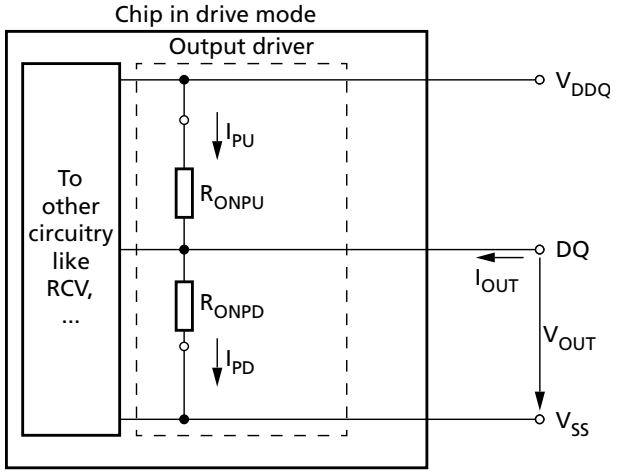


Table 327: Output Driver DC Electrical Characteristics (assuming R_{ZQ} = 240Ω, over entire operating temperature range, and after proper ZQ calibration)

$R_{ON,NOM}$	Resistor	V_{OUT}	MIN	NOM	MAX	Unit	Notes
34Ω	R_{ON34Pd}	$V_{OLdc} = 0.5 \times V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/7$	1, 2
		$V_{OMdc} = 0.8 \times V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/7$	1, 2
		$V_{OHdc} = 0.95 \times V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/7$	1, 2
	R_{ON34Pu}	$V_{OLdc} = 0.5 \times V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/7$	1, 2
		$V_{OMdc} = 0.8 \times V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/7$	1, 2
		$V_{OHdc} = 0.95 \times V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/7$	1, 2

Table 327: Output Driver DC Electrical Characteristics (assuming R_{ZQ} = 240Ω, over entire operating temperature range, and after proper ZQ calibration)

$R_{ON,NOM}$	Resistor	V_{OUT}	MIN	NOM	MAX	Unit	Notes
48Ω	R_{ON48Pd}	V_{OLdc} = 0.5 × V_{DDQ}	0.8	1	1.1	R_{ZQ}/5	1, 2
		V_{OMdc} = 0.8 × V_{DDQ}	0.9	1	1.1	R_{ZQ}/5	1, 2
		V_{OHdc} = 0.95 × V_{DDQ}	0.9	1	1.25	R_{ZQ}/5	1, 2
	R_{ON48Pu}	V_{OLdc} = 0.5 × V_{DDQ}	0.9	1	1.25	R_{ZQ}/5	1, 2
		V_{OMdc} = 0.8 × V_{DDQ}	0.9	1	1.1	R_{ZQ}/5	1, 2
		V_{OHdc} = 0.95 × V_{DDQ}	0.8	1	1.1	R_{ZQ}/5	1, 2
Mismatch between pull-up and pull-down, MM_{PuPd}		V_{OMdc} = 0.8 × V_{DDQ}	-10		10	%	1, 2, 3, 4
Mismatch DQ-DQ within byte variation pull-up, MM_{Pudd}		V_{OMdc} = 0.8 × V_{DDQ}			10	%	1, 2, 4
Mismatch DQ-DQ within byte variation pull-down, MM_{Pddd}		V_{OMdc} = 0.8 × V_{DDQ}			10	%	1, 2, 4

Notes: 1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. Pull-up and pull-down output driver impedances are recommended to be calibrated at 0.8 × VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 × VDDQ and 0.95 × VDDQ.
3. Measurement definition for mismatch between pull-up and pull-down, MMPuPd: Measure $R_{ON,Pu}$ and $R_{ON,Pd}$ both at 0.8 × V_{DD} separately; $R_{ON,NOM}$ is the nominal R_{ON} value

$$MM_{PuPd} = \frac{R_{ON,Pu} - R_{ON,Pd}}{R_{ON,NOM}} \times 100$$

4. R_{ON} variance range ratio to R_{ON} nominal value in a given component, including DQS_t and DQS_c.

$$MM_{Pu,dd} = \frac{R_{ON,Pu,Max} - R_{ON,Pu,Min}}{R_{ON,NOM}} \times 100$$

$$MM_{Pd,dd} = \frac{R_{ON,Pd,Max} - R_{ON,Pd,Min}}{R_{ON,NOM}} \times 100$$

5. This parameter of x16 device is specified for upper byte and lower byte.

Output Driver DC Electrical Characteristics for Loopback Signals LBDQS, LBDQ

The DDR5 loopback driver supports 34 ohms. A functional representation of the output buffer is shown in the figure below.

$$R_{ON,Pu} = \frac{V_{DDQ} - V_{OUT}}{|I_{OUT}|} \text{ under the condition that } R_{ONPd} \text{ is off}$$

$$R_{ON,Pd} = \frac{V_{OUT}}{|I_{OUT}|} \text{ under the condition that } R_{ONPu} \text{ is off}$$

Figure 223: Output Driver for Loopback Signals

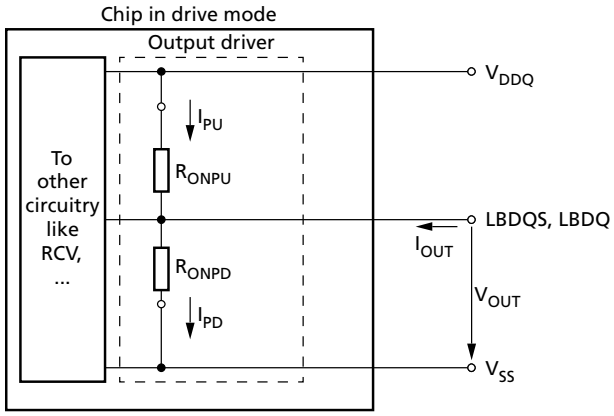


Table 328: Output Driver DC Electrical Characteristics, Assuming R_{ZQ} = 240Ω; Entire Operating Temperature Range; After Proper ZQ Calibration

$R_{ON,NOM}$	Resistor	V_{OUT}	MIN	NOM	MAX	Unit	Notes
34Ω	R_{ON34Pd}	V_{OLdc} = 0.5 × V_{DDQ}	0.8	1	1.1	R_{ZQ}/7	1, 2
		V_{OMdc} = 0.8 × V_{DDQ}	0.9	1	1.1	R_{ZQ}/7	1, 2
		V_{OHdc} = 0.95 × V_{DDQ}	0.9	1	1.25	R_{ZQ}/7	1, 2
	R_{ON34Pu}	V_{OLdc} = 0.5 × V_{DDQ}	0.9	1	1.25	R_{ZQ}/7	1, 2
		V_{OMdc} = 0.8 × V_{DDQ}	0.9	1	1.1	R_{ZQ}/7	1, 2
		V_{OHdc} = 0.95 × V_{DDQ}	0.8	1	1.1	R_{ZQ}/7	1, 2
Mismatch between pull-up and pull-down, MM_{PuPd}		V_{OMdc} = 0.8 × V_{DDQ}	-10		10	%	1, 2, 3, 4
Mismatch LBDQS-LBDQ within byte variation pull-up, MM_{Pudd}		V_{OMdc} = 0.8 × V_{DDQ}			10	%	1, 2, 4
Mismatch LBDQS-LBDQ within byte variation pull-down, MM_{Pddd}		V_{OMdc} = 0.8 × VV_{DDQ}			10	%	1, 2, 4

Notes: 1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity (TBD).
2. Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 × V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 × V_{DDQ} and 0.95 × V_{DDQ}.
3. Measurement definition for mismatch between pull-up and pull-down, MM_{PuPd}: Measure $R_{ON,Pu}$ and $R_{ON,PD}$ both at 0.8 × V_{DD} separately; $R_{ON,NOM}$ is the nominal R_{ON} value

$$MM_{PuPd} = \frac{R_{ON,Pu} - R_{ON,Pd}}{R_{ON,NOM}} \times 100$$

4. R_{ON} variance range ratio to R_{ON} nominal value in a given component, including LBDQS and LBDQ.

$$MM_{Pu,dd} = \frac{R_{ON,Pu,Max} - R_{ON,Pu,Min}}{R_{ON,NOM}} \times 100$$

$$MM_{Pd,dd} = \frac{R_{ON,Pd,Max} - R_{ON,Pd,Min}}{R_{ON,NOM}} \times 100$$

Loopback Output Timing

The loopback strobe LBDQS to loopback data LBDQ relationship is illustrated in the figure below.

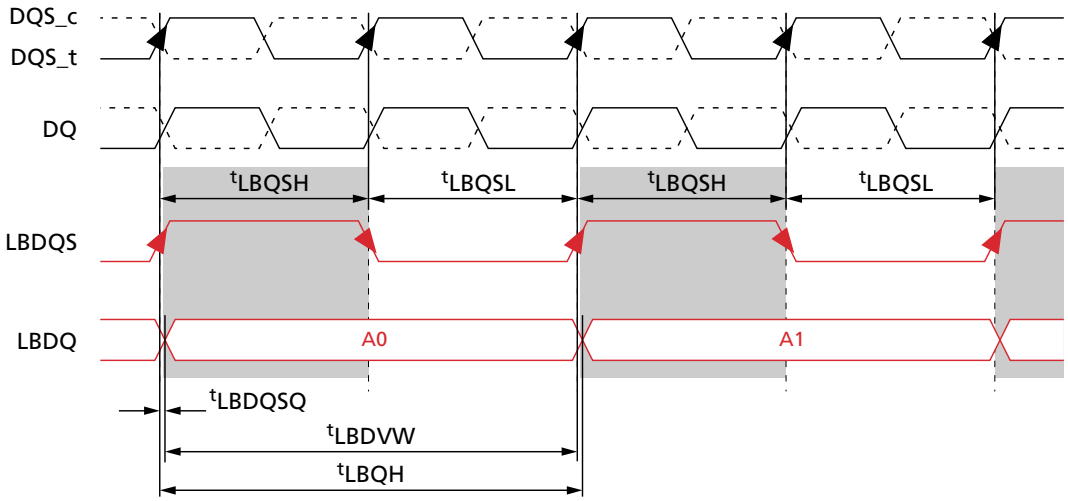
- ^{t}LBQSH describes the single-ended LBDQS strobe high pulse width
- ^{t}LBQSL describes the single-ended LBDQS strobe low pulse width
- ^{t}LBDQSQ describes the latest valid transition of LBDQ measured at both rising and falling edges of LBDQS
- ^{t}LBQH describes the earliest invalid transition of LBDQ measured at both rising and falling edges of LBDQS
- ^{t}LBDVW describes the data valid window per device per UI and is derived from (^{t}LBQH-^{t}LBDQSQ) of each UI on a given DRAM

Table 329: Loopback Output Timing

Parameter	Symbol	3200-4800		5200-6400		6800-8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Loopback LBDQS Output Low Time	^{t}LBQSL	0.7	-	TBD	-	TBD	-	^{t}CK	1
Loopback LBDQS Output High Time	^{t}LBQSH	0.7	-	TBD	-	TBD	-	^{t}CK	1
Loopback LBDQS to LBDQ Skew	^{t}LBDQSQ	0.2	-	TBD	-	TBD	-	^{t}CK/2	1
Loopback LBDQ Output Time from LBDQS	^{t}LBQH	3.6	-	TBD	-	TBD	-	^{t}CK/2	1
Loopback Data valid window (^{t}LBQH-^{t}LBDQSQ) of each UI per DRAM	^{t}LBDVW	3.4	-	TBD	-	TBD	-	^{t}CK/2	1

Notes: 1. Based on loopback four-way interleave setting (see MR53)

Figure 224: Loopback Strobe to Data Relationship



Alert_n Output Driver Characteristic

A functional representation of the output buffer is shown in the figure below. Output driver impedance R_{ON} is defined as follows:

$$R_{ON,Pd} = \frac{V_{OUT}}{|I_{OUT}|} \text{ under the condition that } R_{ONPu} \text{ is off}$$

Figure 225: Alert Driver

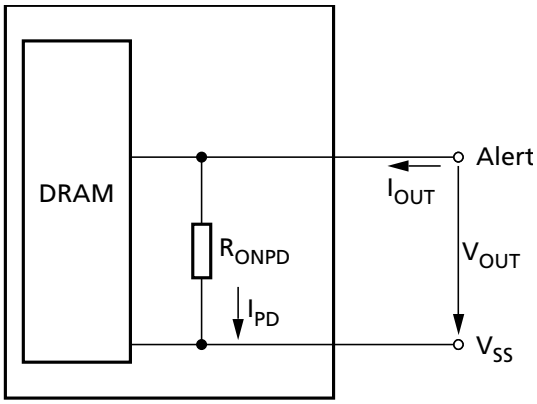


Table 330: Alert_n Output Driver DC Electrical Characteristics

Resistor	V_{OUT}	MIN	MAX	Unit
R_{ONPd}	$V_{OLdc} = 0.1 \times V_{DDQ}$	0.3	1.1	$R_{ZQ}/7$
	$V_{OMdc} = 0.8 \times V_{DDQ}$	0.4	1.1	$R_{ZQ}/7$
	$V_{OHdc} = 0.95 \times V_{DDQ}$	0.4	1.25	$R_{ZQ}/7$

Connectivity Test Mode Output Driver Characteristics

Following output driver impedance, R_{ON} will be applied to the test output pins during connectivity test (CT) mode.

The individual pull-up and pull-down resistors (R_{ON,Pu_CT} and R_{ON,Pd_CT}) are defined as follows:

$$R_{ON,Pu\_CT} = \frac{V_{DDQ} - V_{OUT}}{|I_{OUT}|}$$

$$R_{ON,Pd\_CT} = \frac{V_{OUT}}{|I_{OUT}|}$$

Figure 226: Chip-In Drive Mode

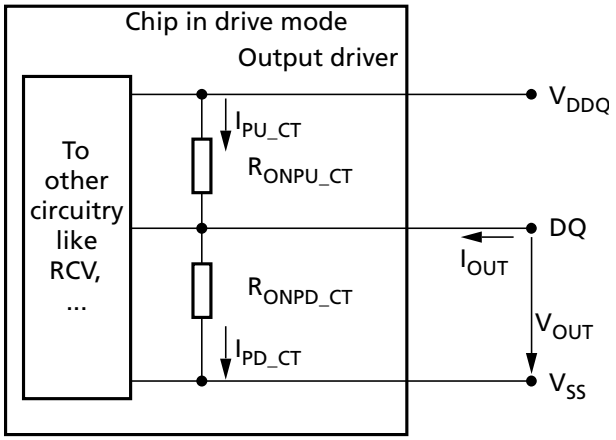


Table 331: Connectivity Test (CT) Mode Output Driver DC Electrical Characteristics

R_{ON,NOM_CT}	Resistor	V_{OUT}	MAX	Unit	Notes
34Ω	R_{ON,Pd_CT}	$V_{OB,dc} = 0.2 \times V_{DDQ}$	1.9	$R_{ZQ}/7$	1,2
		$V_{OLdc} = 0.5 \times V_{DDQ}$	2.0	$R_{ZQ}/7$	1,2
		$V_{OMdc} = 0.8 \times V_{DDQ}$	2.2	$R_{ZQ}/7$	1,2
		$V_{OHdc} = 0.95 \times V_{DDQ}$	2.5	$R_{ZQ}/7$	1,2
	R_{ON,Pu_CT}	$V_{OB,dc} = 0.2 \times V_{DDQ}$	1.9	$R_{ZQ}/7$	1,2
		$V_{OLdc} = 0.5 \times V_{DDQ}$	2.0	$R_{ZQ}/7$	1,2
		$V_{OMdc} = 0.8 \times V_{DDQ}$	2.2	$R_{ZQ}/7$	1,2
		$V_{OHdc} = 1.1 \times V_{DDQ}$	2.5	$R_{ZQ}/7$	1,2

Notes: 1. Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull-up and pull-down is defined.
2. Uncalibrated drive strength tolerance is specified at ±30%.

Single-Ended Output Levels

Table 332: Single-Ended Output Levels for DDR5 3200-6400

Parameter	Symbol	3200-6400	Unit	Notes
Output high measurement level (for output SR)	V_{OH}	0.75 x V_{pk-pk}	V	1
Output low measurement level (for output SR)	V_{OL}	0.25 x V_{pk-pk}	V	1

Notes: 1. V_{pk-pk} is the mean high voltage minus the mean low voltage over TBD samples.

Table 333: Single-Ended Output Levels for DDR5 6800-8800

Parameter	Symbol	6800-8800	Unit	Notes
Output high measurement level (for output SR)	V_{OH}	TBD	V	1
Output low measurement level (for output SR)	V_{OL}	TBD	V	1

Notes: 1. V_{pk-pk} is the mean high voltage minus the mean low voltage over TBD samples.

Single-Ended Output Levels for Loopback Signals

Table 334: Single-Ended Output Levels for Loopback Signals for DDR5 3200-6400

Parameter	Symbol	3200-6400	Unit	Notes
Output high measurement level (for output SR)	V_{OH}	0.75 x V_{pk-pk}	V	1
Output low measurement level (for output SR)	V_{OL}	0.25 x V_{pk-pk}	V	1

Notes: 1. V_{pk-pk} is the mean high voltage minus the mean low voltage over TBD samples.

Table 335: Single-Ended Output Levels for Loopback Signals for DDR5 6800-8800

Parameter	Symbol	6800-8800	Unit	Notes
Output high measurement level (for output SR)	V_{OH}	TBD	V	1
Output low measurement level (for output SR)	V_{OL}	TBD	V	1

Notes: 1. V_{pk-pk} is the mean high voltage minus the mean low voltage over TBD samples.

Single-Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OL} and V_{OH} for single-ended signals, as described in the following tables and figure.

Table 336: Single-Ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	V_{OL}	V_{OH}	[V_{OH} - V_{OL}] / delta TRse
Single-ended output slew rate for failing edge	V_{OH}	V_{OL}	[V_{OL} - V_{OH}] / delta TFse

Notes: 1. Output slew rate is verified by design and characterization and may not be subject to production test.

Figure 227: Single-Ended Output Slew Rate Definition

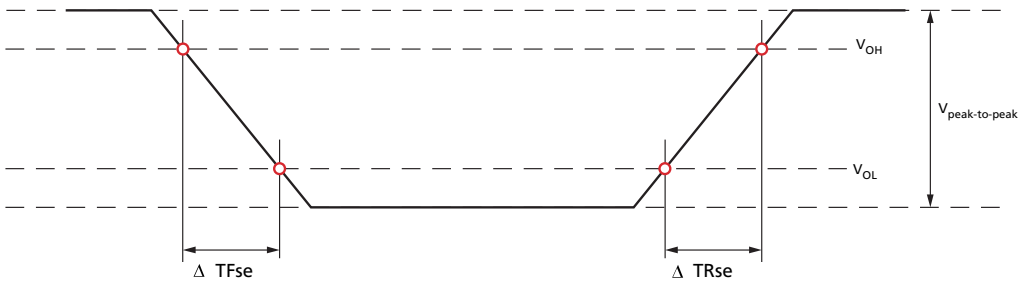


Table 337: Single-Ended Output Slew Rate for DDR5 3200-4800

Parameter	Symbol	3200-3600		4000-4400		4800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Single-ended output slew rate	SRQse	8	24	8	24	8	24	V/ns	

Table 338: Single-Ended Output Slew Rate for DDR5 5200-7200

Parameter	Symbol	5200-5600		6000-6400		6800-7200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Single-ended output slew rate	SRQse	12	24	TBD	TBD	TBD	TBD	V/ns	

Table 339: Single-Ended Output Slew Rate for DDR5 7600-8800

Parameter	Symbol	7600-8000		8400-8800		Unit	Note
		MIN	MAX	MIN	MAX		
Single-ended output slew rate	SRQse	TBD	TBD	TBD	TBD	V/ns	

Differential Output Levels

Table 340: Differential Output Levels for DDR5 3200-6400

Symbol	Parameter	3200-6400	Unit	Note
$V_{OH,diff}$	Differential output high measurement level (for output SR)	0.75 x $V_{diff,pk-pk}$	V	1
$V_{OL,diff}$	Differential output low measurement level (for output SR)	0.25 x $V_{diff,pk-pk}$	V	1

Notes: 1. $V_{diff,pk-pk}$ is the mean high voltage minus the mean low voltage over TBD samples.

Table 341: Differential Output Levels for DDR5 6800-8800

Symbol	Parameter	6800-8800	Unit	Note
$V_{OH,diff}$	Differential output high measurement level (for output SR)	TBD	V	1
$V_{OL,diff}$	Differential output low measurement level (for output SR)	TBD	V	1

Notes: 1. $V_{diff,pk-pk}$ is the mean high voltage minus the mean low voltage over TBD samples.

Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL,diff}$ and $V_{OH,diff}$ for differential signals, as shown in the tables below.

Table 342: Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OL,diff}$	$V_{OH,diff}$	[$V_{OH,diff}$, $V_{OL,diff}$,] / delta TRdiff
Differential output slew rate for failing edge	$V_{OH,diff}$	$V_{OL,diff}$	[$V_{OL,diff}$, $V_{OH,diff}$] / delta TFdiff

Notes: 1. Output slew rate is verified by design and characterization and may not be subject to production test.

Figure 228: Differential Output Slew Rate Definition

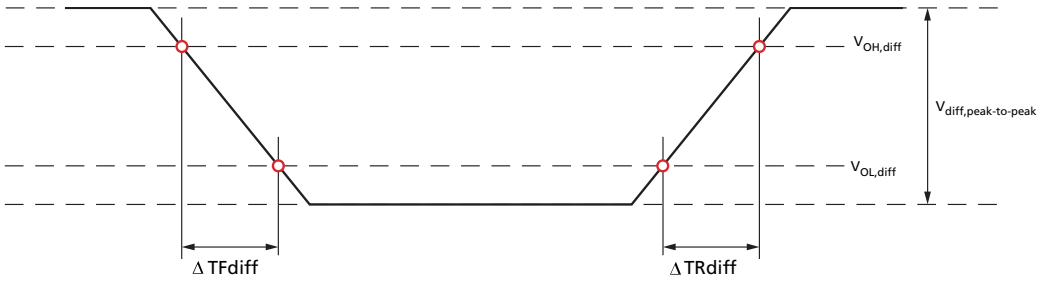


Table 343: Differential Output Slew Rate for DDR5 3200-4800

Parameter	Symbol	3200-3600		4000-4400		4800		Unit
		Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	16	48	16	48	16	48	V/ns

Table 344: Differential Output Slew Rate for DDR5 5200-7200

Parameter	Symbol	5200-5600		6000-6400		6800-7200		Unit
		Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	24	48	TBD	TBD	TBD	TBD	V/ns

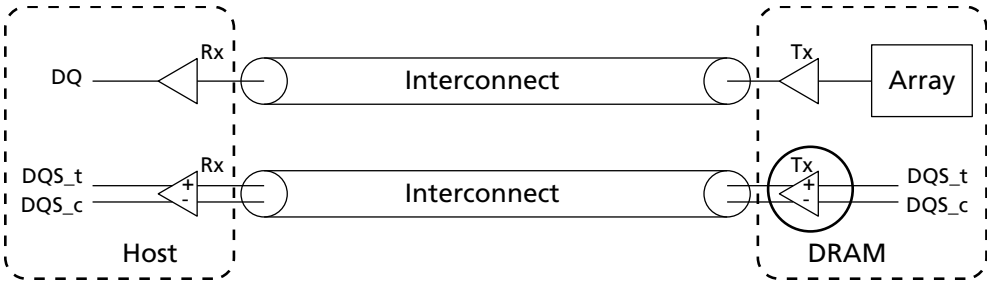
Table 345: Differential Output Slew Rate for DDR5 7600-8800

Parameter	Symbol	7600-8000		8400-8800		Unit
		Min	Max	Min	Max	
Differential output slew rate	SRQdiff	TBD	TBD	TBD	TBD	V/ns

Tx DQS Jitter

The random jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The deterministic jitter (Dj) specified is bounded. The device output jitter must not exceed maximum values specified in the tables below.

Figure 229: Tx DQS Jitter



Tx DQS Jitter Parameters

The following notes apply to all tables:

- DCD = duty cycle distortion; BUJ = bounded uncorrelated jitter; pp = peak to peak

- On-die noise similar to what occurs with all toggling transmitter and receiver lanes needs to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the crosstalk or BUJ is not significant or can be estimated within tolerable error, even with all transmitter lanes sending patterns. When a socket is present, such as DUT being device component, the contribution of the crosstalk may be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note there may be cases when one of the Dj and Rj specs is met and another violated, in which case the signaling analysis should be run to determine link feasibility.
- The validation methodology for these parameters will be covered in the future.
- See the AC and DC Global Definitions section for details on UI, NUI and jitter definitions.
- The DQ pins' duty cycle must be adjusted as close to 50% as possible using the Global and Per-Pin Duty Cycle Adjuster feature prior to running the Tx DQS jtter test.
- The mode registers for the Duty Cycle Adjuster are MR43 and MR44. The mode registers for the per-pin DCA of DQS are MR103-MR110.
- Spread spectrum clocking (SSC) must be disabled while running the Tx DQS jitter test.
- These parameters are tested using the continuous clock pattern, which is sent out from the device without the need for sending out continuous MRR commands. Set MR25:OP[3] = 1 to enable this feature.
- These parameters are tested on the CTC2 card only.

Table 346: Tx DQS Jitter Parameters fo DDR5 3200-4800

Parameter	Symbol	3200		3600		4000		4400		4800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Rj RMS value of 1-UI jitter without BUJ	^{t}TX_DQS_1UI_Rj_NoBUJ	-	^{t}CK_1UI_Rj_noBUJ + 0.002	-	^{t}CK_1UI_Rj_noBUJ + 0.002	-	^{t}CK_1UI_Rj_noBUJ + 0.002	-	^{t}CK_1UI_Rj_noBUJ + 0.002	-	^{t}CK_1UI_Rj_noBUJ + 0.002	UI (RMS)	1,2,3
Dj pp value of 1-UI jitter without BUJ	^{t}TX_DQS_1UI_Dj_NoBUJ	-	0.150	-	0.150	-	0.150	-	0.150	-	0.150	UI	
Rj RMS value of N-UI jitter without BUJ, where 1<N<4	^{t}TX_DQS_NUI_Rj_NoBUJ	-	^{t}CK_NU_Rj_noBUJ + 0.002	-	^{t}CK_NU_Rj_noBUJ + 0.002	-	^{t}CK_NU_Rj_noBUJ + 0.002	-	^{t}CK_NU_Rj_noBUJ + 0.002	-	^{t}CK_NU_Rj_noBUJ + 0.002	UI (RMS)	3
Dj pp value of N-UI jitter without BUJ, where 1<N<4	^{t}Tx_DQS_NUI_Dj_NoBUJ	-	0.150	-	0.150	-	0.150	-	0.150	-	0.150	UI	

Notes: 1. Rj RMS value of 1-UI jitter. Without BUJ, but with on-die system-like noise present. This extraction is to be done after software correction of DCD.
2. See the AC and DC Global Definitions section for details on minimum BER requirements.

3. The maximum value of ^{t}TX_DQS_1UI_Rj_NoBUJ and ^{t}TX_DQS_NUI_Rj_NoBUJ can be 6m UI RMS.

Table 347: Tx DQS Jitter Parameters for DDR5 5200-6400

Parameter	Symbol	5200		5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Rj RMS value of 1-UI jitter without BUJ	^{t}TX_DQS_1UI_Rj_NoBUJ	-	^{t}CK_1UI_Rj_noBUJ + 0.002	-	^{t}CK_1UI_Rj_noBUJ + 0.002	-	TBD	-	TBD	UI (RMS)	1,2,3
Dj pp value of 1-UI jitter without BUJ	^{t}TX_DQS_1UI_Dj_NoBUJ	-	0.130	-	0.130	-	TBD	-	TBD	UI	
Rj RMS value of N-UI jitter without BUJ, where 1<N ≤4	^{t}TX_DQS_NUI_Rj_NoBUJ	-	^{t}CK_NUI_Rj_noBUJ + 0.002	-	^{t}CK_NUI_Rj_noBUJ + 0.002	-	TBD	-	TBD	UI (RMS)	3
Dj pp value of N-UI jitter without BUJ, where 1<N ≤4	^{t}Tx_DQS_NUI_Dj_NoBUJ	-	0.130	-	0.130	-	TBD	-	TBD	UI	
Rj RMS value of N-UI jitter without BUJ, where 1<N ≤5	^{t}TX_DQS_NUI_Rj_NoBUJ	-	-	-	-	-	TBD	-	TBD	UI (RMS)	
Dj pp value of N-UI jitter without BUJ, where 1<N ≤5	^{t}Tx_DQS_NUI_Dj_NoBUJ	-	-	-	-	-	TBD	-	TBD	UI	

Notes: 1. Rj RMS value of 1-UI jitter. Without BUJ, but with on-die system-like noise present. This extraction is to be done after software correction of DCD.
2. See AC and DC Global Definitions section for details on the minimum BER requirements.
3. The maximum value of ^{t}TX_DQS_1UI_Rj_NoBUJ and ^{t}TX_DQS_NUI_Rj_NoBUJ can be 6m UI RMS.

Table 348: Tx DQS Jitter Parameters for DDR5 6800-7600

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Rj RMS value of 1-UI jitter without BUJ	^{t}TX_DQS_1UI_Rj_NoBUJ	-	TBD	-	TBD	-	TBD	UI (RMS)	1,2
Dj pp value of 1-UI jitter without BUJ	^{t}TX_DQS_1UI_Dj_NoBUJ	-	TBD	-	TBD	-	TBD	UI	
Rj RMS value of N-UI jitter without BUJ, where 1<N≤4	^{t}TX_DQS_NUI_Rj_NoBUJ	-	TBD	-	TBD	-	TBD	UI (RMS)	2
Dj pp value of N-UI jitter without BUJ, where 1<N≤4	^{t}Tx_DQS_NUI_Dj_NoBUJ	-	TBD	-	TBD	-	TBD	UI	

Table 348: Tx DQS Jitter Parameters for DDR5 6800-7600 (Continued)

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Rj RMS value of N-UI jitter without BUJ, where 1<N≤6	^{t}TX_DQS_NUI_Rj_NoBUJ	-	TBD	-	TBD	-	TND	UI (RMS)	
Dj pp value of N-UI jitter without BUJ, where 1<N≤6	^{t}Tx_DQS_NUI_Dj_NoBUJ	-	TBD	-	TBD	-	TBD	UI	

Notes: 1. Rj RMS value of 1-UI jitter. Without BUJ, but with on-die system-like noise present. This extraction is to be done after software correction of DCD.
2. The maximum value of ^{t}TX_DQS_1UI_Rj_NoBUJ and ^{t}TX_DQS_NUI_Rj_NoBUJ can be 6m UI RMS.

Table 349: Tx DQS Jitter Parameters for DDR5 7600-8800

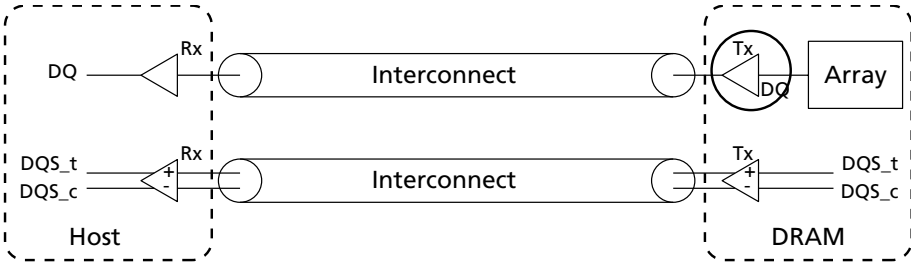
Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Rj RMS value of 1-UI jitter without BUJ	^{t}TX_DQS_1UI_Rj_NoBUJ	-	TBD	-	TBD	-	TBD	UI (RMS)	1,2
Dj pp value of 1-UI jitter without BUJ	^{t}TX_DQS_1UI_Dj_NoBUJ	-	TBD	-	TBD	-	TBD	UI	
Rj RMS value of N-UI jitter without BUJ, where 1<N<4	^{t}TX_DQS_NUI_Rj_NoBUJ	-	TBD	-	TBD	-	TBD	UI (RMS)	2
Dj pp value of N-UI jitter without BUJ, where 1<N<4	^{t}Tx_DQS_NUI_Dj_NoBUJ	-	TBD	-	TBD	-	TBD	UI	

Notes: 1. Rj RMS value of 1-UI jitter. Without BUJ, but with on-die system-like noise present. This extraction is to be done after software correction of DCD.
2. The maximum value of ^{t}TX_DQS_1UI_Rj_NoBUJ and ^{t}TX_DQS_NUI_Rj_NoBUJ can be 6m UI RMS.

Tx DQ Jitter

The random jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The deterministic jitter (Dj) specified is bounded. The device output jitter must not exceed maximum values specified in the tables below.

Figure 230: Tx DQ Jitter



Tx DQ Jitter Parameters

The following notes apply to all tables:

- Dj=deterministic jitter; Rj=random jitter; DCD=duty cycle distortion; BUJ=bounded uncorrelated jitter; pp=peak-to-peak]
- The validation methodology for these parameters will be covered in the future.
- The mode registers for the Duty Cycle Adjuster are MR43 and MR44. The mode registers for the Per Pin DCA of DQLx are MR(133+8x) and MR(134+8x), where 0≤ x≤7. The mode registers for the Per Pin DCA of DQUy are MR(197+8y) and MR(198+8y), where 0 ≤ y ≤7.
- Spread spectrum clocking (SSC) must be disabled while running the Tx DQS jitter test.
- These parameters are tested using the continuous clock pattern, which is sent out from the device without the need for sending out continuous MRR commands. MR25 OP[3] is set to 1 to enable this feature.
- These parameters are tested on the CTC2 card only.

Table 350: Tx DQ Jitter Parameters for DDR5 3200-4800

Parameter	Symbol	3200		3600		4000		4400		4800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Rj RMS value of 1-UI jitter without BUJ	^{t}TX_DQ_1UI_Rj_noBUJ	-	^{t}CK_1UI_Rj_noBUJ + 0.002	-	^{t}CK_1UI_Rj_noBUJ + 0.002	-	^{t}CK_1UI_Rj_noBUJ + 0.002	-	^{t}CK_1UI_Rj_noBUJ + 0.002	-	^{t}CK_1UI_Rj_noBUJ + 0.002	UI (RMS)	1,2,3,5,6,7
Dj pp value of 1-UI jitter without BUJ	^{t}TX_DQ_1UI_Dj_noBUJ	-	0.150	-	0.150	-	0.150	-	0.150	-	0.150	UI	3,4
Rj RMS value of N-UI jitter without BUJ, where 1<N<4	^{t}TX_DQ_NUI_Rj_noBUJ	-	^{t}CK_NU_Rj_noBUJ + 0.002	-	^{t}CK_NU_Rj_noBUJ + 0.002	-	^{t}CK_NU_Rj_noBUJ + 0.002	-	^{t}CK_NU_Rj_noBUJ + 0.002	-	^{t}CK_NU_Rj_noBUJ + 0.002	UI (RMS)	2,3,5,6,7
Dj pp value of N-UI jitter without BUJ, where 1<N<4	^{t}Tx_DQ_NUI_Dj_noBUJ	-	0.150	-	0.150	-	0.150	-	0.150	-	0.150	UI	4,5,6
Delay of any data lane relative to strobe lane	^{t}TX_DQS2DQ	-0.100	0.100	-0.100	0.100	-0.100	0.100	-0.100	0.100	-0.100	0.100	UI	3,4,6

Notes: 1. On-die noise similar to what occurs with all toggling transmitter and receiver lanes needs to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the crosstalk or BUJ is not significant or can be estimated within tolerable error, even with all transmitter lanes sending patterns. When a socket is present, such as DUT being device component, the contribution of the crosstalk may be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note there may be cases when one of the Dj and Rj specs is met and another violated, in which case the signaling analysis should be run to determine link feasibility.
2. Rj RMS value of 1-UI jitter without BUJ, but with on-die system-like noise present. This extraction is to be done after software correction of DCD.
3. Delay of any data lane relative to strobe lane, as measured at Tx output.
4. V_{REF} noise level to DQ jitter should be adjusted to minimize DCD.
5. See AC and DC Global Definitions section for details on UI, NUI and jitter definitions.
6. The DQ pins' duty cycle must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster (MR43-44) feature prior to running the Tx DQS jtter test.
7. The maximum value of ^{t}TX_DQ_Rj_1UI_NoBUJ and ^{t}TX_DQ_Rj_NU_NoBUJ can be 6m UI RMS.

Table 351: Tx DQ Jitter Parameters for DDR5 5200-6400

Parameter	Symbol	5200		5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Rj RMS value of 1-UI jitter without BUJ	^{t}TX_DQ_1UI_Rj_NoBUJ	-	^{t}CK_1UI_Rj_noBUJ + 0.002	-	^{t}CK_1UI_Rj_noBUJ + 0.002	-	TBD	-	TBD	UI (RMS)	1,2,3,5,6
Dj pp value of 1-UI jitter without BUJ	^{t}TX_DQ_1UI_Dj_NoBUJ	-	0.130	-	0.130	-	TBD	-	TBD	UI	3,5
Rj RMS value of N-UI jitter without BUJ, where 1<N ≤4	^{t}TX_DQ_NUI_Rj_NoBUJ	-	^{t}CK_NUI_Rj_noBUJ + 0.002	-	^{t}CK_NUI_Rj_noBUJ + 0.002	-	TBD	-	TBD	UI (RMS)	2,3,6
Dj pp value of N-UI jitter without BUJ, where 1<N ≤4	^{t}Tx_DQ_NUI_Dj_NoBUJ	-	0.130	-	0.130	-	TBD	-	TBD	UI	4,5
Rj RMS of N-UI jitter without BUJ, where 1<N ≤5	^{t}TX_DQ_NUI_Rj_NoBUJ	-	-	-	-	-	TBD	-	TBD	UI (RMS)	
Dj pp value of N-UI jitter without BUJ, where 1<N ≤5	^{t}Tx_DQ_NUI_Dj_NoBUJ	-	-	-	-	-	TBD	-	TBD	UI	
Delay of any data lane relative to strobe lane	^{t}TX_DQS2DQ	-0.100	0.100	-0.100	0.100	TBD	TBD	TBD	TBD	UI	3

Notes: 1. On-die noise similar to what occurs with all toggling transmitter and receiver lanes needs to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the crosstalk or BUJ is not significant or can be estimated within tolerable error, even with all transmitter lanes sending patterns. When a socket is present, such as DUT being device component, the contribution of the crosstalk may be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the

lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note there may be cases when one of the Dj and Rj specs is met and another violated, in which case the signaling analysis should be run to determine link feasibility.
2. Rj RMS value of 1-UI jitter without BUJ, but with on-die system-like noise present. This extraction is to be done after software correction of DCD.
3. Delay of any data lane relative to strobe lane, as measured at Tx output.
4. V_{REF} noise level to DQ jitter should be adjusted to minimize DCD.
5. See AC and DC Global Definitions section for details on UI, NUI and jitter definitions.
6. The maximum value of ^{t}TX_DQS_1UI_Rj_NoBUJ and ^{t}TX_DQS_NUI_Rj_NoBUJ can be 6m UI RMS.

Table 352: Tx DQ Jitter Parameters for DDR5 6800-7600

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Rj RMS value of 1-UI jitter without BUJ	^{t}TX_DQ_1UI_Rj_NoBUJ	-	TBD	-	TBD	-	TBD	UI (RMS)	1,2,3,5,6
Dj pp value of 1-UI jitter without BUJ	^{t}TX_DQ_1UI_Dj_NoBUJ	-	TBD	-	TBD	-	TBD	UI	3,5
Rj RMS value of N-UI jitter without BUJ, where 1<N≤4	^{t}TX_DQ_NUI_Rj_NoBUJ	-	TBD	-	TBD	-	TBD	UI (RMS)	2,3,5,6
Dj pp value of N-UI jitter without BUJ, where 1<N≤4	^{t}Tx_DQ_NUI_Dj_NoBUJ	-	TBD	-	TBD	-	TBD	UI	4,5
Rj RMS of N-UI jitter without BUJ, where 1<N≤6	^{t}TX_DQ_NUI_Rj_NoBUJ	-	TBD	-	TBD	-	TBD	UI (RMS)	
Dj pp N-UI jitter without BUJ, where 1<N≤6	^{t}Tx_DQ_NUI_Dj_NoBUJ	-	TBD	-	TBD	-	TBD	UI	
Delay of any data lane relative to strobe lane	^{t}TX_DQS2DQ	TBD	TBD	TBD	TBD	TBD	TBD	UI	3

Notes: 1. On-die noise similar to what occurs with all toggling transmitter and receiver lanes needs to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the crosstalk or BUJ is not significant or can be estimated within tolerable error, even with all transmitter lanes sending patterns. When a socket is present, such as DUT being device component, the contribution of the crosstalk may be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note there may be cases when one of the Dj and Rj specs is met and another violated, in which case the signaling analysis should be run to determine link feasibility.
2. Rj RMS value of 1-UI jitter without BUJ, but with on-die system-like noise present. This extraction is to be done after software correction of DCD.
3. Delay of any data lane relative to strobe lane, as measured at Tx output.
4. V_{REF} noise level to DQ jitter should be adjusted to minimize DCD.
5. See AC and DC Global Definitions section for details on UI, NUI and jitter definitions.

6. The maximum value of ^{t}TX_DQS_1UI_Rj_NoBUJ and ^{t}TX_DQS_NUI_Rj_NoBUJ can be 6m UI RMS.

Table 353: Tx DQ Jitter Parameters for DDR5 8000-8800

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Rj RMS value of 1-UI jitter without BUJ	^{t}TX_DQ_1UI_Rj_NoBUJ	-	TBD	-	TBD	-	TBD	UI (RMS)	1,2,3,5,6
Dj pp value of 1-UI jitter without BUJ	^{t}TX_DQ_1UI_Dj_NoBUJ	-	TBD	-	TBD	-	TBD	UI	3,5
Rj RMS value of N-UI jitter without BUJ, where 1<N<4	^{t}TX_DQ_NUI_Rj_NoBUJ	-	TBD	-	TBD	-	TBD	UI (RMS)	2,3,5,6
Dj pp value of N-UI jitter without BUJ, where 1<N<4	^{t}Tx_DQ_NUI_Dj_NoBUJ	-	TBD	-	TBD	-	TBD	UI	4,5
Delay of any data lane relative to strobe lane	^{t}TX_DQS2DQ	TBD	TBD	TBD	TBD	TBD	TBD	UI	3

Notes: 1. On-die noise similar to what occurs with all toggling transmitter and receiver lanes needs to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the crosstalk or BUJ is not significant or can be estimated within tolerable error, even with all transmitter lanes sending patterns. When a socket is present, such as DUT being device component, the contribution of the crosstalk may be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note there may be cases when one of the Dj and Rj specs is met and another violated, in which case the signaling analysis should be run to determine link feasibility.
2. Rj RMS value of 1-UI jitter without BUJ, but with on-die system-like noise present. This extraction is to be done after software correction of DCD.
3. Delay of any data lane relative to strobe lane, as measured at Tx output.
4. V_{REF} noise level to DQ jitter should be adjusted to minimize DCD.
5. See AC and DC Global Definitions section for details on UI, NUI and jitter definitions.
6. The maximum value of ^{t}TX_DQS_1UI_Rj_NoBUJ and ^{t}TX_DQS_NUI_Rj_NoBUJ can be 6m UI RMS.

Tx DQ Stressed Eye

Tx DQ stressed eye height and eye width must meet minimum specification values at BER=E-9 and confidence level 99.5%. Tx DQ Stressed Eye shows the DQS to DQ skew for both eye width and height. To support different host receiver (Rx) designs, it is the responsibility of the host to ensure the advanced DQS edges are adjusted accordingly via the Read DQS Offset Timing mode register settings (MR40:OP[3:0]).

Figure 231: Tx DQ Stressed Eye

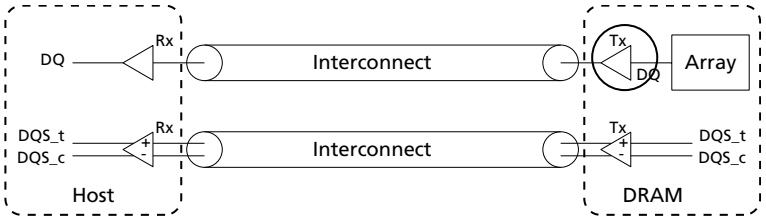


Figure 232: Read Burst Example for Pin DQx Depicting Bit 0 and 5 Relative to the DQS Edge for 0 UI Skew

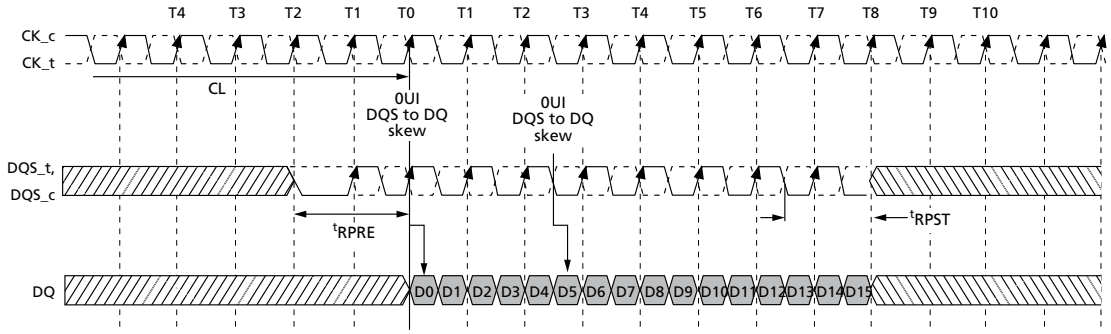
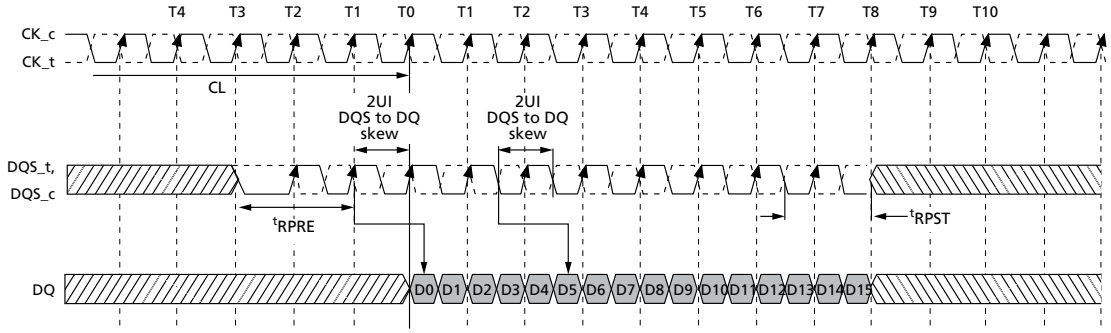


Figure 233: Read Burst Example for Pin DQx Depicting Bit 0 and 5 Relative to the DQS Edge for 2 UI Skew with Read DQS Offset Timing Set to 1 Clock (2UI)



Tx DQ Stressed Eye Parameters

The following notes apply to all tables:

- EH = Eye Height; EW = Eye Width; BER = Bit Error Rate, SES = Stressed Eye Skew
- Minimum BER E^{-9} and Confidence Level of 99.5% per pin.
- Refer to the minimum Bit Error Rate (BER) requirements for DDR5.
- The validation methodology for these parameters will be covered in the future.
- Mismatch is defined as DQS to DQ mismatch in UI increments.
- The DQ pins' duty cycle must be adjusted as close to 50% as possible using the Duty Cycle Adjuster feature prior to running the Tx DQS jtter test.
- The mode registers for the Duty Cycle Adjuster are MR43 and MR44. The mode registers for the per-pin DCA of DQS are MR103-MR110. The mode registers for the per-pin DCA of DQLx are

MR(133+8x) and MR(134+8x), where 0 ≤x ≤7. The mode registers for the per-pin DCA of DQUy are MR(197+8y) and MR(198+8y), where 0 ≤y ≤7.

- Spread spectrum clocking (SSC) must be disabled while running these tests.
- These parameters are tested using the continuous PRBS8 LFSR training pattern, which is sent out on all DQ lanes off the device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to 1 to enable this feature.
- These parameters are tested on the CTC2 card only.
- Matched DQS to DQ would require the DQs to be adjusted by 0.5UI to place it in the center of the DQ eye. 1UI mismatch would require the DQS to be adjusted 1.5UI. Generally, for XUI mismatch the DQ must be adjusted XUI + 0.5UI to be placed in the center of the eye.

Table 354: Tx DQ Stressed Eye Parameters for DDR5 3200–4800

Parameter	Symbol	3200		3600		4000		4400		4800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Eye height specified at the transmitter with a skew between DQ and DQS of 1UI	TXEH_DQ_SES_1UI	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mV	
Eye width specified at the transmitter with a skew between DQ and DQS of 1UI	TXEW_DQ_SES_1UI	0.72	–	0.72	–	0.72	–	0.72	–	0.72	–	UI	
Eye height specified at the transmitter with a skew between DQ and DQS of 2UI	TXEH_DQ_SES_2UI	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mV	
Eye width specified at the transmitter with a skew between DQ and DQS of 2UI	TXEW_DQ_SES_2UI	0.72	–	0.72	–	0.72	–	0.72	–	0.72	–	UI	
Eye height specified at the transmitter with a skew between DQ and DQS of 3UI	TXEH_DQ_SES_3UI	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mV	
Eye width specified at the transmitter with a skew between DQ and DQS of 3UI	TXEW_DQ_SES_3UI	0.72	–	0.72	–	0.72	–	0.72	–	0.72	–	UI	
Eye height specified at the transmitter with a skew between DQ and DQS of 4UI	TXEH_DQ_SES_4UI	-	-	-	-	-	-	-	-	-	-	mV	1

Table 354: Tx DQ Stressed Eye Parameters for DDR5 3200–4800

Parameter	Symbol	3200		3600		4000		4400		4800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Eye width specified at the transmitter with a skew between DQ and DQS of 4UI	TXEW_DQ_SES_4UI	-	-	-	-	-	-	-	-	-	-	UI	1
Eye height specified at the transmitter with a skew between DQ and DQS of 5UI	TXEH_DQ_SES_5UI	-	-	-	-	-	-	-	-	-	-	mV	1
Eye width specified at the transmitter with a skew between DQ and DQS of 5UI	TXEW_DQ_SES_5UI	-	-	-	-	-	-	-	-	-	-	UI	1

Notes: 1. The number of UI's accumulated will depend on the speed of the link. For higher speeds, higher UI accumulation may be specified. For lower speeds, N=4,5 UI may not be applicable.

Table 355: Tx DQ Stressed Eye Parameters for DDR5 5200–6400

Parameter	Symbol	5200		5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Eye height specified at the transmitter with a skew between DQ and DQS of 1UI	TXEH_DQ_SES_1UI	TBD	-	TBD	TBD	TBD	TBD	TBD	TBD	mV	
Eye width specified at the transmitter with a skew between DQ and DQS of 1UI	TXEW_DQ_SES_1UI	0.74	-	0.74	TBD	TBD	TBD	TBD	TBD	UI	
Eye height specified at the transmitter with a skew between DQ and DQS of 2UI	TXEH_DQ_SES_2UI	TBD	-	TBD	TBD	TBD	TBD	TBD	TBD	mV	
Eye width specified at the transmitter with a skew between DQ and DQS of 2UI	TXEW_DQ_SES_2UI	0.74	-	0.74	TBD	TBD	TBD	TBD	TBD	UI	
Eye height specified at the transmitter with a skew between DQ and DQS of 3UI	TXEH_DQ_SES_3UI	TBD	-	TBD	TBD	TBD	TBD	TBD	TBD	mV	
Eye width specified at the transmitter with a skew between DQ and DQS of 3UI	TXEW_DQ_SES_3UI	0.74	-	0.74	TBD	TBD	TBD	TBD	TBD	UI	

Table 355: Tx DQ Stressed Eye Parameters for DDR5 5200–6400

Parameter	Symbol	5200		5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Eye height specified at the transmitter with a skew between DQ and DQS of 4UI	TXEH_DQ_SES_4UI	TBD	-	TBD	TBD	TBD	TBD	TBD	TBD	mV	1
Eye width specified at the transmitter with a skew between DQ and DQS of 4UI	TXEW_DQ_SES_4UI	0.74	-	0.74	TBD	TBD	TBD	TBD	TBD	UI	1
Eye height specified at the transmitter with a skew between DQ and DQS of 5UI	TXEH_DQ_SES_5UI	-	-	-	-	-	-	-	-	mV	1
Eye width specified at the transmitter with a skew between DQ and DQS of 5UI	TXEW_DQ_SES_5UI	-	-	-	-	-	-	-	-	UI	1

Notes: 1. The number of UI's accumulated will depend on the speed of the link. For higher speeds, higher UI accumulation may be specified. For lower speeds, N=4,5 UI may not be applicable.

Table 356: Tx DQ Stressed Eye Parameters for DDR5 6800–7600

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Eye height specified at the transmitter with a skew between DQ and DQS of 1UI	TXEH_DQ_SES_1UI	TBD	TBD	TBD	TBD	TBD	TBD	mV	
Eye width specified at the transmitter with a skew between DQ and DQS of 1UI	TXEW_DQ_SES_1UI	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Eye height specified at the transmitter with a skew between DQ and DQS of 2UI	TXEH_DQ_SES_2UI	TBD	TBD	TBD	TBD	TBD	TBD	mV	
Eye width specified at the transmitter with a skew between DQ and DQS of 2UI	TXEW_DQ_SES_2UI	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Eye height specified at the transmitter with a skew between DQ and DQS of 3UI	TXEH_DQ_SES_3UI	TBD	TBD	TBD	TBD	TBD	TBD	mV	
Eye width specified at the transmitter with a skew between DQ and DQS of 3UI	TXEW_DQ_SES_3UI	TBD	TBD	TBD	TBD	TBD	TBD	UI	

Table 356: Tx DQ Stressed Eye Parameters for DDR5 6800–7600

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Eye height specified at the transmitter with a skew between DQ and DQS of 4UI	TXEH_DQ_SES_4UI	TBD	TBD	TBD	TBD	TBD	TBD	mV	1
Eye width specified at the transmitter with a skew between DQ and DQS of 4UI	TXEW_DQ_SES_4UI	TBD	TBD	TBD	TBD	TBD	TBD	UI	1
Eye height specified at the transmitter with a skew between DQ and DQS of 5UI	TXEH_DQ_SES_5UI	TBD	TBD	TBD	TBD	TBD	TBD	mV	1
Eye width specified at the transmitter with a skew between DQ and DQS of 5UI	TXEW_DQ_SES_5UI	TBD	TBD	TBD	TBD	TBD	TBD	UI	1

Notes: 1. The number of UI's accumulated will depend on the speed of the link. For higher speeds, higher UI accumulation may be specified. For lower speeds, N=4,5 UI may not be applicable.

Table 357: Tx DQ Stressed Eye Parameters for DDR5 8000-8800

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Eye height specified at the transmitter with a skew between DQ and DQS of 1UI	TXEH_DQ_SES_1UI	TBD	TBD	TBD	TBD	TBD	TBD	mV	
Eye width specified at the transmitter with a skew between DQ and DQS of 1UI	TXEW_DQ_SES_1UI	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Eye height specified at the transmitter with a skew between DQ and DQS of 2UI	TXEH_DQ_SES_2UI	TBD	TBD	TBD	TBD	TBD	TBD	mV	
Eye width specified at the transmitter with a skew between DQ and DQS of 2UI	TXEW_DQ_SES_2UI	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Eye height specified at the transmitter with a skew between DQ and DQS of 3UI	TXEH_DQ_SES_3UI	TBD	TBD	TBD	TBD	TBD	TBD	mV	
Eye width specified at the transmitter with a skew between DQ and DQS of 3UI	TXEW_DQ_SES_3UI	TBD	TBD	TBD	TBD	TBD	TBD	UI	

Table 357: Tx DQ Stressed Eye Parameters for DDR5 8000-8800 (Continued)

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Eye height specified at the transmitter with a skew between DQ and DQS of 4UI	TXEH_DQ_SES_4UI	TBD	TBD	TBD	TBD	TBD	TBD	mV	1
Eye width specified at the transmitter with a skew between DQ and DQS of 4UI	TXEW_DQ_SES_4UI	TBD	TBD	TBD	TBD	TBD	TBD	UI	1
Eye height specified at the transmitter with a skew between DQ and DQS of 5UI	TXEH_DQ_SES_5UI	TBD	TBD	TBD	TBD	TBD	TBD	mV	1
Eye width specified at the transmitter with a skew between DQ and DQS of 5UI	TXEW_DQ_SES_5UI	TBD	TBD	TBD	TBD	TBD	TBD	UI	1

Notes: 1. The number of UI's accumulated will depend on the speed of the link. For higher speeds, higher UI accumulation may be specified. For lower speeds, N=4,5 UI may not be applicable.

Speed Bin Tables by Speed Grade: Standard

DDR5 SDRAM timing is primarily covered by two types of tables: the speed bin tables in this section and the tables found in the Electrical Characteristics and AC Timing Parameters section. The speed bin tables on the following pages list the ^{t}AA, ^{t}RCD, ^{t}RP, ^{t}RAS, and ^{t}RC limits of a given data rate and speed bin and are applicable to the CL settings in the lower half of the table, provided they are applied in the correct clock range, which is noted. (Speed bin table notes can be found after the standard DDR5-8400 speed bin table.)

Table 358: DDR5-3200 Speed Bins and Operating Conditions

Speed Bin				DDR5-3200AN		DDR5-3200B		DDR5-3200BN		DDR5-3200C		Unit	Notes
CL-*n*RCD-*n*RP				24-24-24		26-26-26		26-26-26		28-28-28			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data			^{t}AA	15.000	22.222	16.250	22.222	16.250	22.222	17.500	22.222	ns	12
Activate-to-internal read or write delay time			^{t}RCD	15.000	–	16.250	–	16.250	–	17.500	–	ns	7
Row precharge time			^{t}RP	15.000	–	16.250	–	16.250	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	32.000	5×$^{t}REFI$	32.000	5×$^{t}REFI$	32.000	5×$^{t}REFI$	32.000	5×$^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	47.000	–	48.250	–	48.250	–	49.500	–	ns	7,8
CAS WRITE latency			CWL	CL - 2								*n*CK	
Speed Bin[5]	**^{t}AAmin (ns)[5]**	**^{t}RCDmin ^{t}RPmin (ns)[5]**	**READ CL[12]**	**Supported Frequency Down Bins**									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	^{t}CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	15.000	15.000	24	^{t}CK (AVG)	0.625	0.681	Reserved						ns	
Supported CL				22,24,26,28		22,26,28		22,26,28		22,28		*n*CK	

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Table 359: DDR5-3600 Speed Bins and Operating Conditions

Speed Bin				DDR5--3600AN		DDR5--3600B		DDR5--3600BN		DDR5--3600C			
CL-*n*RCD-*n*RP				26-26-26		30-30-30		30-30-30		32-32-32			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
READ command to first data			^{t}AA	14.444	22.222	16.250	22.222	16.666	22.222	17.500	22.222	ns	12
Activate-to-internal read or write delay time			^{t}RCD	14.444	–	16.250	–	16.666	–	17.500	–	ns	7
Row precharge time			^{t}RP	14.444	–	16.250	–	16.666	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	32.000	5×$^{t}REFI$	32	5×$^{t}REFI$	32.000	5×$^{t}REFI$	32.000	5×$^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	46.444	–	48.250	–	48.666	–	49.500	–	ns	7,8
CAS WRITE latency			CWL	CL - 2								*n*CK	
				Supported Frequency Down Bins									
Speed Bin[5]	$^{t}AAmin$ (ns)[5]	^{t}RCD-min $^{t}RPmin$ (ns)[5]	READ CL[12]	Symbol	Min	Max	Min	Max	Min	Max	Min	Min	Unit	Notes
–	20.952	–	22	^{t}CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	
3200C	17.500	17.500	28	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	^{t}CK (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	15.000	15.000	24	^{t}CK (AVG)	0.625	0.681	Reserved						ns	
3600C	17.777	17.777	32	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3200BN,B	16.666	16.666	30	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	14.444	14.444	26	^{t}CK (AVG)	0.555	<0.625	Reserved						ns	
Supported CL				22,24,26,28, 30,32		22,26,28,30,32		22,28,30,32		22,28,32			*n*CK	

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Table 360: DDR5-4000 Speed Bins and Operating Conditions

Speed Bin				DDR5-4000AN		DDR5-4000B		DDR5-4000BN		DDR5-4000C			
CL-*n*RCD-*n*RP				28-28-28		32-32-32		32-32-32		36-35-35			
Parameter	Symbol			Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
READ command to first data	^{t}AA			14.000	22.222	16.000	22.222	16.000	22.222	17.500	22.222	ns	12
Activate-to-internal read or write delay time	^{t}RCD			14.000	–	16.000	–	16.000	–	17.500	–	ns	7
Row precharge time	^{t}RP			14.000	–	16.000	–	16.000	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period	^{t}RAS			32.000	5×$^{t}REFI$	32.000	5×$^{t}REFI$	32.000	5×$^{t}REFI$	32.000	5×$^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period	^{t}RC (^{t}RAS + ^{t}RP)			46.000	–	48.000	–	48.000	–	49.500	–	ns	7,8
CAS WRITE latency	CWL			CL - 2								*n*CK	
Speed Bin[5]	**^{t}AAmin (ns)[5]**	**^{t}RCD-min ^{t}RP-min (ns)[5]**	**READ CL[12]**	**Supported Frequency Down Bins**									
				Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
–	20.952	–	22	^{t}CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	15.000	15.000	24	^{t}CK (AVG)	0.625	0.681	Reserved						ns	
3600C	17.777	17.777	32	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	14.444	14.444	26	^{t}CK (AVG)	0.555	<0.625	Reserved						ns	
4000C	18.000	17.500	36	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	Reserved		ns	
4000AN	14.000	14.000	28	^{t}CK (AVG)	0.500	<0.555	Reserved						ns	
Supported CL				22,24,26,28,30, 32 36		22,26 28,30,32,36		22,26,28,30,32,36		22,28,32,36		*n*CK	

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Table 361: DDR5-4400 Speed Bins and Operating Conditions

Speed Bin				DDR5-4400AN		DDR5-4400B		DDR5-4400BN		DDR5-4400C			
CL-*n*RCD-*n*RP				32-32-32		36-36-36		36-36-36		40-39-39			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
READ command to first data			^{t}AA	14.545	22.222	16.000	22.222	16.363	22.222	17.500	22.222	ns	12
Activate-to-internal read or write delay time			^{t}RCD	14.545	–	16.000	–	16.363	–	17.500	–	ns	7
Row precharge time			^{t}RP	14.545	–	16.000	–	16.363	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	46.545	–	48.000	–	48.363	–	49.500	–	ns	7,8
CAS WRITE latency			CWL	CL - 2									
Speed Bin[5]	$^{t}AAmin$ (ns)[5]	^{t}RCD-min ^{t}RP-min (ns)[5]	READ CL[12]	Supported Frequency Down Bins									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	^{t}CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN, B	16.250	16.250	26	^{t}CK (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	15.000	15.000	24	^{t}CK (AVG)	0.625	0.681	Reserved						ns	
3600C	17.777	17.777	32	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN, B	16.666	16.666	30	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	14.444	14.444	26	^{t}CK (AVG)	Reserved								ns	
4000C	18.000	17.500	36	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN, B	16.000	16.000	32	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	14.000	14.000	28	^{t}CK (AVG)	Reserved								ns	
4400C	18.181	17.727	40	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	

Table 361: DDR5-4400 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-4400AN		DDR5-4400B		DDR5-4400BN		DDR5-4400C		Unit	Notes
CL-*n*RCD-*n*RP					32-32-32		36-36-36		36-36-36		40-39-39			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
4400BN, B	16.363	16.363	36	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	14.545	14.545	32	^{t}CK (AVG)	0.454	<0.500	Reserved						ns	
Supported CL					22,24,26,28,30,32,36,40		22,26,28,30,32,36,40		22,28,30,32,36,40		22,28,32,36,40		*n*CK	

Table 362: DDR5-4800 Speed Bins and Operating Conditions

Speed Bin				DDR5-4800AN		DDR5-4800B		DDR5-4800BN		DDR5-4800C			
CL-*n*RCD-*n*RP				34-34-34		40-39-39		40-40-40		42-42-42			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
READ command to first data			^{t}AA	14.166	22.222	16.000	22.222	16.666	22.222	17.500	22.222	ns	12
Activate-to-internal read or write delay time			^{t}RCD	14.166	–	16.000	–	16.666	–	17.500	–	ns	7
Row precharge time			^{t}RP	14.166	–	16.000	–	16.666	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	46.166	–	48.000	–	48.666	–	49.500	–	ns	7,8
CAS WRITE latency			CWL	CL - 2								*n*CK	
Speed Bin[5]	$^{t}AAmin$ (ns)[5]	^{t}RCD-min $^{t}RPmin$ (ns)[5]	READ CL[12]	Supported Frequency Down Bins									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	^{t}CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	^{t}CK (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	15.000	15.000	24	^{t}CK (AVG)	0.625	0.681	Reserved						ns	
3600C	17.777	17.777	32	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	14.444	14.444	26	^{t}CK (AVG)	0.555	<0.625	Reserved						ns	
4000C	18.000	17.500	36	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	14.000	14.000	28	^{t}CK (AVG)	Reserved								ns	
4400C	18.181	17.727	40	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	Reserved				ns	
4400AN	14.545	14.545	32	^{t}CK (AVG)	0.454	<0.500	Reserved						ns	

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Table 362: DDR5-4800 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-4800AN		DDR5-4800B		DDR5-4800BN		DDR5-4800C		Unit	Notes
CL-*n*RCD-*n*RP					34-34-34		40-39-39		40-40-40		42-42-42			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
4800C	17.500	17.500	42	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	16.666	16.250	40	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	Reserved				ns	
4800AN	14.166	14.166	34	^{t}CK (AVG)	0.416	<0.454	Reserved						ns	
Supported CL					22,24,26,28,30, 32,34,36,40,42		22,26,28,30,32,36,40, 42		22,28,30,32,36,40,4 2		22,28,32,36,40,42		*n*CK	

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Table 363: DDR5-5200 Speed Bins and Operating Conditions

Speed Bin					DDR5-5200AN		DDR5-5200B		DDR5-5200BN		DDR5-5200C		Unit	Notes
CL-*n*RCD-*n*RP					38-38-38		42-42-42		42-42-42		46-46-46			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data				^{t}AA	14.615	22.222	16.000	22.222	16.153	22.222	17.500	22.222	ns	12
Activate-to-internal read or write delay time				^{t}RCD	14.615	–	16.000	–	16.153	–	17.500	–	ns	7
Row precharge time				^{t}RP	14.615	–	16.000	–	16.153	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period				^{t}RAS	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period				^{t}RC (^{t}RAS + ^{t}RP)	46.615	–	48.000	–	48.153	–	49.500	–	ns	7,8
CAS WRITE latency				CWL	CL - 2								*n*CK	
Speed Bin[5]	$^{t}AAmin$ (ns)[5]	^{t}RCD-min $^{t}RPmin$ (ns)[5]	READ CL[12]	Supported Frequency Down Bins Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	^{t}CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	15.000	15.000	24	^{t}CK (AVG)	0.625	0.681	Reserved						ns	
3600C	17.777	17.777	32	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	14.444	14.444	26	^{t}CK (AVG)	Reserved								ns	
4000C	18.000	17.500	36	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	14.000	14.000	28	^{t}CK (AVG)	Reserved								ns	
4400C	18.181	17.727	40	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	14.545	14.545	32	^{t}CK (AVG)	Reserved								ns	

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Table 363: DDR5-5200 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-5200AN		DDR5-5200B		DDR5-5200BN		DDR5-5200C		Unit	Notes
CL-*n*RCD-*n*RP					38-38-38		42-42-42		42-42-42		46-46-46			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
4800C	17.500	17.500	42	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	16.666	16.250	40	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800AN	14.166	14.166	34	^{t}CK (AVG)	Reserved								ns	
5200C	17.692	17.692	46	^{t}CK (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	^{t}CK (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	Reserved		ns	
5200AN	14.615	14.615	38	^{t}CK (AVG)	0.384	<0.416	Reserved						ns	
Supported CL					22,24,26,28,30, 32,36,38,40,42,46		22,26,28,30,32,36,40, 42,46		22,26,28,30,32,36, 40,42,46		22,28,32,36,40,42, 46		*n*CK	

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Table 364: DDR5-5600 Speed Bins and Operating Conditions

Speed Bin				DDR5-5600AN		DDR5-5600B		DDR5-5600BN		DDR5-5600C			
CL-*n*RCD-*n*RP				40-40-40		46-45-45		46-46-46		50-49-49			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
READ command to first data			^{t}AA	14.285	22.222	16.000	22.222	16.428	22.222	17.500	22.222	ns	12
Activate-to-internal read or write delay time			^{t}RCD	14.285	–	16.000	–	16.428	–	17.500	–	ns	7
Row precharge time			^{t}RP	14.285	–	16.000	–	16.428	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	46.285	–	48.000	–	48.428	–	49.500	–	ns	7,8
CAS WRITE latency			CWL	CL - 2								*n*CK	
Speed Bin[5]	$^{t}AAmin$ (ns)[5]	^{t}RCD-min $^{t}RPmin$ (ns)[5]	READ CL[12]	Supported Frequency Down Bins									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	^{t}CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	^{t}CK (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	15.000	15.000	24	^{t}CK (AVG)	0.625	0.681	Reserved						ns	
3600C	17.777	17.777	32	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	14.444	14.444	26	^{t}CK (AVG)	0.555	<0.625	Reserved						ns	
4000C	18.000	17.500	36	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	14.000	14.000	28	^{t}CK (AVG)	Reserved								ns	
4400C	18.181	17.727	40	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	Reserved				ns	
4400AN	14.545	14.545	32	^{t}CK (AVG)	0.454	<0.500	Reserved						ns	

Table 364: DDR5-5600 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-5600AN		DDR5-5600B		DDR5-5600BN		DDR5-5600C		Unit	Notes
CL-*n*RCD-*n*RP					40-40-40		46-45-45		46-46-46		50-49-49			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
4800C	17.500	17.500	42	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	16.666	16.250	40	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	Reserved				ns	
4800AN	14.166	14.166	34	^{t}CK (AVG)	Reserved								ns	
5200C	17.692	17.692	46	^{t}CK (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	^{t}CK (AVG)	0.384	<0.416	0.384	<0.416	Reserved				ns	
5200AN	14.615	14.615	38	^{t}CK (AVG)	0.384	<0.416	Reserved						ns	
5600C	17.857	17.500	50	^{t}CK (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	^{t}CK (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	Reserved		ns	
5600B	16.428	16.071	46	^{t}CK (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600AN	14.285	14.285	40	^{t}CK (AVG)	0.357	<0.384	Reserved						ns	
Supported CL					22,24,26,28,30, 32,36,38,40,42,46, 50		22,26,28,30,32,36,40, 42,46,50		22,28,30,32,36, 40,42,46,50		22,28,32,36,40,42, 46,50		*n*CK	

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Table 365: DDR5-6000 Speed Bins and Operating Conditions

Speed Bin				DDR5-6000AN		DDR5-6000B		DDR5-6000BN		DDR5-6000C			
CL-*n*RCD-*n*RP				42-42-42		48-48-48		48-48-48		54-53-53			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
READ command to first data			^{t}AA	14.000	22.222	16.000	22.222	16.000	22.222	17.500	22.222	ns	12
Activate-to-internal read or write delay time			^{t}RCD	14.000	–	16.000	–	16.000	–	17.500	–	ns	7
Row precharge time			^{t}RP	14.000	–	16.000	–	16.000	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	46.000	–	48.000	–	48.000	–	49.500	–	ns	7,8
CAS WRITE latency			CWL	CL - 2								*n*CK	
Speed Bin[5]	$^{t}AAmin$ (ns)[5]	^{t}RCD-min $^{t}RPmin$ (ns)[5]	READ CL[12]	Supported Frequency Down Bins									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	^{t}CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	15.000	15.000	24	^{t}CK (AVG)	0.625	0.681	Reserved						ns	
3600C	17.777	17.777	32	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	14.444	14.444	26	^{t}CK (AVG)	0.555	<0.625	Reserved						ns	
4000C	18.000	17.500	36	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	Reserved		ns	
4000AN	14.000	14.000	28	^{t}CK (AVG)	0.500	<0.555	Reserved						ns	
4400C	18.181	17.727	40	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	14.545	14.545	32	^{t}CK (AVG)	0.454	<0.500	Reserved						ns	

Table 365: DDR5-6000 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-6000AN		DDR5-6000B		DDR5-6000BN		DDR5-6000C		Unit	Notes
CL-*n*RCD-*n*RP					42-42-42		48-48-48		48-48-48		54-53-53			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
4800C	17.500	17.500	42	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	16.666	16.250	40	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800AN	14.166	14.166	34	^{t}CK (AVG)	0.416	<0.454	Reserved						ns	
5200C	17.692	17.692	46	^{t}CK (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	^{t}CK (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	Reserved		ns	
5200AN	14.615	14.615	38	^{t}CK (AVG)	0.384	<0.416	Reserved						ns	
5600C	17.857	17.500	50	^{t}CK (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	^{t}CK (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	Reserved		ns	
5600B	16.428	16.071	46	^{t}CK (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	Reserved		ns	
5600AN	14.285	14.285	40	^{t}CK (AVG)	0.357	<0.384	Reserved						ns	
6000C	18.000	17.666	54	^{t}CK (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	16.000	16.000	48	^{t}CK (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	Reserved		ns	
6000AN	14.000	14.000	42	^{t}CK (AVG)	0.333	<0.357	Reserved						ns	
Supported CL					22,24,26,28,30, 32,34,36,38,40,42, 46,48,50,54		22,26,28,30,32,36,40, 42,46,48,50,54		22,26,28,30,32,36, 40,42,46,48,50,54		22,28,32,36,40,42, 46,50,54		*n*CK	

Table 366: DDR5-6400 Speed Bins and Operating Conditions

Speed Bin			DDR5-6400AN		DDR5-6400B		DDR5-6400BN		DDR5-6400C			
CL-*n*RCD-*n*RP			46-46-46		52-52-52		52-52-52		56-56-56			
Parameter	Symbol		Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
READ command to first data	^{t}AA		14.375	22.222	16.000	22.222	16.250	22.222	17.500	22.222	ns	12
Activate-to-internal read or write delay time	^{t}RCD		14.375	–	16.000	–	16.250	–	17.500	–	ns	7
Row precharge time	^{t}RP		14.375	–	16.000	–	16.250	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period	^{t}RAS		32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period	^{t}RC (^{t}RAS + ^{t}RP)		46.375	–	48.000	–	48.250	–	49.500	–	ns	7,8
CAS WRITE latency	CWL		CL - 2								*n*CK	
Supported Frequency Down Bins												
Speed Bin[5]	$^{t}AAmin$ (ns)[5]	^{t}RCD-min ^{t}RP-min (ns)[5]	READ CL[12]	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	^{t}CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	15.000	15.000	24	^{t}CK (AVG)	0.625	0.681	Reserved						ns	
3600C	17.777	17.777	32	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	14.444	14.444	26	^{t}CK (AVG)	0.555	<0.625	Reserved						ns	
4000C	18.000	17.500	36	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	

Table 366: DDR5-6400 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-6400AN		DDR5-6400B		DDR5-6400BN		DDR5-6400C		Unit	Notes
CL-*n*RCD-*n*RP					46-46-46		52-52-52		52-52-52		56-56-56			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
4000BN,B	16.000	16.000	32	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	14.000	14.000	28	^{t}CK (AVG)	Reserved								ns	
4400C	18.181	17.727	40	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	14.545	14.545	32	^{t}CK (AVG)	0.454	<0.500	Reserved						ns	
4800C	17.500	17.500	42	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	16.666	16.250	40	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800AN	14.166	14.166	34	^{t}CK (AVG)	Reserved								ns	
5200C	17.692	17.692	46	^{t}CK (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	^{t}CK (AVG)	0.384	<0.416	0.384	<0.416	Reserved				ns	
5200AN	14.615	14.615	38	^{t}CK (AVG)	0.384	<0.416	Reserved						ns	
5600C	17.857	17.500	50	^{t}CK (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	^{t}CK (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	Reserved		ns	
5600B	16.428	16.071	46	^{t}CK (AVG)	0.357	<0.384	Reserved						ns	

Table 366: DDR5-6400 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-6400AN		DDR5-6400B		DDR5-6400BN		DDR5-6400C		Unit	Notes
CL-*n*RCD-*n*RP					46-46-46		52-52-52		52-52-52		56-56-56			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
5600AN	14.285	14.285	40	^{t}CK (AVG)	Reserved								ns	
6000C	18.000	17.666	54	^{t}CK (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	16.000	16.000	48	^{t}CK (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	Reserved		ns	
6000AN	14.000	14.000	42	^{t}CK (AVG)	Reserved								ns	
6400C	17.500	17.500	56	^{t}CK (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	16.250	16.250	52	^{t}CK (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	Reserved		ns	
6400AN	14.375	14.375	46	^{t}CK (AVG)	0.312	<0.333	Reserved						ns	
Supported CL					22,24,26,28,30, 32,36,38,40,42,46, 48,50,52,54,56		22,26,28,30,32,36,40, 42,46,48,50,52,54,56		22,26,28,30,32,36, 40,42,46,48,50,52, 54,56		22,28,32,36,40,42, 46,50,54,56		*n*CK	

Notes: 1. Minimum timing parameters are defined according to the rules in the Rounding Definitions and Algorithms section.
2. The translation of all timing parameters from ns values to *n*CK values must follow the Rounding Algorithm. The translation of ^{t}AA to CL follows the explicit combinations listed in the Speed Bin Tables.
3. The CL setting and CWL setting result in ^{t}CK(avg) MIN and ^{t}CK(avg) MAX requirements. When selecting ^{t}CK(avg), requirements from the CL setting, as well as requirements from the CWL setting, must be fulfilled.
4. Reserved settings are not allowed. User must program a different value.
5. This column shows the intended native speed bin timings to be replaced and supported when down clocking. This column does not necessarily show the actual minimum speed bin timings allowed and supported when down clocking because the timings could be faster according to the Rounding Algorithm and depending on the specific speed bin and down clock frequency combination.
6. 3DS DDR5-3200 AC timing applies if the device operates slower than the 2933 MT/s data rate. This is not limitd to only the Speed Bin Table timings.
7. Parameters apply from ^{t}CK,AVG (MIN) to ^{t}CK,AVG (MAX) at all standard JEDEC clock period values, as stated in the Speed Bin Tables.
8. ^{t}RC(min) is always greater than or equal to ^{t}RAS(min) + ^{t}RP(min), and when using the appropriate rounding algorithms, nRC(min) is always greater than or equal to nRAS(min) + nRP(min).
9. ^{t}CK(avg) MAX of 1.010ns (1980 MT/s data rate) is defined to allow for 1% SSC down-spreading at a data rate of 2000 MT/s according to JESD404-1.

10. Each speed bin lists the timing requirements that must be supported in order for a given device to be JEDEC-compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.
11. Any speed bin also supports functional operation at slower frequencies as shown in the table, which are not subject to production tests but are verified by design/characterization.
12. The CL Algorithm can be used to mathematically determine the valid CAS Latencies listed in the speed bin tables. The CL algorithm calculates supported CAS latencies by rounding the operating frequency up to the next fastest native speed bin (i.e., 3200 MT/s, 3600 MT/s...). Using the resulting ^{t}CK(avg) MIN and the bin target timings, the CL algorithm then uses the Rounding Algorithm to calculate the valid CAS latency. Because the DDR5 SDRAM specification only supports even CAS latencies, odd CAS latencies are rounded up to the next even CAS latency. The 1980-2100 MT/s data rate always uses CL22. If ^{t}AA (corrected) or ^{t} RCD ^{t}RP (corrected) are violated, the CL algorithm uses a slower combination of ^{t}AA (target) and ^{t}RCD ^{t}RP (target) to return slower valid CAS latencies. The DDR5 SDRAM can support up to four valid CAS latencies, CL(AN), CL(B), CL(BN), and CL(C) for a given frequency. ^{t}AA (corrected) and ^{t}RCD ^{t}RP (corrected) are calculated by reducing ^{t}AA(min), ^{t}RCD(min), and ^{t}RP(min) by the Rounding Algorithm correction factor. The proper setting of CL shall be determined by the memory controller, either by using the Speed bin tables or by using the CL Algorithm, or by some other means. Refer to the Rounding Definitions and Algorithm section for more information.

```
// Variables already defined in other areas of the DDR5 SDRAM specification
CorrFact       = 0.30                                          // (%)   Rounding Algorithm correction factor
ScaledCorrFact = 997                                           //       Scaled correction factor (1000*(1-0.30%))
tCKreal        =1011-952, 682-238                              // (ps)  Real application tCK(AVG) (1980-2100MT/s, 2933-8400MT/s)
tAAmin         MONO=14000-17500, 3DS=16000-20000               // (ps)  From Speed Bin Tables and DIMM SPD bytes 30-31
tRCDtRPmin     MONO=14000-17500, 3DS=14000-17500               // (ps)  From Speed Bin Tables and DIMM SPD bytes 32-33 (tRCD=tRP)
tAAcorr        = TRUNC(tAAmin*ScaledCorrFactor/1000)           // (ps)  Corrected tAA(min) per the Rounding Algorithm rules
tRCDtRPcorr    = TRUNC(tRCDtRPmin*ScaledCorrFactor/1000)       // (ps)  Corrected tRCD(min), tRP(min) per the Rounding Algorithm
FUNC[RA(targ)] = TRUNC((targ*ScaledCorrFact/tCKstd+1000)/1000) // (nCK) Use Rounding Algorithm to convert bin target timing to nCK
// Round tCKreal down to the next faster standard frequency (tCK in ps)
IF (TRUNC(2000000/(2000*99%))>=TRUNC(tCKreal)>=TRUNC(2000000/(2000*105%)))             // Check for  1980-2100 nominal data rates
   tCKstd=TRUNC(2000000/2000)                                                          // Assign standard 2000 tCK (ps)
ELSE IF (TRUNC(2000000/(2000+7*(133+1/3)))>=TRUNC(tCKreal)>=TRUNC(2000000/3200))     // Check for  2933-3200 nominal data rates
   tCKstd=TRUNC(2000000/3200)                                                          // Assign standard 3200 tCK (ps)
ELSE
   FOR (DataRateNom=3200; DataRateNom<=8000; DataRateNom=DataRateNom+400)              // Check for >3200-8400 nominal data rates
      IF (TRUNC(2000000/DataRateNom)>TRUNC(tCKreal)>=TRUNC(2000000/(DataRateNom+400)))
         tCKstd=TRUNC(2000000/(DataRateNom+400))                                       // Assign standard 3600-8400 tCK (ps)
      ELSE
         tCKstd=RESERVED                                                             // No valid data rate found

// Timing targets (ps) that have been used to define the Speed Bin Tables
// MONO targets                3DS targets
   BinAN_tAAtarg      = 14000 BinAN_tAAtarg      = 16000         // tAA target for AN bins
   BinB__tAAtarg      = 16000 BinB__tAAtarg      = 16500         // tAA target for AN, B bins
   BinBN_tAAtarg      = 16000 BinBN_tAAtarg      = 16500         // tAA target for AN, B, BN bins
   BinC__tAAtarg      = 17500 BinC__tAAtarg      = 20000         // tAA target for AN, B, BN, C bins
   BinAN_tRCDtRPtarg = 14000 BinAN_tRCDtRPtarg = 14000         // tRCD, tRP target for AN bins
   BinBN_tRCDtRPtarg = 16000 BinBN_tRCDtRPtarg = 16000         // tRCD, tRP target for AN, B, BN bins
   BinC__tRCDtRPtarg = 17500 BinC__tRCDtRPtarg = 17500         // tRCD, tRP target for AN, B, BN, C bins
IF (TRUNC(2000000/3600)>tCKstd)                                // tRCD, tRP target for B bins is frequency dependent
   BinB__tRCDtRPtarg = 16000 BinB__tRCDtRPtarg = 16000         // tRCD, tRP target for AN, B bins data rates faster than 3600
ELSE
   // 16250=(2000000/3200)*EVEN(TRUNC((BinB__tRCDtRPtarg*ScaledCorrFact/(2000000/3200)+1000)/1000))
```

```
   BinB__tRCDtRPtarg = 16250 BinB__tRCDtRPtarg = 16250         // tRCD, tRP target for AN, B bins for data rates 3600 and slower

// CL Algorithm using variables defined above
// Up to four valid CL's can be returned for a specific freq: CL(AN), CL(B), CL(BN), CL(C), depending on tAAmin, tRCDmin, tRPmin
// The B and BN bins return the same CL
// Only even CL's (not odd CL's) are valid per the DDR5 SDRAM specification
// nRCD, nRP are only even at standard native frequencies for the AN, BN bins (can be even or odd at intermediate frequencies)
// nRCD, nRP may be even or odd at standard native frequencies for the B, C bins (can be even or odd at intermediate frequencies)
IF (TRUNC(2000000/2000)=tCKstd)                                 // CL22 is the only valid CL for 1980-2100 data rates
   CL(AN)=22                                                    // Valid even CL for AN bins
   CL(B )=22                                                    // Valid even CL for AN, B, bins
   CL(BN)=22                                                    // Valid even CL for AN, B, BN bins
   CL(C )=22                                                    // Valid even CL for AN, B, BN, C bins
ELSE IF (TRUNC(2000000/3200)>=tCKstd>=TRUNC(2000000/8400))      // Valid CL for 2933-8400 data rates
   IF      ((EVEN(RA(BinAN_tAAtarg))*tCKstd>=tAAcorr)AND(EVEN(RA(BinAN_tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even only
      CL(AN)=EVEN(RA(BinAN_tAAtarg))                            // Valid even CL for AN bins
      CL(B )=EVEN(RA(BinB__tAAtarg))                            // Valid even CL for AN, B bins
      CL(BN)=EVEN(RA(BinBN_tAAtarg))                            // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                            // Valid even CL for AN, B, BN, C bins
   ELSE IF ((EVEN(RA(BinB__tAAtarg))*tCKstd>=tAAcorr)AND(    (RA(BinB__tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even, odd
      CL(AN)=RESERVED                                           // Valid even CL for AN bins
      CL(B )=EVEN(RA(BinB__tAAtarg))                            // Valid even CL for AN, B bins
      CL(BN)=EVEN(RA(BinBN_tAAtarg))                            // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                            // Valid even CL for AN, B, BN, C bins
   ELSE IF ((EVEN(RA(BinBN_tAAtarg))*tCKstd>=tAAcorr)AND(EVEN(RA(BinBN_tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even only
      CL(AN)=RESERVED                                           // Valid even CL for AN bins
      CL(B )=RESERVED                                           // Valid even CL for AN, B bins
      CL(BN)=EVEN(RA(BinBN_tAAtarg))                            // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                            // Valid even CL for AN, B, BN, C bins
   ELSE IF ((EVEN(RA(BinC__tAAtarg))*tCKstd>=tAAcorr)AND(    (RA(BinC__tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even, odd
      CL(AN)=RESERVED                                           // Valid even CL for AN bins
      CL(B )=RESERVED                                           // Valid even CL for AN, B bins
      CL(BN)=RESERVED                                           // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                            // Valid even CL for AN, B, BN, C bins
   ELSE                                                         // No valid CL found (tAAmin, tRCDmin, tRPmin are too slow)
      CL(AN)=RESERVED                                           // Valid even CL for AN bins
      CL(B )=RESERVED                                           // Valid even CL for AN, B bins
      CL(BN)=RESERVED                                           // Valid even CL for AN, B, BN bins
      CL(C )=RESERVED                                           // Valid even CL for AN, B, BN, C bins
ELSE                                                            // No valid data rate found
   CL(AN)=RESERVED                                              // Valid even CL for AN bins
   CL(B )=RESERVED                                              // Valid even CL for AN, B bins
   CL(BN)=RESERVED                                              // Valid even CL for AN, B, BN bins
   CL(C )=RESERVED                                              // Valid even CL for AN, B, BN, C bins
```

Table 367: DDR5-6800 Speed Bins and Operating Conditions

Speed Bin				DDR5-6800AN		DDR5-6800B		DDR5-6800BN		DDR5-6800C		Unit	Notes
CL-*n*RCD-*n*RP				TBD		TBD		TBD		TBD			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data			^{t}AA	TBD	–	TBD	–	TBD	–	TBD	–	ns	12
Activate-to-internal read or write delay time			^{t}RCD	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
Row precharge time			^{t}RP	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	TBD	–	TBD	–	TBD	–	TBD	–	ns	7,8
CAS WRITE latency			CWL	CL - 2								*n*CK	
Speed Bin[5]	**^{t}AAmin (ns)[5]**	**^{t}RCDmin ^{t}RPmin (ns)[5]**	**READ CL[12]**	**Supported Frequency Down Bins**									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
				^{t}CK (AVG)									ns	6,9
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
Supported CL													*n*CK	

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Table 368: DDR5-7200 Speed Bins and Operating Conditions

Speed Bin				DDR5-7200AN		DDR5-7200B		DDR5-7200BN		DDR5-7200C		Unit	Notes
CL-*n*RCD-*n*RP				TBD		TBD		TBD		TBD			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data			^{t}AA	TBD	–	TBD	–	TBD	–	TBD	–	ns	12
Activate-to-internal read or write delay time			^{t}RCD	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
Row precharge time			^{t}RP	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	TBD	–	TBD	–	TBD	–	TBD	–	ns	7,8
CAS WRITE latency			CWL	CL - 2								*n*CK	
Speed Bin[5]	**^{t}AAmin (ns)[5]**	**^{t}RCDmin ^{t}RPmin (ns)[5]**	**READ CL[12]**	**Supported Frequency Down Bins**									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
				^{t}CK (AVG)									ns	6,9
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
Supported CL													*n*CK	

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Table 369: DDR5-7600 Speed Bins and Operating Conditions

Speed Bin				DDR5-7600AN		DDR5-7600B		DDR5-7600BN		DDR5-7600C		Unit	Notes
CL-*n*RCD-*n*RP				TBD		TBD		TBD		TBD			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data			^{t}AA	TBD	–	TBD	–	TBD	–	TBD	–	ns	12
Activate-to-internal read or write delay time			^{t}RCD	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
Row precharge time			^{t}RP	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	TBD	–	TBD	–	TBD	–	TBD	–	ns	7,8
CAS WRITE latency			CWL	CL - 2								*n*CK	
Speed Bin[5]	**^{t}AAmin (ns)[5]**	**^{t}RCDmin ^{t}RPmin (ns)[5]**	**READ CL[12]**	**Supported Frequency Down Bins**									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
				^{t}CK (AVG)									ns	6,9
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
Supported CL													*n*CK	

Table 370: DDR5-8000 Speed Bins and Operating Conditions

Speed Bin				DDR5-8000AN		DDR5-8000B		DDR5-8000BN		DDR5-8000C		Unit	Notes
CL-*n*RCD-*n*RP				TBD		TBD		TBD		TBD			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data			^{t}AA	TBD	–	TBD	–	TBD	–	TBD	–	ns	12
Activate-to-internal read or write delay time			^{t}RCD	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
Row precharge time			^{t}RP	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	TBD	–	TBD	–	TBD	–	TBD	–	ns	7,8
CAS WRITE latency			CWL	CL - 2								*n*CK	
Speed Bin[5]	**^{t}AAmin (ns)[5]**	**^{t}RCDmin ^{t}RPmin (ns)[5]**	**READ CL[12]**	**Supported Frequency Down Bins**									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
				^{t}CK (AVG)									ns	6,9
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
Supported CL													*n*CK	

Table 371: DDR5-8400 Speed Bins and Operating Conditions

Speed Bin				DDR5-8400AN		DDR5-8400B		DDR5-8400BN		DDR5-8400C		Unit	Notes
CL-*n*RCD-*n*RP				TBD		TBD		TBD		TBD			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data			^{t}AA	TBD	–	TBD	–	TBD	–	TBD	–	ns	12
Activate-to-internal read or write delay time			^{t}RCD	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
Row precharge time			^{t}RP	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	TBD	–	TBD	–	TBD	–	TBD	–	ns	7,8
CAS WRITE latency			CWL	CL - 2								*n*CK	
Speed Bin[5]	**^{t}AAmin (ns)[5]**	**^{t}RCDmin ^{t}RPmin (ns)[5]**	**READ CL[12]**	**Supported Frequency Down Bins**									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
				^{t}CK (AVG)									ns	6,9
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
Supported CL													*n*CK	

Table 372: DDR5-8800 Speed Bins and Operating Conditions

Speed Bin				DDR5-8800AN		DDR5-8800B		DDR5-8800BN		DDR5-8800C		Unit	Notes
CL-*n*RCD-*n*RP				TBD		TBD		TBD		TBD			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data			^{t}AA	TBD	–	TBD	–	TBD	–	TBD	–	ns	12
Activate-to-internal read or write delay time			^{t}RCD	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
Row precharge time			^{t}RP	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	TBD	–	TBD	–	TBD	–	TBD	–	ns	7,8
CAS WRITE latency			CWL	CL - 2								*n*CK	
Speed Bin[5]	**^{t}AAmin (ns)[5]**	**^{t}RCDmin ^{t}RPmin (ns)[5]**	**READ CL[12]**	**Supported Frequency Down Bins**									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
				^{t}CK (AVG)									ns	6,9
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
Supported CL													*n*CK	

Speed Bin Tables by Speed Grade: 3DS

DDR5 SDRAM timing is primarily covered by two types of tables: the speed bin tables in this section and the tables found in the Electrical Characteristics and AC Timing Parameters section. The speed bin tables on the following pages list the ^{t}AA, ^{t}RCD, ^{t}RP, ^{t}RAS, and ^{t}RC limits of a given data rate and speed bin and are applicable to the CL settings in the lower half of the table, provided they are applied in the correct clock range, which is noted. (3DS speed bin table notes can be found after the 3DS DDR5-6400 speed bin table.)

Table 373: 3DS DDR5-3200 Speed Bins and Operating Conditions

Speed Bin				DDR5-3200AN 3DS		DDR5-3200B 3DS		DDR5-3200BN 3DS		DDR5-3200C 3DS		Unit	Notes
CL-*n*RCD-*n*RP				26-24-24		30-26-26		30-26-26		32-28-28			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data			^{t}AA	16.250	22.222	18.750	22.222	18.750	22.222	20.000	22.222	ns	12
Activate-to-internal read or write delay time			^{t}RCD	15.000	–	16.250	–	16.250	–	17.500	–	ns	7
Row precharge time			^{t}RP	15.000	–	16.250	–	16.250	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	32.000	5×$^{t}REFI$	32.000	5×$^{t}REFI$	32.000	5×$^{t}REFI$	32.000	5×$^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	45.750	–	48.250	–	48.250	–	49.500	–	ns	7,8
CAS WRITE latency			CWL	CL - 2								*n*CK	
Speed Bin[5]	**^{t}AAmin (ns)[5]**	**^{t}RCDmin ^{t}RPmin (ns)[5]**	**READ CL[12]**	**Supported Frequency Down Bins**									
				Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
–	20.952	–	22	^{t}CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	16.250	15.000	26	^{t}CK (AVG)	0.625	0.681	Reserved						ns	
Supported CL				22,26,30,32		22,30,32		22,30,32		22,32		*n*CK	

Table 374: 3DS DDR5-3600 Speed Bins and Operating Conditions

Speed Bin				DDR5-3600AN 3DS		DDR5-3600B 3DS		DDR5-3600ABN 3DS		DDR5-3600C 3DS			
CL-*n*RCD-*n*RP				26-26-26		30-30-30		30-30-30		32-32-32			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
READ command to first data			^{t}AA	16.666	22.222	18.750	22.222	18.888	22.222	20.000	22.222	ns	12
Activate-to-internal read or write delay time			^{t}RCD	14.444	–	16.250	–	16.666	–	17.500	–	ns	7
Row precharge time			^{t}RP	14.444	–	16.250	–	16.666	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	32.000	5×$^{t}REFI$	32.000	5×$^{t}REFI$	32.000	5×$^{t}REFI$	32.000	5×$^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	46.444	–	48.250	–	48.666	–	49.500	–	ns	7,8
CAS WRITE latency			CWL	CL - 2								*n*CK	
Speed Bin[5]	$^{t}AAmin$ (ns)[5]	^{t}RCD-min $^{t}RPmin$ (ns)[5]	READ CL[12]	Supported Frequency Down Bins									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	^{t}CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	^{t}CK (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	16.250	15.000	26	^{t}CK (AVG)	Reserved								ns	
3600C	20.000	17.777	36	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	16.666	14.444	30	^{t}CK (AVG)	0.555	<0.625	Reserved						ns	
Supported CL				22,30,32.34.36		22,30,32,34,36		22,32,34,36		22,32,36		*n*CK	

Table 375: 3DS DDR5-4000 Speed Bins and Operating Conditions

Speed Bin		DDR5-4000AN 3DS		DDR5-4000B 3DS		DDR5-4000BN 3DS		DDR5-4000C 3DS			
CL-*n*RCD-*n*RP		28-28-28		32-32-32		32-32-32		36-35-35			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
READ command to first data	^{t}AA	16.000	22.222	18.750	22.222	19.000	22.222	20.000	22.222	ns	12
Activate-to-internal read or write delay time	^{t}RCD	14.000	–	16.000	–	16.000	–	17.500	–	ns	7
Row precharge time	^{t}RP	14.000	–	16.000	–	16.000	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period	^{t}RAS	32.000	5×$^{t}REFI$	32.000	5×$^{t}REFI$	32.000	5×$^{t}REFI$	32.000	5×$^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period	^{t}RC (^{t}RAS + ^{t}RP)	46.000	–	48.000	–	48.000	–	49.500	–	ns	7,8
CAS WRITE latency	CWL	CL - 2								*n*CK	

Speed Bin[5]	^{t}AAmin (ns)[5]	^{t}RCD-min ^{t}RP-min (ns)[5]	READ CL[12]	Supported Frequency Down Bins									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	^{t}CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	16.250	15.000	26	^{t}CK (AVG)	0.625	0.681	Reserved						ns	
3600C	20.000	17.777	36	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	16.666	14.444	30	^{t}CK (AVG)	0.555	<0.625	Reserved						ns	
4000C	20.000	17.500	40	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	Reserved		ns	
4000AN	16.000	14.000	32	^{t}CK (AVG)	0.500	<0.555	Reserved						ns	
Supported CL					22,26,30, 32,34,36,38,40		22,30,32,34,36,38, 40		22,32,36,38,40		22,32,36,40		*n*CK	

Table 376: 3DS DDR5-4400 Speed Bins and Operating Conditions

Speed Bin				DDR5-4400AN 3DS		DDR5-4400B 3DS		DDR5-4400BN 3DS		DDR5-4400C 3DS		Unit	Notes
CL-*n*RCD-*n*RP				36-32-32		42-36-36		42-36-36		44-39-39			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data			^{t}AA	16.363	22.222	18.750	22.222	19.090	22.222	20.000	22.222	ns	12
Activate-to-internal read or write delay time			^{t}RCD	14.545	–	16.000	–	16.363	–	17.500	–	ns	7
Row precharge time			^{t}RP	14.545	–	16.000	–	16.363	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	46.545	–	48.000	–	48.363	–	49.500	–	ns	7,8
CAS WRITE latency			CWL	CL - 2									
Speed Bin[5]	$^{t}AAmin$ (ns)[5]	^{t}RCD-min ^{t}RP-min (ns)[5]	READ CL[12]	Supported Frequency Down Bins									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	^{t}CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	^{t}CK (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	16.250	15.000	26	^{t}CK (AVG)	Reserved								ns	
3600C	20.000	17.777	36	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	Reserved				ns	
3600AN	16.666	14.444	30	^{t}CK (AVG)	Reserved								ns	
4000C	20.000	17.500	40	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	16.000	14.000	32	^{t}CK (AVG)	Reserved								ns	
4400C	20.000	17.727	44	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	

Table 376: 3DS DDR5-4400 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-4400AN 3DS		DDR5-4400B 3DS		DDR5-4400BN 3DS		DDR5-4400C 3DS		Unit	Notes
CL-*n*RCD-*n*RP					36-32-32		42-36-36		42-36-36		44-39-39			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
4400AN	16.363	14.545	36	^{t}CK (AVG)	0.454	<0.500	Reserved						ns	
Supported CL					22,30,32,34,36,38, 40,42,44		22,30,32,34,36,38, 40,42,44		22,32,36,40,42,44		22,32,36,40,44		*n*CK	

Table 377: 3DS DDR5-4800 Speed Bins and Operating Conditions

Speed Bin				DDR5-4800AN 3DS		DDR5-4800B 3DS		DDR5-4800BN 3DS		DDR5-4800C 3DS			
CL-*n*RCD-*n*RP				40-34-34		46-39-39		46-40-40		48-42-42			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
READ command to first data			^{t}AA	16.666	22.222	18.750	22.222	19.166	22.222	20.000	22.222	ns	12
Activate-to-internal read or write delay time			^{t}RCD	14.166	–	16.000	–	16.666	–	17.500	–	ns	7
Row precharge time			^{t}RP	14.166	–	16.000	–	16.666	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	46.166	–	48.000	–	48.666	–	49.500	–	ns	7,8
CAS WRITE latency			CWL	CL - 2								*n*CK	
Speed Bin[5]	$^{t}AAmin$ (ns)[5]	^{t}RCD-min $^{t}RPmin$ (ns)[5]	READ CL[12]	Supported Frequency Down Bins									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	^{t}CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	^{t}CK (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	16.250	15.000	26	^{t}CK (AVG)	Reserved								ns	
3600C	20.000	17.777	36	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	Reserved				ns	
3600AN	16.666	14.444	30	^{t}CK (AVG)	0.555	<0.625	Reserved						ns	
4000C	20.000	17.500	40	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	16.000	14.000	32	^{t}CK (AVG)	Reserved								ns	
4400C	20.000	17.727	44	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	Reserved				ns	
4400AN	16.363	14.545	36	^{t}CK (AVG)	Reserved								ns	

Table 377: 3DS DDR5-4800 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-4800AN 3DS		DDR5-4800B 3DS		DDR5-4800BN 3DS		DDR5-4800C 3DS		Unit	Notes
CL-*n*RCD-*n*RP					40-34-34		46-39-39		46-40-40		48-42-42			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
4800C	20.000	17.500	48	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	19.166	16.250	46	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	Reserved				ns	
4800AN	16.666	14.166	40	^{t}CK (AVG)	0.416	<0.454	Reserved						ns	
Supported CL					22,30,32,34,36,38, 40,42,44,46,48		22,30,32,34,36,38,40, 42,44,46,48		22,32,36,40,44,46, 48		22,32,36,40,44,48		*n*CK	

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Table 378: 3DS DDR5-5200 Speed Bins and Operating Conditions

Speed Bin					DDR5-5200AN 3DS		DDR5-5200B 3DS		DDR5-5200BN 3DS		DDR5-5200C 3DS			
CL-*n*RCD-*n*RP					42-38-38		50-42-42		50-42-42		52-46-46			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
READ command to first data				^{t}AA	16.153	22.222	18.750	22.222	19.230	22.222	20.000	22.222	ns	12
Activate-to-internal read or write delay time				^{t}RCD	14.615	–	16.000	–	16.153	–	17.500	–	ns	7
Row precharge time				^{t}RP	14.615	–	16.000	–	16.153	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period				^{t}RAS	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period				^{t}RC (^{t}RAS + ^{t}RP)	46.615	–	48.000	–	48.153	–	49.500	–	ns	7,8
CAS WRITE latency				CWL	CL - 2								*n*CK	
Speed Bin[5]	$^{t}AAmin$ (ns)[5]	^{t}RCD-min $^{t}RPmin$ (ns)[5]	READ CL[12]	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	^{t}CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	^{t}CK (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	16.250	15.000	26	^{t}CK (AVG)	0.625	0.681	Reserved						ns	
3600C	20.000	17.777	36	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	Reserved				ns	
3600AN	16.666	14.444	30	^{t}CK (AVG)	Reserved								ns	
4000C	20.000	17.500	40	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	16.000	14.000	32	^{t}CK (AVG)	Reserved								ns	
4400C	20.000	17.727	44	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	Reserved				ns	
4400AN	16.363	14.545	36	^{t}CK (AVG)	Reserved								ns	

Table 378: 3DS DDR5-5200 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-5200AN 3DS		DDR5-5200B 3DS		DDR5-5200BN 3DS		DDR5-5200C 3DS		Unit	Notes
CL-*n*RCD-*n*RP					42-38-38		50-42-42		50-42-42		52-46-46			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
4800C	20.000	17.500	48	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	Reserved				ns	
4800B	19.166	16.250	46	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	Reserved				ns	
4800AN	16.666	14.166	40	^{t}CK (AVG)	Reserved								ns	
5200C	20.000	17.692	52	^{t}CK (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	19.230	16.153	50	^{t}CK (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	Reserved		ns	
5200AN	16.153	14.615	42	^{t}CK (AVG)	0.384	<0.416	Reserved						ns	
Supported CL					22,26,30,32, 34,36,38,40,42,44, 46,48,50,52		22,30,32,34,36,38,40, 42,44,46,48,50,52		22,32,36, 40,44,48,50,52		22,32,36,40,44, 48,52		*n*CK	

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Table 379: 3DS DDR5-5600 Speed Bins and Operating Conditions

Speed Bin				DDR5-5600AN 3DS		DDR5-5600B 3DS		DDR5-5600BN 3DS		DDR5-5600C 3DS			
CL-*n*RCD-*n*RP				46-40-40		52-45-45		52-46-46		56-49-49			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
READ command to first data			^{t}AA	16.428	22.222	18.571	22.222	18.571	22.222	20.000	22.222	ns	12
Activate-to-internal read or write delay time			^{t}RCD	14.285	–	16.000	–	16.428	–	17.500	–	ns	7
Row precharge time			^{t}RP	14.285	–	16.000	–	16.428	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	46.285	–	48.000	–	48.428	–	49.500	–	ns	7,8
CAS WRITE latency			CWL	CL - 2								*n*CK	
Speed Bin[5]	$^{t}AAmin$ (ns)[5]	^{t}RCD-min $^{t}RPmin$ (ns)[5]	READ CL[12]	Supported Frequency Down Bins									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	^{t}CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	^{t}CK (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	16.250	15.000	26	^{t}CK (AVG)	Reserved								ns	
3600C	20.000	17.777	36	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	16.666	14.444	30	^{t}CK (AVG)	0.555	<0.625	Reserved						ns	
4000C	20.000	17.500	40	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	16.000	14.000	32	^{t}CK (AVG)	Reserved								ns	
4400C	20.000	17.727	44	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	Reserved				ns	
4400AN	16.363	14.545	36	^{t}CK (AVG)	Reserved								ns	

Table 379: 3DS DDR5-5600 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-5600AN 3DS		DDR5-5600B 3DS		DDR5-5600BN 3DS		DDR5-5600C 3DS		Unit	Notes
CL-*n*RCD-*n*RP					46-40-40		52-45-45		52-46-46		56-49-49			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
4800C	20.000	17.500	48	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	19.166	16.250	46	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	Reserved				ns	
4800AN	16.666	14.166	40	^{t}CK (AVG)	Reserved								ns	
5200C	20.000	17.692	52	^{t}CK (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	19.230	16.153	50	^{t}CK (AVG)	0.384	<0.416	0.384	<0.416	Reserved				ns	
5200AN	16.153	14.615	42	^{t}CK (AVG)	Reserved								ns	
5600C	20.000	17.500	56	^{t}CK (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	52	^{t}CK (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	Reserved		ns	
5600B	18.571	16.071	52	^{t}CK (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600AN	16.428	14.285	46	^{t}CK (AVG)	0.357	<0.384	Reserved						ns	
Supported CL					22,30,32, 34,36,38,40,42,44, 46,48,50,52,56		22,30,32,34,36,38,40, 42,44,46,48,50,52,56		22,32,34,36, 38,40,42,44,46,48, 50,52,56		22,32,36,40,44, 48,52,56		*n*CK	

Table 380: 3DS DDR5-6000 Speed Bins and Operating Conditions

Speed Bin				DDR5-6000AN 3DS		DDR5-6000B 3DS		DDR5-6000BN 3DS		DDR5-6000C 3DS			
CL-*n*RCD-*n*RP				48-42-42		56-48-48		56-48-48		60-53-53			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
READ command to first data			^{t}AA	16.000	22.222	18.571	22.222	18.666	22.222	20.000	22.222	ns	12
Activate-to-internal read or write delay time			^{t}RCD	14.000	–	16.000	–	16.000	–	17.500	–	ns	7
Row precharge time			^{t}RP	14.000	–	16.000	–	16.000	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	46.000	–	48.000	–	48.000	–	49.500	–	ns	7,8
CAS WRITE latency			CWL	CL - 2								*n*CK	
Speed Bin[5]	$^{t}AAmin$ (ns)[5]	^{t}RCD-min $^{t}RPmin$ (ns)[5]	READ CL[12]	Supported Frequency Down Bins									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	^{t}CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	16.250	15.000	26	^{t}CK (AVG)	0.625	0.681	Reserved						ns	
3600C	20.000	17.777	36	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	16.666	14.444	30	^{t}CK (AVG)	0.555	<0.625	Reserved						ns	
4000C	20.000	17.500	40	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	Reserved		ns	
4000AN	16.000	14.000	32	^{t}CK (AVG)	0.500	<0.555	Reserved						ns	
4400C	20.000	17.727	44	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	16.363	14.545	36	^{t}CK (AVG)	Reserved								ns	

Table 380: 3DS DDR5-6000 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-6000AN 3DS		DDR5-6000B 3DS		DDR5-6000BN 3DS		DDR5-6000C 3DS		Unit	Notes
CL-*n*RCD-*n*RP					48-42-42		56-48-48		56-48-48		60-53-53			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
4800C	20.000	17.500	48	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	19.166	16.250	46	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800AN	16.666	14.166	40	^{t}CK (AVG)			Reserved						ns	
5200C	20.000	17.692	52	^{t}CK (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	19.230	16.153	50	^{t}CK (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	Reserved		ns	
5200AN	16.153	14.615	42	^{t}CK (AVG)	0.384	<0.416	Reserved						ns	
5600C	20.000	17.500	56	^{t}CK (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	52	^{t}CK (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600B	18.571	16.071	52	^{t}CK (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600AN	16.428	14.285	46	^{t}CK (AVG)	0.357	<0.384	Reserved						ns	
6000C	20.000	17.666	60	^{t}CK (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	16.000	16.000	56	^{t}CK (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	Reserved		ns	
6000AN	14.000	14.000	48	^{t}CK (AVG)	0.333	<0.357	Reserved						ns	
Supported CL					22,26,30,32, 34,36,38,40,42,44, 46,48,50,52,56, 60		22,30,32,34,36,38, 40,42,44,46,48,50, 52,56, 60		22,30,32,34,36, 38,40,42,44,46,48, 50,52,56,60		22,32,36,40,44, 48,52,56,60		*n*CK	

Table 381: 3DS DDR5-6400 Speed Bins and Operating Conditions

Speed Bin					DDR5-6400AN 3DS		DDR5-6400B 3DS		DDR5-6400BN 3DS		DDR5-6400C 3DS			
CL-*n*RCD-*n*RP					52-46-46		60-52-52		60-52-52		64-56-56			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
READ command to first data				^{t}AA	16.250	22.222	18.571	22.222	18.750	22.222	20.000	22.222	ns	12
Activate-to-internal read or write delay time				^{t}RCD	14.375	–	16.000	–	16.250	–	17.500	–	ns	7
Row precharge time				^{t}RP	14.375	–	16.000	–	16.250	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period				^{t}RAS	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	32.000	5 × $^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period				^{t}RC (^{t}RAS + ^{t}RP)	46.375	–	48.000	–	48.250	–	49.500	–	ns	7,8
CAS WRITE latency				CWL	CL - 2								*n*CK	
Speed Bin[5]	$^{t}AAmin$ (ns)[5]	^{t}RCD-min $^{t}RPmin$ (ns)[5]	READ CL[12]	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	^{t}CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	^{t}CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	16.250	15.000	26	^{t}CK (AVG)	0.625	0.681	Reserved						ns	
3600C	20.000	17.777	36	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	^{t}CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	16.666	14.444	30	^{t}CK (AVG)	0.555	<0.625	Reserved						ns	
4000C	20.000	17.500	40	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	^{t}CK (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	16.000	14.000	32	^{t}CK (AVG)	Reserved								ns	
4400C	20.000	17.727	44	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	^{t}CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	16.363	14.545	36	^{t}CK (AVG)	0.454	<0.500	Reserved						ns	

Table 381: 3DS DDR5-6400 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-6400AN 3DS		DDR5-6400B 3DS		DDR5-6400BN 3DS		DDR5-6400C 3DS		Unit	Notes
CL-*n*RCD-*n*RP					52-46-46		60-52-52		60-52-52		64-56-56			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
4800C	20.000	17.500	48	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	19.166	16.250	46	^{t}CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800AN	16.666	14.166	40	^{t}CK (AVG)	Reserved								ns	
5200C	20.000	17.692	52	^{t}CK (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	19.230	16.153	50	^{t}CK (AVG)	0.384	<0.416	0.384	<0.416	Reserved				ns	
5200AN	16.153	14.615	42	^{t}CK (AVG)	Reserved								ns	
5600C	20.000	17.500	56	^{t}CK (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	52	^{t}CK (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600B	18.571	16.071	52	^{t}CK (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600AN	16.428	14.285	46	^{t}CK (AVG)	Reserved								ns	
6000C	20.000	17.666	60	^{t}CK (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	18.666	16.000	56	^{t}CK (AVG)	0.333	<0.357	0.333	<0.357	Reserved				ns	
6000AN	16.600	14.000	48	^{t}CK (AVG)	Reserved								ns	
6400C	20.000	17.500	64	^{t}CK (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	18.750	16.250	60	^{t}CK (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	Reserved		ns	
6400AN	16.250	14.375	52	^{t}CK (AVG)	0.312	<0.333	Reserved						ns	
Supported CL					22,26,30,32,34,36,38,40,42,44,46,48,50,52,56,60,64		22,30,32,34,36,38,40,42,44,46,48,50,52,54,56,60,64		22,30,32,34,36,40,42,46,48,52,56,60,64		22,32,36,40,44,48,52,56,60,64		*n*CK	

Notes: 1. Minimum timing parameters are defined according to the rules in the Rounding Definitions and Algorithms section.
2. The translation of all timing parameters from ns values to *n*CK values must follow the Rounding Algorithm. The translation of ^{t}AA to CL follows the explicit combinations listed in the Speed Bin Tables.
3. The CL setting and CWL setting result in ^{t}CK(avg) MIN and ^{t}CK(avg) MAX requirements. When selecting ^{t}CK(avg), requirements from the CL setting, as well as requirements from the CWL setting, must be fulfilled.
4. Reserved settings are not allowed. User must program a different value.

5. This column shows the intended native speed bin timings to be replaced and supported when down clocking. This column does not necessarily show the actual minimum speed bin timings allowed and supported when down clocking because the timings could be faster according to the Rounding Algorithm and depending on the specific speed bin and down clock frequency combination.
6. 3DS DDR5-3200 AC timing applies if the device operates slower than the 2933 MT/s data rate. This is not limited to only the Speed Bin Table timings.
7. Parameters apply from ^{t}CK,AVG (MIN) to ^{t}CK,AVG (MAX) at all standard JEDEC clock period values, as stated in the Speed Bin Tables.
8. ^{t}RC(min) is always greater than or equal to ^{t}RAS(min) + ^{t}RP(min), and when using the appropriate rounding algorithms, nRC(min) is always greater than or equal to nRAS(min) + nRP(min).
9. ^{t}CK(avg) MAX of 1.010ns (1980 MT/s data rate) is defined to allow for 1% SSC down-spreading at a data rate of 2000 MT/s according to JESD404-1.
10. Each speed bin lists the timing requirements that must be supported in order for a given device to be JEDEC-compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.
11. Any speed bin also supports functional operation at slower frequencies as shown in the table, which are not subject to production tests but are verified by design/characterization.
12. The CL Algorithm can be used to mathematically determine the valid CAS Latencies listed in the speed bin tables. The CL algorithm calculates supported CAS latencies by rounding the operating frequency up to the next fastest native speed bin (i.e., 3200 MT/s, 3600 MT/s...). Using the resulting ^{t}CK(avg) MIN and the bin target timings, the CL algorithm then uses the Rounding Algorithm to calculate the valid CAS latency. Because the DDR5 SDRAM specification only supports even CAS latencies, odd CAS latencies are rounded up to the next even CAS latency. The 1980-2100 MT/s data rate always uses CL22. If ^{t}AA (corrected) or ^{t} RCD ^{t}RP (corrected) are violated, the CL algorithm uses a slower combination of ^{t}AA (target) and ^{t}RCD ^{t}RP (target) to return slower valid CAS latencies. The DDR5 SDRAM can support up to four valid CAS latencies, CL(AN), CL(B), CL(BN), and CL(C) for a given frequency. ^{t}AA (corrected) and ^{t}RCD ^{t}RP (corrected) are calculated by reducing ^{t}AA(min), ^{t}RCD(min), and ^{t}RP(min) by the Rounding Algorithm correction factor. The proper setting of CL shall be determined by the memory controller, either by using the Speed bin tables or by using the CL Algorithm, or by some other means. Refer to the Rounding Definitions and Algorithm section for more information.

```
// Variables already defined in other areas of the DDR5 SDRAM specification
CorrFact       = 0.30                                          // (%)   Rounding Algorithm correction factor
ScaledCorrFact = 997                                           //       Scaled correction factor (1000*(1-0.30%))
tCKreal        =1011-952, 682-238                              // (ps)  Real application tCK(AVG) (1980-2100MT/s, 2933-8400MT/s)
tAAmin         MONO=14000-17500, 3DS=16000-20000               // (ps)  From Speed Bin Tables and DIMM SPD bytes 30-31
tRCDtRPmin     MONO=14000-17500, 3DS=14000-17500               // (ps)  From Speed Bin Tables and DIMM SPD bytes 32-33 (tRCD=tRP)
tAAcorr        = TRUNC(tAAmin*ScaledCorrFactor/1000)           // (ps)  Corrected tAA(min) per the Rounding Algorithm rules
tRCDtRPcorr    = TRUNC(tRCDtRPmin*ScaledCorrFactor/1000)       // (ps)  Corrected tRCD(min), tRP(min) per the Rounding Algorithm
FUNC[RA(targ)] = TRUNC((targ*ScaledCorrFact/tCKstd+1000)/1000) // (nCK) Use Rounding Algorithm to convert bin target timing to nCK
// Round tCKreal down to the next faster standard frequency (tCK in ps)
IF (TRUNC(2000000/(2000*99%))>=TRUNC(tCKreal)>=TRUNC(2000000/(2000*105%)))             // Check for  1980-2100 nominal data rates
   tCKstd=TRUNC(2000000/2000)                                                          // Assign standard 2000 tCK (ps)
ELSE IF (TRUNC(2000000/(2000+7*(133+1/3)))>=TRUNC(tCKreal)>=TRUNC(2000000/3200))     // Check for  2933-3200 nominal data rates
   tCKstd=TRUNC(2000000/3200)                                                          // Assign standard 3200 tCK (ps)
ELSE
   FOR (DataRateNom=3200; DataRateNom<=8000; DataRateNom=DataRateNom+400)              // Check for >3200-8400 nominal data rates
      IF (TRUNC(2000000/DataRateNom)>TRUNC(tCKreal)>=TRUNC(2000000/(DataRateNom+400)))
         tCKstd=TRUNC(2000000/(DataRateNom+400))                                       // Assign standard 3600-8400 tCK (ps)
      ELSE
         tCKstd=RESERVED                                                             // No valid data rate found

// Timing targets (ps) that have been used to define the Speed Bin Tables
// MONO targets                3DS targets
   BinAN_tAAtarg      = 14000 BinAN_tAAtarg      = 16000         // tAA target for AN bins
   BinB__tAAtarg      = 16000 BinB__tAAtarg      = 18500         // tAA target for AN, B bins
   BinBN_tAAtarg      = 16000 BinBN_tAAtarg      = 18500         // tAA target for AN, B, BN bins
   BinC__tAAtarg      = 17500 BinC__tAAtarg      = 20000         // tAA target for AN, B, BN, C bins
   BinAN_tRCDtRPtarg = 14000 BinAN_tRCDtRPtarg = 14000         // tRCD, tRP target for AN bins
   BinBN_tRCDtRPtarg = 16000 BinBN_tRCDtRPtarg = 16000         // tRCD, tRP target for AN, B, BN bins
   BinC__tRCDtRPtarg = 17500 BinC__tRCDtRPtarg = 17500         // tRCD, tRP target for AN, B, BN, C bins
IF (TRUNC(2000000/3600)>tCKstd)                                // tRCD, tRP target for B bins is frequency dependent
   BinB__tRCDtRPtarg = 16000 BinB__tRCDtRPtarg = 16000         // tRCD, tRP target for AN, B bins data rates faster than 3600
ELSE
   // 16250=(2000000/3200)*EVEN(TRUNC((BinB__tRCDtRPtarg*ScaledCorrFact/(2000000/3200)+1000)/1000))
```

```
   BinB__tRCDtRPtarg = 16250 BinB__tRCDtRPtarg = 16250          // tRCD, tRP target for AN, B bins for data rates 3600 and slower

// CL Algorithm using variables defined above
// Up to four valid CL's can be returned for a specific freq: CL(AN), CL(B), CL(BN), CL(C), depending on tAAmin, tRCDmin, tRPmin
// The B and BN bins return the same CL
// Only even CL's (not odd CL's) are valid per the DDR5 SDRAM specification
// nRCD, nRP are only even at standard native frequencies for the AN, BN bins (can be even or odd at intermediate frequencies)
// nRCD, nRP may be even or odd at standard native frequencies for the B, C bins (can be even or odd at intermediate frequencies)
IF (TRUNC(2000000/2000)=tCKstd)                                 // CL22 is the only valid CL for 1980-2100 data rates
   CL(AN)=22                                                    // Valid even CL for AN bins
   CL(B )=22                                                    // Valid even CL for AN, B, bins
   CL(BN)=22                                                    // Valid even CL for AN, B, BN bins
   CL(C )=22                                                    // Valid even CL for AN, B, BN, C bins
ELSE IF (TRUNC(2000000/3200)>=tCKstd>=TRUNC(2000000/8400))      // Valid CL for 2933-8400 data rates
   IF      ((EVEN(RA(BinAN_tAAtarg))*tCKstd>=tAAcorr)AND(EVEN(RA(BinAN_tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even only
      CL(AN)=EVEN(RA(BinAN_tAAtarg))                            // Valid even CL for AN bins
      CL(B )=EVEN(RA(BinB__tAAtarg))                            // Valid even CL for AN, B bins
      CL(BN)=EVEN(RA(BinBN_tAAtarg))                            // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                            // Valid even CL for AN, B, BN, C bins
   ELSE IF ((EVEN(RA(BinB__tAAtarg))*tCKstd>=tAAcorr)AND(    (RA(BinB__tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even, odd
      CL(AN)=RESERVED                                           // Valid even CL for AN bins
      CL(B )=EVEN(RA(BinB__tAAtarg))                            // Valid even CL for AN, B bins
      CL(BN)=EVEN(RA(BinBN_tAAtarg))                            // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                            // Valid even CL for AN, B, BN, C bins
   ELSE IF ((EVEN(RA(BinBN_tAAtarg))*tCKstd>=tAAcorr)AND(EVEN(RA(BinBN_tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even only
      CL(AN)=RESERVED                                           // Valid even CL for AN bins
      CL(B )=RESERVED                                           // Valid even CL for AN, B bins
      CL(BN)=EVEN(RA(BinBN_tAAtarg))                            // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                            // Valid even CL for AN, B, BN, C bins
   ELSE IF ((EVEN(RA(BinC__tAAtarg))*tCKstd>=tAAcorr)AND(    (RA(BinC__tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even, odd
      CL(AN)=RESERVED                                           // Valid even CL for AN bins
      CL(B )=RESERVED                                           // Valid even CL for AN, B bins
      CL(BN)=RESERVED                                           // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                            // Valid even CL for AN, B, BN, C bins
   ELSE                                                         // No valid CL found (tAAmin, tRCDmin, tRPmin are too slow)
      CL(AN)=RESERVED                                           // Valid even CL for AN bins
      CL(B )=RESERVED                                           // Valid even CL for AN, B bins
      CL(BN)=RESERVED                                           // Valid even CL for AN, B, BN bins
      CL(C )=RESERVED                                           // Valid even CL for AN, B, BN, C bins
ELSE                                                            // No valid data rate found
   CL(AN)=RESERVED                                              // Valid even CL for AN bins
   CL(B )=RESERVED                                              // Valid even CL for AN, B bins
   CL(BN)=RESERVED                                              // Valid even CL for AN, B, BN bins
   CL(C )=RESERVED                                              // Valid even CL for AN, B, BN, C bins
```

Table 382: DDR5-6800 Speed Bins and Operating Conditions

Speed Bin				DDR5-6800AN		DDR5-6800B		DDR5-6800BN		DDR5-6800C		Unit	Notes
CL-*n*RCD-*n*RP				TBD		TBD		TBD		TBD			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data			^{t}AA	TBD	–	TBD	–	TBD	–	TBD	–	ns	12
Activate-to-internal read or write delay time			^{t}RCD	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
Row precharge time			^{t}RP	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	TBD	–	TBD	–	TBD	–	TBD	–	ns	7,8
CAS WRITE latency			CWL	CL - 2								*n*CK	
Speed Bin[5]	**^{t}AAmin (ns)[5]**	**^{t}RCDmin ^{t}RPmin (ns)[5]**	**READ CL[12]**	**Supported Frequency Down Bins**									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
				^{t}CK (AVG)									ns	6,9
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
Supported CL													*n*CK	

Table 383: DDR5-7200 Speed Bins and Operating Conditions

Speed Bin				DDR5-7200AN		DDR5-7200B		DDR5-7200BN		DDR5-7200C		Unit	Notes
CL-*n*RCD-*n*RP				TBD		TBD		TBD		TBD			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data			^{t}AA	TBD	–	TBD	–	TBD	–	TBD	–	ns	12
Activate-to-internal read or write delay time			^{t}RCD	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
Row precharge time			^{t}RP	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	TBD	–	TBD	–	TBD	–	TBD	–	ns	7,8
CAS WRITE latency			CWL	CL - 2								*n*CK	
Speed Bin[5]	**^{t}AAmin (ns)[5]**	**^{t}RCDmin ^{t}RPmin (ns)[5]**	**READ CL[12]**	**Supported Frequency Down Bins**									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
				^{t}CK (AVG)									ns	6,9
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
Supported CL													*n*CK	

Table 384: DDR5-7600 Speed Bins and Operating Conditions

Speed Bin				DDR5-7600AN		DDR5-7600B		DDR5-7600BN		DDR5-7600C			
CL-*n*RCD-*n*RP				TBD		TBD		TBD		TBD			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
READ command to first data			^{t}AA	TBD	–	TBD	–	TBD	–	TBD	–	ns	12
Activate-to-internal read or write delay time			^{t}RCD	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
Row precharge time			^{t}RP	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	TBD	–	TBD	–	TBD	–	TBD	–	ns	7,8
CAS WRITE latency			CWL	CL - 2								*n*CK	
Speed Bin[5]	**^{t}AAmin (ns)[5]**	**^{t}RCDmin ^{t}RPmin (ns)[5]**	**READ CL[12]**	**Supported Frequency Down Bins**									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
				^{t}CK (AVG)									ns	6,9
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
Supported CL													*n*CK	

Table 385: DDR5-8000 Speed Bins and Operating Conditions

Speed Bin			DDR5-8000AN		DDR5-8000B		DDR5-8000BN		DDR5-8000C		Unit	Notes
CL-*n*RCD-*n*RP			TBD		TBD		TBD		TBD			
Parameter	Symbol		Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data	^{t}AA		TBD	–	TBD	–	TBD	–	TBD	–	ns	12
Activate-to-internal read or write delay time	^{t}RCD		TBD	–	TBD	–	TBD	–	TBD	–	ns	7
Row precharge time	^{t}RP		TBD	–	TBD	–	TBD	–	TBD	–	ns	7
ACTIVATE-to-PRECHARGE command period	^{t}RAS		TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period	^{t}RC (^{t}RAS + ^{t}RP)		TBD	–	TBD	–	TBD	–	TBD	–	ns	7,8
CAS WRITE latency	CWL		CL - 2								*n*CK	
Speed Bin[5]	**^{t}AAmin (ns)[5]**	**^{t}RCDmin ^{t}RPmin (ns)[5]**	**READ CL[12]**	**Supported Frequency Down Bins**								
				Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
				^{t}CK (AVG)									ns	6,9
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
Supported CL											*n*CK	

Table 386: DDR5-8400 Speed Bins and Operating Conditions

Speed Bin				DDR5-8400AN		DDR5-8400B		DDR5-8400BN		DDR5-8400C		Unit	Notes
CL-*n*RCD-*n*RP				TBD		TBD		TBD		TBD			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data			^{t}AA	TBD	–	TBD	–	TBD	–	TBD	–	ns	12
Activate-to-internal read or write delay time			^{t}RCD	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
Row precharge time			^{t}RP	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	TBD	–	TBD	–	TBD	–	TBD	–	ns	7,8
CAS WRITE latency			CWL	CL - 2								*n*CK	
Speed Bin[5]	**^{t}AAmin (ns)[5]**	**^{t}RCDmin ^{t}RPmin (ns)[5]**	**READ CL[12]**	**Supported Frequency Down Bins**									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
				^{t}CK (AVG)									ns	6,9
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
Supported CL													*n*CK	

Table 387: DDR5-8800 Speed Bins and Operating Conditions

Speed Bin				DDR5-8800AN		DDR5-8800B		DDR5-8800BN		DDR5-8800C		Unit	Notes
CL-*n*RCD-*n*RP				TBD		TBD		TBD		TBD			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data			^{t}AA	TBD	–	TBD	–	TBD	–	TBD	–	ns	12
Activate-to-internal read or write delay time			^{t}RCD	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
Row precharge time			^{t}RP	TBD	–	TBD	–	TBD	–	TBD	–	ns	7
ACTIVATE-to-PRECHARGE command period			^{t}RAS	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	TBD	5×$^{t}REFI$	ns	7
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC (^{t}RAS + ^{t}RP)	TBD	–	TBD	–	TBD	–	TBD	–	ns	7,8
CAS WRITE latency			CWL	CL - 2								*n*CK	
Speed Bin[5]	**^{t}AAmin (ns)[5]**	**^{t}RCDmin ^{t}RPmin (ns)[5]**	**READ CL[12]**	**Supported Frequency Down Bins**									
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
				^{t}CK (AVG)									ns	6,9
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
				^{t}CK (AVG)									ns	
Supported CL													*n*CK	

IDD and IDDQ Parameters and Test Conditions

This section defines IDD, IPP and IDDQ measurement conditions such as test load and patterns. Setup and test load for IDD, IPP and IDDQ measurements are shown in the Measurement Setup and Test Load for IPP, IPP and IDDQ Measurements figure.

The following IDD currents are measured as time-averaged currents with all VDD balls of the device under test tied together. Any IPP or IDDQ current is not included in IDD currents:

IDD0, IDDQ0, IPP0, IDD0F, IDDQ0F, IPP0F, IDD2N, IDDQ2N, IPP2N, IDD2NT, IDDQ2NT, IPP2NT, IDD2P, IDDQ2P, IPP2P, IDD3N, IDDQ3N, IPP3N, IDD3P, IDDQ3P, IPP3P, IDD4R, IDDQ4R, IPP4R, IDD4RC, IDD4W, IDDQ4W, IPP4W, IDD4WC, IDD5F, IDDQ5F, IPP5F, IDD5B, IDDQ5B, IPP5B, IDD5C, IDDQ5C, IPP5C, IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD7, IDDQ7, IPP7, IDD8, IDDQ8, IPP8, IDD9, IDD9Q, IPP9.

IDDQ currents are measured as time-averaged currents with all VDDQ balls of the device under test tied together. Any IDD or IPP current is not included in IDDQ currents.

IPP currents are measured as time-averaged currents with all VPP balls of the device under test tied together. Any IDD or IDDQ current is not included in IPP currents.

Important:IDDQ values cannot be directly used to calculate IO power of the DDR5 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in the Correlation from Simulated Channel IO Power to Actual Channel IO Power Supported by IDDQ Measurement figure.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- 0 and LOW defined as $V_{IN} \leq V_{ILAC,max}$
- 1 and HIGH defined as $V_{IN} \geq V_{IHAC,min}$
- MID-LEVEL is defined as inputs $V_{REF} = 0.75 * V_{DDQ}$
- Timings used for IDD, IPP and IDDQ measurement loop patterns are found in the timing parameter tables
- Basic IDD, IPP and IDDQ measurement conditions are described in the Basic IDD, IPP and IDDQ Measurement Conditions table later in this section
- Detailed IDD, IPP and IDDQ measurement loop patterns are described in the measurement loops tables in the following sections
- IDD measurements are done after properly initializing and training the device. This includes, but is not limited to, setting:
  - TDQS_t disabled in MR5
  - CRC disabled in MR5
  - DM disabled in MR5
  - 1N mode enabled by setting CS assertion duration bit MR2:OP[4]=1b, unless otherwise specified in the IDD, IDDQ, and IPP patterns conditions definitions
- **Important:**The IDD, IPP and IDDQ measurement loop patterns need to be executed at least one time before actual IDD, IPP or IDDQ measurement is started, with the exception of IDD9 which can be measured any time after the device enters MBIST mode.
- T_{CASE} is defined as 0 - 95°C, unless stated in the specific condition definition table below.
- For all IDD, IDDQ, IPP measurement loop timing parameters, refer to the timing parameters defined in the spec to calculate the nCK required.

Figure 234: Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

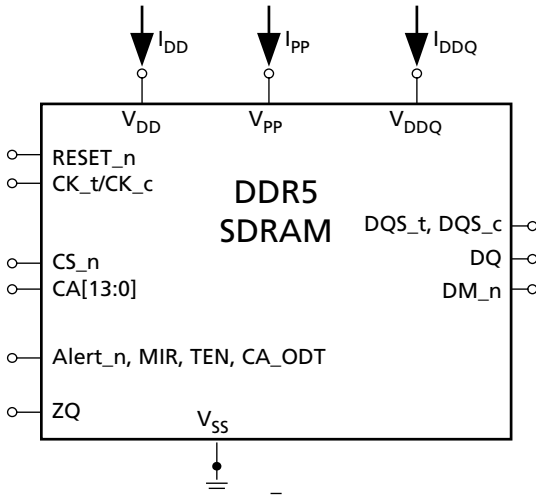


Figure 235: Correlation From Simulated Channel IO Power to Actual Channel IO Power Supported by IDDQ Measurement

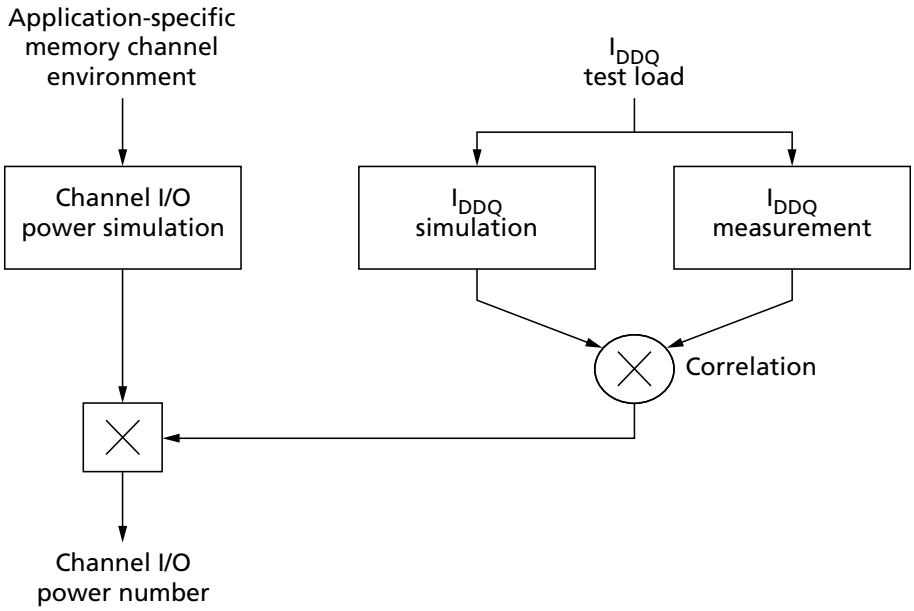


Table 388: Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current** **External clock**: On; tCK, tRC, tRAS, tRP, tRRD CA[13:0]: see Timing Parameter Tables; **BL**: 16[1]; **CS_n**: HIGH between ACT and PRE; **CA Inputs**: Partially toggling according to IDD0, IDD0Q, IPP0 table; **Data IO**: V_{DDQ}; **DM_n**: stable at 1; **Bank Activity**: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see IDD0, IDD0Q, IPP0 table); **Output Buffer and RTT**: Enabled in mode registers[2]; **Pattern Details**: See IDD0, IDD0Q, IPP0 table
IDDQ0	**Operating One Bank Active-Precharge IDDQ Current** Same conditions as IDD0, however measuring IDDQ current instead of IDD current

Table 388: Basic IDD, IPP and IDDQ Measurement Conditions (Continued)

Symbol	Description
IPP0	**Operating One Bank Active-Precharge IPP Current** Same conditions as IDD0, however measuring IPP current instead of IDD current
IDD0F	**Operating Four Bank Active-Precharge Current** **External clock**: On; ^{t}CK, ^{t}RC, ^{t}RAS, ^{t}RP, ^{t}RRD CA[13:0]: see Timing Parameter Tables; **BL:** 16[1]; **CS_n**: HIGH between ACT and PRE; **CA Inputs**: Partially toggling according to the IDD0F, IDDQ0F, IPP0F table; **Data IO**: V_{DDQ};**DM_n**: Stable at 1; **Bank Activity**: Cycling with four banks active at a time: (see the IDD0F, IDDQ0F, IPP0F table); **Output Buffer and RTT**: Enabled in mode registers[2]; **Pattern Details**: See the IDD0F, IDDQ0F, IPP0F table
IDDQ0F	**Operating Four Bank Active-Precharge IDDQ Current** Same conditions with IDD0F, however measuring IDDQ current instead of IDD current
IPP0F	**Operating Four Bank Active-Precharge IPP Current** Same condition with IDD0F, however measuring IPP current instead of IDD current
IDD2N	**Precharge Standby Current** **External clock**: On; ^{t}CK: see Timing Parameter Tables; **CS_n**: stable at 1; **CA Inputs**: Partially toggling according to the IDD2N, IDD3N, IDDQ2N, IDDQ3N, IPP2N, IPP3N table; **Data IO:**V_{DDQ}; **DM_n**: Stable at 1; **Bank Activity**: All banks closed; **Output Buffer and RTT**: Enabled in mode registers[2]; **Pattern Details**: See the IDD2N, IDD3N, IDDQ2N, IDDQ3N, IPP2N, IPP3N table
IDDQ2N	**Precharge Standby IDDQ Current** Same conditions with IDD2N, however measuring IDDQ current instead of IDD current
IPP2N	**Precharge Standby IPP Current** Same conditions with IDD2N, however measuring IPP current instead of IDD current
IDD2NT	**Precharge Standby Non-Target Command Current** **External clock**: On; ^{t}CK; **CS_n**: See Timing Parameter Tables;**BL**: 16[1]; **CS_n**: HIGH between WRITE NT commands; **CS_n, CA Inputs**: Partially toggling according to the IDD2NT, IDDQ2NT, IPP2NT table; **Data IO:** V_{DDQ}; **DM_n**: Stable at 1; **Bank Activity**: All banks closed; **Output Buffer and RTT**: Enabled in mode registers[2]; **Pattern Details**: see the IDD2NT, IDDQ2NT, IPP2NT table
IDDQ2NT (optional)	**Precharge Standby Non-Target Command IDDQ Current** Same conditions with IDD2NT, however measuring IDDQ current instead of IDD current
IPP2NT (optional)	**Precharge Standby Non-Target Command IPP Current** Same conditions with IDD2NT, however measuring IPP current instead of IDD current
IDD2P	**Precharge Power-Down Current** **Device in Precharge Power-Down with ODT control disabled during Power-Down, External clock**: On; ^{t}CK see Timing Parameter Tables; **CS_n**: Stable at 1 after POWER DOWN ENTRY (PDE) command; **CA Inputs**: CA11=HIGH during PDE command; **Data IO**: V_{DDQ}; **DM_n**: Stable at 1; **Bank Activity**: All banks closed; **Output Buffer and RTT**: Enabled in mode registers[2]; **Pattern Details**: see the IDD2N, IDD3N, IDDQ2N, IDDQ3N, IPP2N, IPP3N table
IDDQ2P	**Precharge Power-Down IDDQ Current** Same conditions with IDD2P, however measuring IDDQ current instead of IDD current
IPP2P	**Precharge Power-Down IPP Current** Same conditions with IDD2P, however measuring IPP current instead of IDD current
IDD3N	**Active Standby Current** **External clock**: On; ^{t}CK: see Timing Parameter Tables; **CS_n**: Stable at 1; **CA Inputs**: Partially toggling according to the IDD2N, IDD3N, IDDQ2N, IDDQ3N, IPP2N, IPP3N table; **Data IO**: V_{DDQ}; **DM_n**: Stable at 1; **Bank Activity**: All banks open;**Output Buffer and RTT**: Enabled in mode registers[2]; **Pattern Details**: See the IDD2N, IDD3N, IDDQ2N, IDDQ3N, IPP2N, IPP3N table

Table 388: Basic IDD, IPP and IDDQ Measurement Conditions (Continued)

Symbol	Description
IDDQ3N	**Active Standby IDDQ Current** Same conditions with IDD3N, however measuring IDDQ current instead of IDD current
IPP3N	**Active Standby IPP Current** Same conditions with IDD3N, however measuring IPP current instead of IDD current
IDD3P	**Active Power-Down Current** **Device in Active Power-Down with ODT control disabled during Power-Down, External clock**: On; ^{t}CK: see Timing Parameter Tables; **CS_n**: Stable at 1 after POWER DOWN ENTRY (PDE) command; **CA Inputs**: Stable at 1, CA11=HIGH during PDE command; **Data IO**: V_{DDQ}; **DM_n**: Stable at 1; **Bank Activity**: All banks open; **Output Buffer and RTT**: Enabled in mode registers[2]
IDDQ3P	**Active Power-Down IDDQ Current** Same conditions with IDD3P, however measuring IDDQ current instead of IDD current
IPP3P	**Active Power-Down IPP Current** Same conditions with IDD3P, however measuring IPP current instead of IDD current
IDD4R	**Operating Burst Read Current** External Clock: On; ^{t}CK, ^{t}CCD, CL: see Timing Parameter Tables; **BL**: 16[1]; **CS_n**: HIGH between RD; **CA Inputs**: Partially toggling according to the IDD4R, IDDQ4R, IPP4R table;**Data IO**: Seamless read data burst with different data between one burst and the next one according to the IDD4R, IDDQ4R, IPP4R table; **DM_n**: Stable at 1; **Bank Activity**: All banks open, RD commands cycling through banks (see the IDD4R, IDDQ4R, IPP4R table); **Output Buffer and RTT**: Enabled in mode registers[2]; **Pattern Details**: See the IDD4R, IDDQ4R, IPP4R table
IDD4RC	**Operating Burst Read Current with Read CRC** Read CRC enabled[4],**Other conditions**: See IDD4R
IDDQ4R	**Operating Burst Read IDDQ Current** Same conditions with IDD4R, however measuring IDDQ current instead of IDD current
IPP4R	**Operating Burst Read IPP Current** Same conditions with IDD4R, however measuring IPP current instead of IDD current
IDD4W	**Operating Burst Write Current** **External clock**: On; ^{t}CK, ^{t}CCD, CL: see Timing Parameter Tables; **BL**: 16[1]; **CS_n**: HIGH between WR; **CA Inputs**: Partially toggling according to the IDD4W, IDDQ4W, IPP4W table; **Data IO**: Seamless write data burst with different data between one burst and the next one according to the IDD4W, IDDQ4W, IPP4W table; **DM_n**: Stable at 1; **Bank Activity**: All banks open, WR commands cycling through banks (see the IDD4W, IDDQ4W, IPP4W table); **Output Buffer and RTT**: Enabled in mode registers[2]; **Pattern Details**: See the IDD4W, IDDQ4W, IPP4W table
IDD4WC	**Operating Burst Write Current with Write CRC** **Write CRC enabled[3], Other conditions**: See IDD4W
IDDQ4W	**Operating Burst Write IDDQ Current** Same conditions with IDD4W, however measuring IDDQ current instead of IDD current
IPP4W	**Operating Burst Write IPP Current** Same conditions with IDD4W, however measuring IPP current instead of IDD current
IDD5B	**Burst Refresh Current (Normal Refresh Mode)** **External clock:** On; ^{t}CK, ^{t}RFC1: see Timing Parameter Tables; **CS_n**: HIGH between REF; **CA Inputs**: Partially toggling according to the IDD5B, IDDQ5B, IPP5B table; **Data IO**: V_{DDQ}; **DM_n**: Stable at 1; **Bank Activity**: REF command every ^{t}RFC1 (see the IDD5B, IDDQ5B, IPP5B table); **Output Buffer and RTT**: Enabled in mode registers[2]; **Pattern Details**: See the IDD5B, IDDQ5B, IPP5B table

Table 388: Basic IDD, IPP and IDDQ Measurement Conditions (Continued)

Symbol	Description
IDDQ5B	**Burst Refresh IDDQ Current (Normal Refresh Mode)** Same conditions with IDD5B, however measuring IDDQ current instead of IDD current
IPP5B	**Burst Refresh IPP Current (Normal Refresh Mode)** Same conditions with IDD5B, however measuring IPP current instead of IDD current
IDD5F	**Burst Refresh Current (Fine Granularity Refresh Mode)** Same conditions with IDD5B, FGR mode enabled in MR4, **^{t}RFC=^{t}RFC2, Bank Activity**: REF command every ^{t}RFC2, **Pattern Details**: See the IDD5B, IDDQ5B, IPP5B table
IDDQ5F	**Burst Refresh IDDQ Current (Fine Granularity Refresh Mode)** Same conditions with IDD5F, however measuring IDDQ current instead of IDD current
IPP5F	**Burst Refresh IPP Current (Fine Granularity Refresh Mode)** Same conditions with IDD5F, however measuring IPP current instead of IDD current
IDD5C	**Burst Refresh Current (Same Bank Refresh Mode)** **External clock**: On; ^{t}CK, ^{t}RFCsb: See Timing Parameter Tables; **BL**: 16[1]; **CS_n**: HIGH between REF; **CA Inputs**: Partially toggling according to the IDD5C, IDDQ5C, IPP5C table ; **Data IO**: V_{DDQ}; **DM_n**: Stable at 1; **Bank Activity**: REF command every ^{t}RFCsb (see the IDD5C, IDDQ5C, IPP5C table); **Output Buffer and RTT**: Enabled in mode registers[2];**FGR mode enabled in MR4**. **Pattern Details**: See the IDD5C, IDDQ5C, IPP5C table.
IDDQ5C	**Burst Refresh IDDQ Current (Same Bank Refresh Mode)** Same conditions with IDD5C, however measuring IDDQ current instead of IDD current
IPP5C	**Burst Refresh IPP Current (Same Bank Refresh Mode)** Same conditions with IDD5C, however measuring IPP current instead of IDD current
IDD6N	**Self Refresh Current: Normal Temperature Range** T_{CASE}: 0-85°C; **External clock**: Off; CK_t and CK_c#: HIGH; **^{t}CK, ^{t}CPDED**: See Timing Parameter Tables; **BL**: 16[1]; **CS_n#**: LOW; **CA Inputs Data IO**: HIGH; **DM_n**: Stable at 1; **Bank Activity**: Self-refresh operation; **Output Buffer and RTT**: All ODT disabled in MR32-MR35; **Pattern Details**: see the IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD6R, IDDQ6R, IPP6R table
IDDQ6N	**Self Refresh IDDQ Current: Normal Temperature Range** Same conditions with IDD6N, however measuring IDDQ current instead of IDD current
IPP6N	**Self Refresh IPP Current: Normal Temperature Range** Same conditions with IDD6N, however measuring IPP current instead of IDD current
IDD6E	**Self Refresh Current: Extended Temperature Range** T_{CASE}: 85°C-95°C; **External clock**: Off; CK_t and CK_c#: HIGH; ^{t}CK, ^{t}CPDED: see Timing Parameter Tables; **BL**: 16[1]; **CS_n#**: LOW; **CA Inputs, Data IO**: HIGH; **DM_n**: Stable at 1; **Bank Activity**: Self refresh operation; **Output Buffer and RTT**: Enabled in mode registers[2]; **Pattern Details**: see the IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD6R, IDDQ6R, IPP6R table
IDDQ6E	**Self Refresh IDDQ Current: Extended Temperature Range** Same conditions with IDD6E, however measuring IDDQ current instead of IDD current
IPP6E	**Self Refresh IPP Current: Extended Temperature Range** Same conditions with IDD6E, however measuring IPP current instead of IDD current

Table 388: Basic IDD, IPP and IDDQ Measurement Conditions (Continued)

Symbol	Description
IDD7	**Operating Bank Interleave Read Current** **External clock**: On; tCK, tRC, tRAS, tRCD, tRRD_s, tFAW, tCCD_S, **CL**: see Timing Parameter Tables; **BL**: 16[1]; **CS_n**: HIGH between ACT and RDA; **CA Inputs**: Partially toggling according to the IDD7, IDDQ7, IPP7 table; **Data IO**: Read data bursts with different data between one burst and the next one according to the IDD7, IDDQ7, IPP7 table; **DM_n**: Stable at 1; **Bank Activity**: Two times interleaved cycling through bank groups (0, 1, ...7) with different addressing, see the IDD7, IDDQ7, IPP7 table; **Output Buffer and RTT**: Enabled in mode registers[2]; **Pattern Details**: See the IDD7, IDDQ7, IPP7 table
IDDQ7	**Operating Bank Interleave Read IDDQ Current** Same conditions with IDD7, however measuring IDDQ current instead of IDD current
IPP7	**Operating Bank Interleave Read IPP Current** Same conditions with IDD7, however measuring IPP current instead of IDD current
IDD8	**Maximum Power Saving Deep Power Down Current** **External clock**: Off; **CK_t and CK_c#**: HIGH; **tCK, tCPDED**: see Timing Parameter Tables; **BL**: 16[1]; **CS_n**: LOW;CA: High; **DM_n**: Stable at 1; **Bank Activity**: All banks closed and device in MPSM deep power down mode[5]; **Output Buffer and RTT**: Enabled in mode registers[2] ; **Patterns Details**: Same as IDD6N table, but MPSM is enabled in mode register
IDDQ8	**Maximum Power Saving Deep Power Down IDDQ Current** Same conditions with IDD8 however measuring IDDQ current instead of IDD current
IPP8	**Maximum Power Down IPP Current** Same conditions with IDD8 however measuring IDDQ current instead of IDD current
IDD9 (optional)	**MBIST Current** Device in MBIST mode; **External clock**: On; **CS_n**: Stable at 1 after MBIST entry; **CA Inputs**: Stable at 1; **Data IO**: VDDQ; **Bank Activity**: MBIST operation; **Output Buffer and RTT**: Enabled in mode registers[2]
IDDQ9 (optional)	**MBIST IDDQ Current** Same condition with IDD9; however, measuring IDDQ current instead of IDD current
IPP9 (optional)	MBIST IPP Current Same condition with IDD9; however, measuring IPP current instead of IDD current

Notes: 1. Burst Length: BL16 fixed by MR0 OP[1:0]=00b
2. Output buffer enable:
   —Set MR5:OP[0] = 0b: Qoff = output buffer enabled
   —Set MR5:OP[2:1] = 00b: pull-up output driver impedance = RZQ/7
   —Set MR5:OP[7:6] = 00b: pull-down output driver impedance = RZQ/7
3. RTT_Nom enable:
   —Set MR35 OP[5:3] = 110110b: RTT_NOM_WR = RTT_NOM_RD = RZQ/6
4. RTT_WR enable:
   —Set MR34 OP[5:3] = 010b: RTT_WR = RZQ/2
   —CA/CS/CK ODT, DQS_RTT_PARK, and RTT_PARK disable
   —Set MR32 OP[5:0] = 000000b
   —Set MR33 OP[5:0] = 000000b
   —Set MR34 OP[2:0] = 000b
5. WRITE CRC enable: Set MR50 OP[2:1] = 11b
6. Read CRC enable: SEt MR50 OP[0] = 1b
7. MPSM Deep Power Down Mode
   —Set MR2:OP[3] = 1b if PDA Enumerate ID not equal to 15
   —Set MR2:OP[5] = 1b if PDA Enumerate ID equal to 15

IDD and IDDQ ACTIVE and PRECHARGE Measurement Loops

IDD0, IDD0Q, IPP0

Executes ACTIVE and PRECHARGE commands with tightest timing possible while exercising all bank and bank group addresses. Note 2 applies to entire table.

Table 389: IDD0, IDD0Q, IPP0

Subloop	Sequence	Command	CS_n	C/A [13:0]	Row Address [17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Special Instructions
0	0	ACT	L	-	0x00000	0x0	0x00	0x0	
			H						
	1	DES	H	Toggling[1]					Repeat sequence to satisfy ^{t}RAS (MIN), truncate if required
	2	PREpb	L	-		0x0	0x00	0x0	
	3	DES	H	Toggling[1]					Repeat sequence to satisfy ^{t}RP (MIN), truncate if required
	4	ACT	L	-	0x03FFF	0x0	0x00	0x0	
			H						
	5	DES	H	Toggling[1]					Repeat sequence to satisfy ^{t}RAS (MIN), truncate if required
	6	PREpb	L	-		0x0	0x00	0x0	
	7	DES	H	Toggling[1]					Repeat sequence to satisfy ^{t}RP (MIN), truncate if required
1	8-15	Repeat subloop 0, use BG[2:0]=0x1 instead							
2	16-23	Repeat subloop 0, use BG[2:0]=0x2 instead							
3	24-31	Repeat subloop 0, use BG[2:0]=0x3 instead							
4	32-39	Repeat subloop 0, use BG[2:0]=0x4 instead							Skip for x16
5	40-47	Repeat subloop 0, use BG[2:0]=0x5 instead							Skip for x16
6	48-55	Repeat subloop 0, use BG[2:0]=0x6 instead							Skip for x16
7	56-63	Repeat subloop 0, use BG[2:0]=0x7 instead							Skip for x16
8-15	64-127	Repeat subloops 0-7, use BA[1:0]=0x1 instead							
16-23	128-191	Repeat subloops 0-7, use BA[1:0]=0x2 instead							
24-31	192-255	Repeat subloops 0-7, use BA[1:0]=0x3 instead							
...	...	Repeat subloops 0-31 for each 3DS logical rank, if applicable							CID[2:0]=0x1-0x7

Notes: 1. Utilize DESELECTs between commands while toggling all C/A bits per the four-cycle sequence defined in the IDD2N, IDD3N pattern.
2. For 3DS devices, all non-target logical ranks have IDD2N conditions.

IDD0F, IDDQ0F, IPP0F Pattern

Executes four ACTIVE and PRECHARGE commands per ^{t}RC time while exercising all bank, bank group, and CID addresses. Note 2 applies to entire table.

Table 390: IDD0F, IDDQ0F, IPP0F

Sub-loop	Sequence	Command	CS_n	C/A [13:0]	Row Address [17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Special Instructions
0	0	ACT	L		0x00000	0x0	0x00	0x0	
			H						
	1	DES	H	Toggling[1]					Repeat to satisfy ^{t}RRD (MIN) (6 DES to meet 8nCK)
	2	ACT	L		0x00000	0x0	0x01	0x0	
			H						
	3	DES	H	Toggling[1]					Repeat to satisfy ^{t}RRD (MIN) (6 DES to meet 8nCK)
	4	ACT	L		0x00000	0x0	0x02	0x0	
			H						
	5	DES	H	Toggling[1]					Repeat to satisfy ^{t}RRD (MIN) (6 DES to meet 8nCK)
	6	ACT	L		0x00000	0x0	0x03	0x0	
			H						
	7	DES	H	Toggling[1]					Repeat to satisfy ^{t}RAS(MIN) from sequence 0
	8	PREpb	L			0x0	0x00	0x0	
	9	DES	H	Toggling[1]					Repeat for ^{t}RRD (MIN) (7 DES to meet 8nCK); This allows for next PRE to meet ^{t}RAS (MIN)
	10	PREpb	L			0x0	0x01	0x0	
	11	DES	H	Toggling[1]					Repeat for ^{t}RRD (MIN) (7 DES to meet 8nCK); This allows for next PRE to meet ^{t}RAS (MIN)
	12	PREpb	L			0x0	0x02	0x0	
	13	DES	H	Toggling[1]					Repeat for ^{t}RRD (MIN) (7 DES to meet 8nCK); This allows for next PRE to meet ^{t}RAS (MIN)
	14	PREpb	L			0x0	0x03	0x0	

Table 390: IDD0F, IDDQ0F, IPP0F (Continued)

Sub-loop	Sequ-ence	Comm-and	CS_n	C/A [13:0]	Row Address [17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Special Instructions
0 (cont)	15	DES	H	Toggling[1]					Repeat for ^{t}RRD (MIN) (7 DES to meet 8nCK); This allows for next PRE to meet ^{t}RAS (MIN)
	16	DES	H	Toggling[1]					Repeat for ^{t}RC (MIN) from sequence 0 first ACTIVATE. This will be zero DESELECTS for 4000 MT/s and slower.
1	17-33	Repeat subloop 0, use row address = 0x03FFF for the ACT instead							
2-3	34-67	Repeat subloop 0-1, use BG[2:0]=0x4,0x5,0x6,0x7 instead of 0x0,0x1,0x2,0x3							Skip for x16
4-7	68-101	Repeat subloops 0-3, use BA[1:0]=0x1 instead							
8-11	102-135	Repeat subloops 0-3, use BA[1:0]=0x2 instead							
12-15	136-169	Repeat subloops 0-3, use BA[1:0]=0x3 instead							
...	...	Repeat subloops 0-15 for each 3DS logical rank, if applicable							CID[2:0]=0x1-0x7

Notes: 1. Utilize DESELECTs between commands while toggling all C/A bits per the four-cycle sequence defined in the IDD2N, IDD3N pattern.
2. For 3DS devices, all non-target logical ranks have IDD2N conditions.

IDD2N, IDD3N, IDDQ2N, IDDQ3N, IPP2N, IPP3N

Executes DESELECT commands while exercising all command/address pins in a predefined pattern. All notes apply to entire table.

Table 391: IDD2N, IDD3N, IDDQ2N, IDDQ3N, IPP2N, IPP3N

Sequence	Command	CS	C/A [13:0]
0	DES	H	0x0000
1	DES	H	0x3FFF
2	DES	H	0x3FFF
3	DES	H	0x3FFF

Notes: 1. Data is pulled to V_{DDQ}.
2. DQS_t and DQS_c are pulled to V_{DDQ}.
3. Command/address ODT is disabled.
4. Repeat sequences 0-3.
5. For 3DS devices, all logical ranks have these test conditions.

IDD2NT, IDDQ2NT, IPP2NT

Executes non-target WRITE commands simulating rank-to-rank timing while exercising all C/A bits. Notes 3-6 apply to entire table.

Table 392: IDD2NT, IDDQ2NT, IPP2NT

Sequence	Command	CS _n	C/A [13:0]	Special Instructions
0	WRITE[1]	L	0x002D	All valid C/A inputs to VSS
		L	0x0000	
1	DES	H	Toggling[2]	Repeat sequence to meet 1*^{t}CCD_S (MIN), truncate if required
2	WRITE[1]	L	0x3FED	All valid C/A inputs to VDDQ
		L	0x3FFF	
3	DES	H	Toggling[2]	Repeat sequence to meet 1*^{t}CCD_S (MIN), truncate if required

Notes: 1. WRITE with CS_n=L on both cycles indicates a non-target WRITE.
2. Utilize DESELECTs between commands while toggling C/A bits per the four-cycle sequence defined in the IDD2N, IDD3N pattern.
3. Time between non-target WRITEs reflect ^{t}CCD_S (MIN) for one rank.
4. DQ signals are V_{DDQ}.
5. DQS_t, DQS_c are V_{DDQ}.
6. Repeat 0-3.

IDD4R, IDDQ4R, and IPP4R

Executes READ commands with the tightest possible timing while exercising all bank and bank group addresses. Notes 2-10 apply to entire table.

Table 393: IDD4R, IDDQ4R, IPP4R

Subloop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Instructions
0	0	READ	L	-	0x000	0x00	0x0	0x0	Pattern A	All valid inputs = V_{DDQ}
			H							
	1	DES	H	Toggling[1]	-					Repeat sequence to satisfy ^{t}CCD_S (MIN), truncate if required
1	2	READ	L	-	0x3F0	0x00	0x1	0x0	Pattern B	All valid inputs = V_{DDQ}
			H							
	3	DES	H	Toggling[1]	-					Repeat sequence to satisfy ^{t}CCD_S (MIN), truncate if required
2	4-5	Repeat subloop 0, use BG[2:0]=0x2 instead								
3	6-7	Repeat subloop 1, use BG[2:0]=0x3 instead								
4	8-9	Repeat subloop 0, use BG[2:0]=0x4 instead								Skip for x16
5	10-11	Repeat subloop 1, use BG[2:0]=0x5 instead								Skip for x16

Table 393: IDD4R, IDDQ4R, IPP4R (Continued)

Subloop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Instructions
6	12-13	Repeat subloop 0, use BG[2:0]=0x6 instead								Skip for x16
7	14-15	Repeat subloop 1, use BG[2:0]=0x7 instead								Skip for x16
8	16	READ	L	-	0x3F0	0x00	0x0	0x0	Pattern B	All valid inputs = V_{DDQ}
			H							
	17	DES	H	Toggling[1]						Repeat sequence to satisfy ^{t}CCD_S (MIN), truncate if required
9	18	READ	L	-	0x000	0x00	0x1	0x0	Pattern A	All valid inputs = V_{DDQ}
			H							
	19	DES	H	Toggling[1]						Repeat sequence to satisfy ^{t}CCD_S (MIN), truncate if required
10	20-21	Repeat subloop 8, use BG[2:0]=0x2 instead								
11	22-23	Repeat subloop 9, use BG[2:0]=0x3 instead								
12	24-25	Repeat subloop 8, use BG[2:0]=0x4 instead								Skip for x16
13	26-27	Repeat subloop 9, use BG[2:0]=0x5 instead								Skip for x16
14	28-29	Repeat subloop 8, use BG[2:0]=0x6 instead								Skip for x16
15	30-31	Repeat subloop 9, use BG[2:0]=0x7 instead								Skip for x16
16-31	32-33	Repeat subloops 0-15, use BA[1:0]=0x1 instead								
32-47	34-35	Repeat subloops 0-15, use BA[1:0]=0x2 instead								
48-63	36-37	Repeat subloops 0-15, use BA[1:0]=0x3 instead								
...	...	Repeat subloops 0-63 for each 3DS logical rank, if applicable								CID[2:0] = 0x1-0x7

Notes:
1. Utilize DESELECTs between commands per the four-cycle sequence defined in the IDD2N, IDD3N pattern.
2. READs performed with auto precharge = HIGH, burst chop = HIGH.
3. Row address is set to 0x0000.
4. Data reflects burst length of 16.
5. Data pattern A for x4: 0x0, 0xF, 0xF, 0x0, 0x0, 0xF, 0x0, 0xF, 0xF, 0x0, 0x0, 0xF, 0x0, 0xF, 0x0, 0xF.
6. Data pattern B for x4: 0xF, 0x0, 0x0, 0xF, 0xF, 0x0, 0xF, 0x0, 0x0, 0xF, 0xF, 0x0, 0xF, 0x0, 0xF, 0x0.
7. Data pattern for x8 each beat will reflect two like nibbles (data pattern A = 0x00, 0xFF, 0xFF...).
8. Data pattern for x16 each beat will reflect two like bytes (data pattern A = 0x0000, 0xFFFF, 0xFFFF...).
9. Where C/A column is not populated, refer to command truth table, column address, BA, BG, and CID for the C/A state.
10. For 3DS devices, all non-target logical ranks have IDD2N conditions.

IDD4W, IDDQ4W, and IPP4W

Executes WRITE commands with the tightest possible timing while exercising all bank and bank group addresses. Notes 2-7 apply to entire table.

Table 394: IDD4W, IDDQ4W, IPP4W

Subloop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Instructions
0	0	WRITE	L	-	0x000	0x00	0x0	0x0	Pattern A	All valid inputs = V_{DDQ}
			H							
	1	DES	H	Toggling[1]	-					Repeat sequence to satisfy ^{t}CCD_S (MIN), truncate if required
1	2	WRITE	L	-	0x3F0	0x00	0x1	0x0	Pattern B	All valid inputs = V_{DDQ}
			H							
	3	DES	H	Toggling[1]	-					Repeat sequence to satisfy ^{t}CCD_S (MIN), truncate if required
2	4-5	Repeat subloop 0, use BG[2:0]=0x2 instead								
3	6-7	Repeat subloop 1, use BG[2:0]=0x3 instead								
4	8-9	Repeat subloop 0, use BG[2:0]=0x4 instead								Skip for x16
5	10-11	Repeat subloop 1, use BG[2:0]=0x5 instead								Skip for x16
6	12-13	Repeat subloop 0, use BG[2:0]=0x6 instead								Skip for x16
7	14-15	Repeat subloop 1, use BG[2:0]=0x7 instead								Skip for x16
8	16	WRITE	L	-	0x3F0	0x00	0x0	0x0	Pattern B	All valid inputs = V_{DDQ}
			H							
	17	DES	H	Toggling[1]						Repeat sequence to satisfy ^{t}CCD_S (MIN), truncate if required
9	18	WRITE	L	-	0x000	0x00	0x1	0x0	Pattern A	All valid inputs = V_{DDQ}
			H							
	19	DES	H	Toggling[1]						Repeat sequence to satisfy ^{t}CCD_S (MIN), truncate if required
10	20-21	Repeat subloop 8, use BG[2:0]=0x2 instead								
11	22-23	Repeat subloop 9, use BG[2:0]=0x3 instead								
12	24-25	Repeat subloop 8, use BG[2:0]=0x4 instead								Skip for x16
13	26-27	Repeat subloop 9, use BG[2:0]=0x5 instead								Skip for x16
14	28-29	Repeat subloop 8, use BG[2:0]=0x6 instead								Skip for x16
15	30-31	Repeat subloop 9, use BG[2:0]=0x7 instead								Skip for x16

Table 394: IDD4W, IDDQ4W, IPP4W (Continued)

Subloop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Instructions
16-31	32-33	Repeat subloops 0-15, use BA[1:0]=0x1 instead								
32-47	34-35	Repeat subloops 0-15, use BA[1:0]=0x2 instead								
48-63	36-37	Repeat subloops 0-15, use BA[1:0]=0x3 instead								
...	...	Repeat subloops 0-63 for each 3DS logical rank, if applicable								CID[2:0] = 0x1-0x7

Notes: 1. Utilize DESELECTs between commands per the four-cycle sequence defined in the IDD2N, IDD3N pattern.
2. WRITEs performed with auto precharge = HIGH, burst chop = HIGH.
3. Row address is set to 0x0000.
4. Data reflects burst length of 16.
5. Refer to IDD4R measurement loop table for data pattern definition.
6. Where C/A column is not populated, refer to command truth table, column address, BA, BG, and CID for the C/A state.
7. For 3DS devices, all non-target logical ranks have IDD2N conditions.

IDD5B, IDDQ5B, IPP5B, IDD5F, IDDQ5F, IPP5F

Executes REFRESH (all banks) commands at minimum ^{t}RFC1. Notes 3-6 apply to entire table.

Table 395: I_{DD5B}, I_{DDQ5B}, I_{PP5B}, I_{DD5F}, I_{DDQ5F}, I_{PP5F}

Sequence	Command	CS_n	C/A[13:0]	CA[9:8]	CID[2:0]	Special Instructions
0	REFab	L	-	H	0x0	All valid inputs = V_{DDQ}
1	DES	H	Toggling[1]	-	-	Repeat sequence to satisfy ^{t}RFC (MIN)[2], truncate if required
2	REFab	L	-	H	0x0	All valid inputs = V_{DDQ}
3	DES	H	Toggling[1]	-	-	Repeat sequence to satisfy ^{t}RFC (MIN)[2], truncate if required
...	Repeat sequence 0-3 for each 3DS logical rank, if applicable					CID[2:0] = 0x1-0x7

Notes: 1. Utilize DESELECTs between commands per the four-cycle sequence defined in the IDD2N, IDD3N pattern.
2. For IDD5B, use ^{t}RFC1 (MIN). For IDD5F, use ^{t}RFC2 (MIN).
3. DQ signals are V_{DDQ}.
4. For 3DS devices, all non-target logical ranks have I_{DD2N} conditions.
5. Where C/A[13:0] column is not populated, refer to command truth table, CA[9:8], and CID columns for the C/A state.
6. Must set CA[9:8]=H on REFab commands to indicate 1X refresh rate on devices that support RIR.

IDD5C, IDDQ5C, IPP5C

Executes REFRESH (same bank) commands at minimum ^{t}RFCsb. All notes apply to entire table.

Table 396: IDD5C, IDDQ5C, IPP5C

Sequence	Command	CS_n	C/A[13:0]	CA[9:8]	BA[1:0]	CID[2:0]	Special Instructions
0	REFsb	L	-	H	0x0	0x0	

Table 396: IDD5C, IDDQ5C, IPP5C (Continued)

Sequence	Command	CS_n	C/A[13:0]	CA[9:8]	BA[1:0]	CID[2:0]	Special Instructions
1	DES	H	Toggling[1]	-	-	-	Repeat sequence to satisfy ^{t}RFCsb (MIN), truncate if required
2	REFsb	L	-	H	0x1	0x0	
3	DES	H	Toggling[1]	-	-	-	Repeat sequence to satisfy ^{t}RFCsb (MIN), truncate if required
4	REFsb	L	-	H	0x2	0x0	
5	DES	H	Toggling[1]	-			Repeat sequence to satisfy ^{t}RFCsb (MIN), truncate if required
6	REFsb	L	-	H	0x3	0x0	
7	DES	H	Toggling[1]	-			Repeat sequence to satisfy ^{t}RFCsb (MIN), truncate if required
...	Repeat sequence 0-7 for each 3DS logical rank, if applicable						CID[2:0] = 0x1-0x7

Notes: 1. Utilize DESELECTs between commands per the four-cycle sequence defined in the IDD2N, IDD3N pattern.
2. DQ signals are V_{DDQ}.
3. For 3DS devices, all non-target logical ranks have I_{DD2N} conditions.
4. Where C/A[13:0] column is not populated, refer to command truth table, CA[9:8], and CID columns for the C/A state.

IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E

All notes apply to entire table.

Table 397: IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E

Sequence	Command	Clock	CS_n	C/A[13:0]	Special Instructions
0	SRE	Valid	L	0x3BF7	Clocks must be valid ^{t}CKLCS (MIN) time
1	DES	Valid	H	0x3FFF	Repeat sequence to satisfy ^{t}CPDED (MIN), truncate if required
2	All C/A=H	Valid	L	0x3FFF	
3	All C/A=H	CK_t=CK_c=H	L	0x3FFF	Repeat sequence indefinitely

Notes: 1. Data is pulled to V_{DDQ}.
2. DQS_t and DQS_c are pulled to V_{DDQ}.
3. For 3DS, all banks of all logical ranks mimic the same test condition.

IDD7, IDDQ7, IPP7

Executes ACTIVATE, READ/A commands with tightest timing possible while exercising all bank and bank group addresses. All notes apply to entire table.

Table 398: IDD7, IDDQ7, IPP7

Subloop	Sequence	Command	CS_n	C/A [13:0]	Row Address [17:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Instructions
0	0	ACT	L	-	0x00000	-	0x0	0x0	0x0	-	
			H								
	1	DES	H	Toggling[1]							Repeat sequence to satisfy ^{t}RRD_S (MIN)
1	2	ACT	L	-	0x03FFF	-	0x0	0x1	0x0	-	
			H								
	3	DES	H	Toggling[1]							Repeat sequence to satisfy ^{t}RRD_S (MIN)
2	4-5	Repeat subloop 0, use BG[2:0]=0x2 instead									
3	6-7	Repeat subloop 1, use BG[2:0]=0x3 instead									
4	8-9	Repeat subloop 0, use BG[2:0]=0x4 instead									Skip for x16
5	10-11	Repeat subloop 1, use BG[2:0]=0x5 instead									Skip for x16
6	12-13	Repeat subloop 0, use BG[2:0]=0x6 instead									Skip for x16
7	14-15	Repeat subloop 1, use BG[2:0]=0x7 instead									Skip for x16
8	16	RDA	L	-	-	0x3F0	0x0	0x0	0x0	Pattern A	
			H								
	17	ACT	L	-	0x00000	-	0x1	0x0	0x0	-	
			H								
	18	DES	H	Toggling[1]							Repeat sequence to satisfy ^{t}CCD_S (MIN)
9	19	RDA	L	-	-	0x000	0x0	0x0	0x0	Pattern B	
			H								
	20	ACT	L	-	0x03FFF	-	0x1	0x1	0x0	-	
			H								
	21	DES	H	Toggling[1]							Repeat sequence to satisfy ^{t}CCD_S (MIN)
10	22-24	Repeat subloop 8, use BG[2:0]=0x2 instead									
11	25-27	Repeat subloop 9, use BG[2:0]=0x3 instead									
12	28-30	Repeat subloop 8, use BG[2:0]=0x4 instead									Skip for x16
13	31-33	Repeat subloop 9, use BG[2:0]=0x5 instead									Skip for x16
14	34-36	Repeat subloop 8, use BG[2:0]=0x6 instead									Skip for x16
15	37-39	Repeat subloop 9, use BG[2:0]=0x7 instead									Skip for x16
16-23	40-64	Repeat subloops 8-15, use BA[1:0]=0x1 for the RDA and BA[1:0]=0x2 for the ACT									

Table 398: IDD7, IDDQ7, IPP7 (Continued)

Subloop	Sequence	Command	CS_n	C/A [13:0]	Row Address [17:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Instructions
24-31	65-89	Repeat subloops 8-15, use BA[1:0]=0x2 for the RDA and BA[1:0]=0x3 for the ACT									
32-39	90-114	Repeat subloops 8-15, use BA[1:0]=0x3 for the RDA and BA[1:0]=0x0 for the ACT									
...	...	Repeat subloops 0-18 for each 3DS logical rank, if applicable									CID[2:0] = 0x1-0x7

Notes: 1. Utilize DESELECTs between commands per the four-cycle sequence defined in the IDD2N, IDD3N pattern.
2. READs performed with auto precharge = LOW, burst chop = HIGH.
3. Data reflects burst length of 16.
4. Refer to IDDR4 measurement loop table for data pattern definition.
5. For 3DS devices, all non-target logical ranks have IDD2N conditions.

IDD Specifications

Table 399: I_{DD6} Specification

Symbol	Temperature Range	Value	Unit	Notes
I_{DD0}	0 –85°C		mA	3, 4
I_{DD06E}	0 –95°C		mA	4, 5

Notes: 1. Some I_{DD} currents are higher for x16 organization due to larger page-size architecture.
2. Maximum values for I_{DD} currents considering worst-case conditions of process, temperature, and voltage.
3. Applicable for MR4:OP[2:0]=001b, 010b.
4. Supplier data sheets include a maximum value for I_{DD6}.
5. Applicable for MR4:OP[2:0]=011b, 100b, 101b.

Input/Output Capacitance

Table 400: Silicon Pad I/O Capacitance for DDR5 3200-6400

Parameter	Symbol	3200/3600/4000		4400/4800		5200/5600		6000/6400		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Input/output capacitance (DQ, DM_n, DQS_t and DQS_c, TDQS_t, TDQS_c)	C_{IO}	0.45	0.9	0.45	0.9	0.45	0.85	TBD	TBD	pF	1,2
Input/output capacitance delta (DQ, DM_n)	C_{DIO}	–0.1	0.1	–0.1	0.1	-0.1	0.1	TBD	TBD	pF	1,2,8
Input/output capacitance delta (DQS_t and DQS_c)	C_{DDQS}	-	0.04	-	0.04		0.04	TBD	TBD	pF	1,2,4
Input capacitance (CK_t and CK_c)	C_{CK}	0.2	0.7	0.2	0.6	0.2	0.55	TBD	TBD	pF	1,2
Input capacitance delta (CK_t and CK_c)	C_{DCK}	-	0.05	-	0.05		0.05	TBD	TBD	pF	1,2,3
Input capacitance (CS_n and CA[13:0] pins only)	C_I	0.2	0.7	0.2	0.6	0.20	0.55	TBD	TBD	pF	1,2,5
Input capacitance delta (CS_n pins only)	C_{DI_CS}	–0.1	0.1	–0.1	0.1	-0.1	0.1	TBD	TBD	pF	1,2,6
Input capacitance delta (CA[13:0] pins only)	C_{DI_CA}	–0.1	0.1	–0.1	0.1	-0.1	0.1	TBD	TBD	pF	1,2,7
Input/output capacitance of ALERT	C_{ALERT}	0.4	1.5	0.4	1.5	0.4	1.5	TBD	TBD	pF	1,2
Input/output capacitance of Loopback (LBDQ, LBDQS)	$C_{Loopback}$	0.3	1.0	0.3	1.0	0.3	1.0	TBD	TBD	pF	1,2
Input capacitance of TEN	C_{TEN}	0.2	2.3	0.2	2.3	0.2	2.3	TBD	TBD	pF	1,2,9
Input capacitance of ZQ	C_{ZQ}	-	5	-	5	-	5	TBD	TBD	pF	1,2,11
Input capacitance of MIR, CAI, CA_ODT pins	C_{STRAP}	-	10	-	10	-	10	TBD	TBD	pF	1,2,10

Notes: 1. This parameter is not subject to production test. This parameter is measured by using vendor-specific measurement methodology.
2. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.
3. Absolute value C_{IO}(CK_t) - C_{IO}(CK_c)
4. Absolute value of C_{IO}(DQS_t) - C_{IO}(DQS_c)
5. C_I applies to CS_n and CA[13:0]
6. $C_{DI\_CS\_n} = C_I(CS\_n) - 0.5 \times (C_I(CLK\_t) + C_ICLK\_c))$
7. $C_{DI\_CA} = C_I(CA) - 0.5$ x $(CI_(CLK\_t) + C_I(CLK\_c))$.
8. $C_{DIO} = C_{IO}(DQ,DM) - Avg(C_{IO}DQ,DM))$

9. TEN pin may be DRAM internally pulled LOW through a weak pull-down resistor to V_{SS}. In this case, C_{TEN} might not be valid and the system should verify TEN signal with vendor-specific information.
10. MIR, CAI, and CA_ODT are strap pins used to configure module or point-to-point use cases depending on power, signal integrity, and termination requirements. No active AC signaling requirements defined for these pins.
11. Maximum external load capacitance on ZQ pin: 25pF. The ZQ functionality/accuracy with the max capacitive load is characterized.

Table 401: Silicon Pad I/O Capacitance for DDR5 6800-8800

Parameter	Symbol	6800/7200		7600/8000		8400/8800		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Input/output capacitance (DQ, DM_n, DQS_t and DQS_c, TDQS_t, TDQS_c)	C_{IO}	TBD	TBD	TBD	TBD	TBD	TBD	pF	1,2
Input/output capacitance delta (DQ, DM_n)	C_{DIO}	TBD	TBD	TBD	TBD	TBD	TBD	pF	1,2,8
Input/output capacitance delta (DQS_t and DQS_c)	C_{DDQS}		TBD	TBD	TBD	TBD	TBD	pF	1,2,4
Input capacitance (CK_t and CK_c)	C_{CK}	TBD	TBD	TBD	TBD	TBD	TBD	pF	1,2
Input capacitance delta (CK_t and CK_c)	C_{DCK}		TBD	TBD	TBD	TBD	TBD	pF	1,2,3
Input capacitance (CS_n and CA[13:0] pins only)	C_I	TBD	TBD	TBD	TBD	TBD	TBD	pF	1,2,5
Input capacitance delta (CS_n pins only)	C_{DI_CS}	TBD	TBD	TBD	TBD	TBD	TBD	pF	1,2,6
Input capacitance delta (CA[13:0] pins only)	C_{DI_CA}	TBD	TBD	TBD	TBD	TBD	TBD	pF	1,2,7
Input/output capacitance of ALERT	C_{ALERT}	TBD	TBD	TBD	TBD	TBD	TBD	pF	1,2
Input/output capacitance of Loopback (LBDQ, LBDQS)	$C_{Loopback}$	TBD	TBD	TBD	TBD	TBD	TBD	pF	1,2
Input capacitance of TEN	C_{TEN}	TBD	TBD	TBD	TBD	TBD	TBD	pF	1,2,9
Input capacitance of ZQ	C_{ZQ}	-	TBD	TBD	TBD	TBD	TBD	pF	1,2,11
Input capacitance of MIR, CAI, CA_ODT pins	C_{STRAP}	-	TBD	TBD	TBD	TBD	TBD	pF	1,2,10

Notes: 1. This parameter is not subject to production test. This parameter is measured by using vendor-specific measurement methodology.
2. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.
3. Absolute value C_{IO}(CK_t) - C_{IO}(CK_c)
4. Absolute value of C_{IO}(DQS_t) - C_{IO}(DQS_c)
5. C_I applies to CS_n and CA[13:0]
6. $C_{DI\_CS\_n} = C_I(CS\_n) - 0.5 \times (C_I(CLK\_t) + C_ICLK\_c))$
7. $C_{DI\_CA} = C_I(CA) - 0.5 \times (CI_(CLK\_t) + C_I(CLK\_c))$.
8. $C_{DIO} = C_{IO}(DQ,DM) - Avg(C_{IO}DQ,DM))$
9. TEN pin may be DRAM internally pulled LOW through a weak pull-down resistor to V_{SS}. In this case, C_{TEN} might not be valid and the system should verify TEN signal with vendor-specific information.

10. MIR, CAI, and CA_ODT are strap pins used to configure module or point-to-point use cases depending on power, signal integrity, and termination requirements. No active AC signaling requirements defined for these pins.
11. Maximum external load capacitance on ZQ pin: 25pF. The ZQ functionality/accuracy with the max capacitive load is characterized.

Table 402: DRAM Package Electrical Specifications (x4/x8) for DDR5 3200-6400

Parameter	Symbol	3200-4800		5200-5600		6000-6400		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Input/output Z_{pkg}	Z_{pkg_DQ}	45	75	TBD	TBD	TBD	TBD	ohms	1,2,4,5,10
Input/output pkg delay	$T_{pkg\_delay\_DQ}$	10	35	TBD	TBD	TBD	TBD	ps	1,3,4,5
DQS_t, DQS_c Z_{pkg}	Z_{pkg_DQS}	45	75	TBD	TBD	TBD	TBD	ohms	1,2,5,10,12
DQS_t, DQS_c pkg delay	$T_{pkg\_delay\_DQS}$	10	35	TBD	TBD	TBD	TBD	ps	1,3,5,10,12
Delta Z_{pkg} DQS_t, DQS_c	DZ_{pkg_DQS}	–	5	-	TBD	-	TBD	ohms	1,2,5,7,10
Delta delay DQS_t, DQS_c	$DT_{pkg\_delay\_DQS}$	–	2	-	TBD	-	TBD	ps	1,3,5,7,10
Input-CTRL pins Z_{pkg}	Z_{pkg_CTRL}	45	75	TBD	TBD	TBD	TBD	ohms	1,2,5,9,10
Input-CTRL pins pkg delay	$T_{pkg\_delay\_CTRL}$	10	35	TBD	TBD	TBD	TBD	ps	1,3,5,9,10
Input-CMD ADD pins Z_{pkg}	Z_{pkg_CA}	45	75	TBD	TBD	TBD	TBD	ohms	1,2,5,8,10
Input-CMD ADD pins pkg delay	$T_{pkg\_delay\_CA}$	10	35	TBD	TBD	TBD	TBD	ps	1,3,5,8,10
CLK_t and CLK_c Z_{pkg}	Z_{pkg_CLK}	45	75	TBD	TBD	TBD	TBD	ohms	1,2,5,10
CLK_t and CLK_c pkg delay	$T_{pkg\_delay\_CLK}$	10	30	TBD	TBD	TBD	TBD	ps	1,3,5,10
Delta Z_{pkg} CLK_t and CLK_c	$DZ_{pkg\_delay\_CLK}$	–	5	-	TBD	-	TBD	ohms	1,2,5,6,10
Delta delay CLK_t and CLK_c	$DT_{pkg\_delay\_CLK}$	–	2	-	TBD	-	TBD	ps	1,3,5,6,10
ALERT Z_{pkg}	Z_{pkg_ALERT}	45	75	TBD	TBD	TBD	TBD	ohms	1,2,5,10
ALERT delay	$T_{pkg\_delay\_ALERT}$	10	60	TBD	TBD	TBD	TBD	ps	1,3,5,10
Loopback Z_{pkg}	$Z_{pkg\_Loopback}$	45	75	TBD	TBD	TBD	TBD	ohms	1,2,5,10,11
Loopback delay	$T_{pkg\_delay\_Loopback}$	10	60	TBD	TBD	TBD	TBD	ps	1,3,5,10,11

Notes: 1. This parameter is not subject to production test.
2. This parameter is measured by using vendor-specific measurement methodology.
3. This parameter is measured by using vendor-specific measurement methodology.
4. Z_{pkg_DQ} and $T_{pkg\_delay\_DQ}$ applies to DQ, DM, TDQS_t, and TDQS_c.
5. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.
6. Absolute value of $Z_{pkg\_CK\_t}$ - $Z_{pkg\_CK\_c}$ for impedance (Z) or absolute value of $T_{pkg\_delay\_CK\_t}$ - $T_{pkg\_delay\_CK\_c}$ for delay (T_{pkg_delay}).
7. Absolute value of $Z_{pkg(DQS\_t)}$ - $Z_{pkg(DQS\_c)}$ for impedance (Z) or absolute value of $T_{pkg\_delay\_DQS\_t}$ - $T_{pkg\_delay\_DQS\_c}$ for delay (T_{pkg_delay})
8. Z_{pkg_CA} and $T_{pkg\_delay\_CA}$ applies to CA[13:0].
9. Z_{pkg_CTRL} and $T_{pkg\_delay\_CTRL}$ applies to CS_n.
10. Package implementations should meet specifications if the designed Z_{pkg} and T_{pkg_delay} fall within the ranges shown.
11. $Z_{pkg\_Loopback}$ and $T_{pkg\_delay\_Loopback}$ applies to LBDQ and LBDQS.
12. Z_{pkg_DQS} and $T_{pkg\_delay\_DQS}$ applies to DQS_C, DQS_T, TDQS_T and TDQS_C.

Table 403: DRAM Package Electrical Specifications (x4/x8) for DDR5 6800-8800

Parameter	Symbol	6800-7200		7600-8000		8400-8800		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Input/output Z_{pkg}	Z_{pkg_DQ}	TBD	TBD	TBD	TBD	TBD	TBD	ohms	1,2,4,5,10
Input/output pkg delay	$T_{pkg\_delay\_DQ}$	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,3,4,5
DQS_t, DQS_c Z_{pkg}	Z_{pkg_DQS}	TBD	TBD	TBD	TBD	TBD	TBD	ohms	1,2,5,10,12
DQS_t, DQS_c pkg delay	$T_{pkg\_delay\_DQS}$	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,3,5,10,12
Delta Z_{pkg} DQS_t, DQS_c	DZ_{pkg_DQS}	–	TBD	-	TBD	-	TBD	ohms	1,2,5,7,10
Delta delay DQS_t, DQS_c	$DT_{pkg\_delay\_DQS}$	–	TBD	-	TBD	-	TBD	ps	1,3,5,7,10
Input-CTRL pins Z_{pkg}	Z_{pkg_CTRL}	TBD	TBD	TBD	TBD	TBD	TBD	ohms	1,2,5,9,10
Input-CTRL pins pkg delay	$T_{pkg\_delay\_CTRL}$	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,3,5,9,10
Input-CMD ADD pins Z_{pkg}	Z_{pkg_CA}	TBD	TBD	TBD	TBD	TBD	TBD	ohms	1,2,5,8,10
Input-CMD ADD pins pkg delay	$T_{pkg\_delay\_CA}$	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,3,5,8,10
CLK_t and CLK_c Z_{pkg}	Z_{pkg_CLK}	TBD	TBD	TBD	TBD	TBD	TBD	ohms	1,2,5,10
CLK_t and CLK_c pkg delay	$T_{pkg\_delay\_CLK}$	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,3,5,10
Delta Z_{pkg} CLK_t and CLK_c	$DZ_{pkg\_delay\_CLK}$	–	TBD	-	TBD	-	TBD	ohms	1,2,5,6,10

Table 403: DRAM Package Electrical Specifications (x4/x8) for DDR5 6800-8800 (Continued)

Parameter	Symbol	6800-7200		7600-8000		8400-8800		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Delta delay CLK_t and CLK_c	$DT_{pkg\_delay\_CLK}$	–	TBD	-	TBD	-	TBD	ps	1,3,5,6,10
ALERT Z_{pkg}	Z_{pkg_ALERT}	TBD	TBD	TBD	TBD	TBD	TBD	ohms	1,2,5,10
ALERT delay	$T_{pkg\_delay\_ALERT}$	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,3,5,10
Loopback Z_{pkg}	$Z_{pkg\_Loopback}$	TBD	TBD	TBD	TBD	TBD	TBD	ohms	1,2,5,10,11
Loopback delay	$T_{pkg\_delay\_Loopback}$	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,3,5,10,11

Notes:
1. This parameter is not subject to production test.
2. This parameter is measured by using vendor-specific measurement methodology.
3. This parameter is measured by using vendor-specific measurement methodology.
4. Z_{pkg_DQ} and $T_{pkg\_delay\_DQ}$ applies to DQ, DM, TDQS_t, and TDQS_c.
5. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.
6. Absolute value of $Z_{pkg\_CK\_t}$ - $Z_{pkg\_CK\_c}$ for impedance (Z) or absolute value of $T_{pkg\_delay\_CK\_t}$ - $T_{pkg\_delay\_CK\_c}$ for delay (T_{pkg_delay}).
7. Absolute value of $Z_{pkg(DQS\_t)}$ - $Z_{pkg(DQS\_c)}$ for impedance (Z) or absolute value of $T_{pkg\_delay\_DQS\_t}$ - $T_{pkg\_delay\_DQS\_c}$ for delay (T_{pkg_delay})
8. Z_{pkg_CA} and $T_{pkg\_delay\_CA}$ applies to CA[13:0].
9. Z_{pkg_CTRL} and $T_{pkg\_delay\_CTRL}$ applies to CS_n.
10. Package implementations should meet specifications if the designed Z_{pkg} and T_{pkg_delay} fall within the ranges shown.
11. $Z_{pkg\_Loopback}$ and $T_{pkg\_delay\_Loopback}$ applies to LBDQ and LBDQS.
12. Z_{pkg_DQS} and $T_{pkg\_delay\_DQS}$ applies to DQS_C, DQS_T, TDQS_T and TDQS_C.

Table 404: DRAM Package Electrical Specifications (x16) for DDR5 3200-6400

Parameter	Symbol	3200-4800		5200-5600		6000-6400		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Input/output Z_{pkg}	Z_{pkg_DQ}	45	75	TBD	TBD	TBD	TBD	ohms	1,2,4,5,10
Input/output pkg delay	$T_{pkg\_delay\_DQ}$	10	40	TBD	TBD	TBD	TBD	ps	1,3,4,5,10
DQS_t, DQS_c Z_{pkg}	Z_{pkg_DQS}	45	75	TBD	TBD	TBD	TBD	ohms	1,2,5,10,12
DQS_t, DQS_c pkg delay	$T_{pkg\_delay\_DQS}$	10	40	TBD	TBD	TBD	TBD	ps	1,3,5,10,12
Delta Z_{pkg} DQS_t, DQS_c	DZ_{pkg_DQS}	–	5	-	TBD	-	TBD	ohms	1,2,5,7,10
Delta delay DQS_t, DQS_c	$DT_{pkg\_delay\_DQS}$	–	2	-	TBD	-	TBD	ps	1,3,5,7,10

Table 404: DRAM Package Electrical Specifications (x16) for DDR5 3200-6400 (Continued)

Parameter	Symbol	3200-4800		5200-5600		6000-6400		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Input-CTRL pins Z_{pkg}	Z_{pkg_CTRL}	45	75	TBD	TBD	TBD	TBD	ohms	1,2,5,9,10
Input-CTRL pins pkg delay	$T_{pkg\_delay\_CTRL}$	10	40	TBD	TBD	TBD	TBD	ps	1,3,5,9,10
Input-CMD ADD pins Z_{pkg}	Z_{pkg_CA}	45	75	TBD	TBD	TBD	TBD	ohms	1,2,5,8,10
Input-CMD ADD pins pkg delay	$T_{pkg\_delay\_CA}$	10	45	TBD	TBD	TBD	TBD	ps	1,3,5,8,10
CLK_t and CLK_c	Z_{pkg_CLK}	45	75	TBD	TBD	TBD	TBD	ohms	1,2,5,10
CLK_t and CLK_c pkg delay	$T_{pkg\_delay\_CLK}$	10	45	TBD	TBD	TBD	TBD	ps	1,3,5,10
Delta Z_{pkg} CLK_t and CLK_c	$DZ_{pkg\_delay\_CLK}$	–	5	-	TBD	-	TBD	ohms	1,2,5,6,10
Delta delay CLK_t and CLK_c	$DT_{pkg\_delay\_CLK}$	–	2	-	TBD	-	TBD	ps	1,3,5,6,10
ALERT Z_{pkg}	Z_{pkg_ALERT}	45	75	TBD	TBD	TBD	TBD	ohms	1,2,5,10
ALERT delay	$T_{pkg\_delay\_ALERT}$	10	60	TBD	TBD	TBD	TBD	ps	1,3,5,10
Loopback Z_{pkg}	$Z_{pkg\_Loopback}$	45	75	TBD	TBD	TBD	TBD	ohms	1,2,5,10,11
Loopback delay	$T_{pkg\_delay\_Loopback}$	10	60	TBD	TBD	TBD	TBD	ps	1,3,5,10,11

Notes:
1. This parameter is not subject to production test.
2. This parameter is measured by using vendor-specific measurement methodology.
3. This parameter is measured by using vendor-specific measurement methodology.
4. Z_{pkg_DQ} and $T_{pkg\_delay\_DQ}$ applies to DQ, DMU, and DMI.
5. This parameter applies to monolithic devices only; Stacked/dual-die devices are not covered here.
6. Absolute value of $Z_{pkg\_CK\_t}$ - $Z_{pkg\_CK\_c}$ for impedance (Z) or absolute value of $T_{pkg\_delay\_CK\_t}$ - $T_{pkg\_delay\_CK\_c}$ for delay (T_{pkg_delay}).
7. Absolute value of $Z_{pkg(DQS\_t)}$ - $Z_{pkg(DQS\_c)}$ for impedance (Z) or absolute value of $T_{pkg\_delay\_DQS\_t}$ - $T_{pkg\_delay\_DQS\_c}$ for delay (T_{pkg_delay})
8. Z_{pkg_CA} and $T_{pkg\_delay\_CA}$ applies to CA[13:0].
9. Z_{pkg_CTRL} and $T_{pkg\_delay\_CTRL}$ apply to CS_n.
10. Package implementations should meet specifications if the designed Z_{pkg} and T_{pkg_delay} fall within the ranges shown.
11. $Z_{pkg\_Loopback}$ and $T_{pkg\_delay\_Loopback}$ applies to LBDQ and LBDQS.

12. Z_{pkg_DQS} and $T_{pkg\_delay\_DQS}$ applies to DQS_C, DQS_T, TDQS_T and TDQS_C.

Table 405: DRAM Package Electrical Specifications (x16) for DDR5 6800-8800

Parameter	Symbol	6800-7200		7600-8000		8400-8800		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Input/output Z_{pkg}	Z_{pkg_DQ}	TBD	TBD	TBD	TBD	TBD	TBD	ohms	1,2,4,5,10
Input/output pkg delay	$T_{pkg\_delay\_DQ}$	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,3,4,5,10
DQS_t, DQS_c Z_{pkg}	Z_{pkg_DQS}	TBD	TBD	TBD	TBD	TBD	TBD	ohms	1,2,5,10,12
DQS_t, DQS_c pkg delay	$T_{pkg\_delay\_DQS}$	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,3,5,10,12
Delta Z_{pkg} DQS_t, DQS_c	DZ_{pkg_DQS}	–	TBD	-	TBD	-	TBD	ohms	1,2,5,7,10
Delta delay DQS_t, DQS_c	$DT_{pkg\_delay\_DQS}$	–	TBD	-	TBD	-	TBD	ps	1,3,5,7,10
Input-CTRL pins Z_{pkg}	Z_{pkg_CTRL}	TBD	TBD	TBD	TBD	TBD	TBD	ohms	1,2,5,9,10
Input-CTRL pins pkg delay	$T_{pkg\_delay\_CTRL}$	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,3,5,9,10
Input-CMD ADD pins Z_{pkg}	Z_{pkg_CA}	TBD	TBD	TBD	TBD	TBD	TBD	ohms	1,2,5,8,10
Input-CMD ADD pins pkg delay	$T_{pkg\_delay\_CA}$	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,3,5,8,10
CLK_t and CLK_c	Z_{pkg_CLK}	TBD	TBD	TBD	TBD	TBD	TBD	ohms	1,2,5,10
CLK_t and CLK_c pkg delay	$T_{pkg\_delay\_CLK}$	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,3,5,10
Delta Z_{pkg} CLK_t and CLK_c	$DZ_{pkg\_delay\_CLK}$	–	TBD	-	TBD	-	TBD	ohms	1,2,5,6,10
Delta delay CLK_t and CLK_c	$DT_{pkg\_delay\_CLK}$	–	TBD	-	TBD	-	TBD	ps	1,3,5,6,10
ALERT Z_{pkg}	Z_{pkg_ALERT}	TBD	TBD	TBD	TBD	TBD	TBD	ohms	1,2,5,10
ALERT delay	$T_{pkg\_delay\_ALERT}$	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,3,5,10
Loopback Z_{pkg}	$Z_{pkg\_Loopback}$	TBD	TBD	TBD	TBD	TBD	TBD	ohms	1,2,5,10,11
Loopback delay	$T_{pkg\_delay\_Loopback}$	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,3,5,10,11

Notes: 1. This parameter is not subject to production test.
2. This parameter is measured by using vendor-specific measurement methodology.
3. This parameter is measured by using vendor-specific measurement methodology.

4. Z_{pkg_DQ} and $T_{pkg\_delay\_DQ}$ applies to DQ, DMU, and DMI.
5. This parameter applies to monolithic devices only; Stacked/dual-die devices are not covered here.
6. Absolute value of $Z_{pkg\_CK\_t}$ - $Z_{pkg\_CK\_c}$ for impedance (Z) or absolute value of $T_{pkg\_delay\_CK\_t}$ - $T_{pkg\_delay\_CK\_c}$ for delay (T_{pkg_delay}).
7. Absolute value of $Z_{pkg(DQS\_t)}$ - $Z_{pkg(DQS\_c)}$ for impedance (Z) or absolute value of $T_{pkg\_delay\_DQS\_t}$ - $T_{pkg\_delay\_DQS\_c}$ for delay (T_{pkg_delay})
8. Z_{pkg_CA} and $T_{pkg\_delay\_CA}$ applies to CA[13:0].
9. Z_{pkg_CTRL} and $T_{pkg\_delay\_CTRL}$ apply to CS_n.
10. Package implementations should meet specifications if the designed Z_{pkg} and T_{pkg_delay} fall within the ranges shown.
11. $Z_{pkg\_Loopback}$ and $T_{pkg\_delay\_Loopback}$ applies to LBDQ and LBDQS.
12. Z_{pkg_DQS} and $T_{pkg\_delay\_DQS}$ applies to DQS_C, DQS_T, TDQS_T and TDQS_C.

ESD Sensitivity Characteristics

Table 406: ESD Sensitivity Characteristics[1]

Parameter	Symbol	MIN	MAX	Units	Notes
Human body model (HBM)	ESD_{HBM}	1000	–	V	2
Charged device model (CDM)	ESC_{CDM}	250	–	V	2

Notes: 1. State-of-the-art ESD control measures must be in place when handling devices.
2. Refer to ESDA/JEDEC Joint Standard JS-001 for measurement procedures.

Electrical Characteristics and AC Timing

Reference Load for AC Timing and Output Slew Rate

The figure below represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

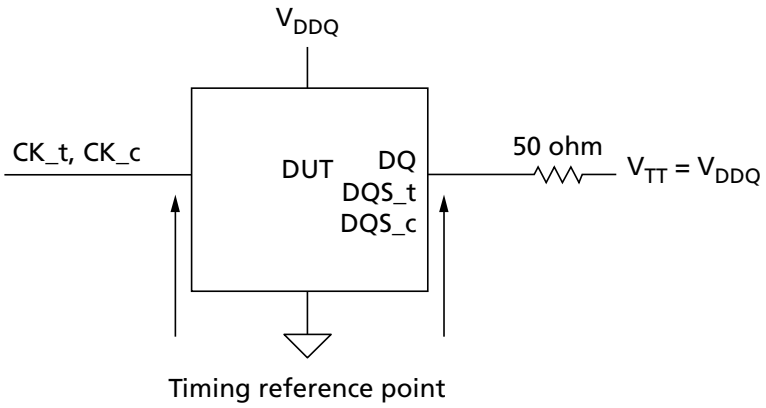
R_{ON} nominal of DQ, DQS_t, and DQS_c drivers uses 34 ohms to specify the relevant AC timing parameter values of the device.

- The maximum DC high level of output signal = $1.0 \times V_{DDQ}$.
- The minimum DC low level of output signal = $\{34/(34 + 50)\} \times V_{DDQ} = 0.4 \times V_{DDQ}$
- The nominal reference level of an output signal can be approximated by the following:
  - The center of maximum DC high and minimum DC low
    $= \{(1 + 0.4)/2\} \times V_{DDQ} = 0.7 \times V_{DDQ}$

The actual reference level of output signal might vary with driver R_{ON} and reference load tolerances. Thus, the actual reference level or midpoint of an output signal is at the widest part of the output signal's eye. Prior to measuring AC parameters, the reference level of the verification tool should be set to an appropriate level.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

Figure 236: Reference Load for AC Timing and Output Slew Rate



Timing Parameters by Speed Grade: Standard

Timing Parameters for DDR5 3200-4000

The analog timing parameters in this section have been defined based on nominal ^{t}CK (AVG) MIN according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

Table 407: DDR5 3200-4000: Clock Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Average clock period	^{t}CK,AVG	0.625		0.555		0.500		ns	23

Table 408: DDR5 3200-4000: Command and Address Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum READ to READ command delay for same bank group, same bank	^{t}CCD_L	max(8*n*CK,5 ns)	-	max(8*n*CK,5 ns)	-	max(8*n*CK,5 ns)	-	*n*CK, ns	
Minimum WRITE to WRITE command delay for same bank group, same bank	^{t}CCD_L_WR	max(32*n*CK, 20ns)	-	max(32*n*CK, 20ns)	-	max(32*n*CK, 20ns)	-	*n*CK, ns	
Minimum WRITE to WRITE command delay for same bank group, second WRITE not RMW	^{t}CCD_L_WR2	max(16*n*CK, 10ns)	-	max(16*n*CK, 10ns)	-	max(16*n*CK, 10ns)	-	*n*CK, ns	
Minimum READ to WRITE command delay for same bank group	^{t}CCD_L_RTW	CL - CWL + RBL/2 + 2 ^{t}CK - (Read DQS offset) + (^{t}RPST - 0.5 ^{t}CK) + ^{t}WPRE						*n*CK, ns	30,31,36
Minimum WRITE to READ command delay for same bank group, same bank	^{t}CCD_L_WTR	CWL + WBL/2 + max(16nCK,10ns)						*n*CK, ns	30,32
READ to READ command delay for different bank group	^{t}CCD_S	8	-	8	-	8	-	*n*CK	
Minimum WRITE to WRITE command delay for different bank group	^{t}CCD_S_WR	8	-	8	-	8	-	*n*CK	
Minimum READ to WRITE command delay for different bank group	^{t}CCD_S_RTW	CL - CWL + RBL/2 + 2 ^{t}CK - (Read DQS offset) + (^{t}RPST - 0.5 ^{t}CK) + ^{t}WPRE						*n*CK, ns	30,31,36
Minimum WRITE to READ command delay for different bank group	^{t}CCD_S_WTR	CWL + WBL/2 + max(4*n*CK,2.5ns)						nCK, ns	30,32
Minimum WRITE to READ with AUTO PRECHARGE command for same bank	^{t}CCD_WTRA	CWL + WBL/2 + ^{t}WR-^{t}RTP						nCK, ns	30,32,35

Table 408: DDR5 3200-4000: Command and Address Timing (Continued)

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ACTIVATE to ACTIVATE command delay to same bank group for 1KB page size	^{t}RRD_L,1K	max(8*n*CK,5 ns)	-	max(8*n*CK,5 ns)	-	max(8*n*CK,5 ns)	-	nCK, ns	
ACTIVATE to ACTIVATE command delay to same bank group for 2KB page size	^{t}RRD_L,2K	max(8*n*CK,5 ns)	-	max(8*n*CK,5 ns)	-	max(8*n*CK,5 ns)	-	nCK, ns	
ACTIVATE to ACTIVATE command delay to different bank group for 1KB page size	^{t}RRD_S,1K	8	-	8	-	8	-	*n*CK	
ACTIVATE to ACTIVATE command delay to different bank group for 2KB page size	^{t}RRD_S,2K	8	-	8	-	8	-	*n*CK	
Four activate window for 2KB page size	^{t}FAW,2K	max(40*n*CK, 25.000ns)	-	max(40*n*CK, 22.222ns)	-	max(40*n*CK, 20.000ns)	-	nCK, ns	
Four activate window for 1KB page size	^{t}FAW,1K	max(32*n*CK, 20.000ns)	-	max(32*n*CK, 17.777ns)	-	max(32*n*CK, 16.000ns)	-	nCK, ns	
READ to PRECHARGE command delay	^{t}RTP	max(12*n*CK, 7.5ns)	-	max(12*n*CK, 7.5ns)	-	max(12*n*CK, 7.5ns)	-		
PRECHARGE to PRECHARGE delay	^{t}PPD	2	-	2	-	2	-	*n*CK	37
WRITE recovery time	^{t}WR	30	-	30	-	30	-	ns	1,23
DLL locking time	^{t}DLLK	1024	-	1024	-	1280	-	*n*CK	

Table 409: DDR5 3200-4000: Mode Register Read/Write Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Mode register READ command period	^{t}MRR	max(14ns, 16*n*CK)	-	max(14ns, 16*n*CK)	-	max(14ns ,16*n*CK)	-		2
Mode register READ patter to mode register READ patter command spacing	^{t}MRR_p	8	-	8	-	8	-	*n*CK	
Mode register WRITE command period	^{t}MRW	max(5ns, 8*n*CK)	-	max(5ns, 8*n*CK)	-	max(5ns, 8*n*CK)	-		2
Mode register SET command delay	^{t}MRD	max(14ns, 16*n*CK)	-	max(14ns, 16*n*CK)	-	max(14ns ,16*n*CK)	-		
DFE mode register WRITE update delay time	^{t}DFE	80	-	80	-	80	-	ns	3

Table 410: DDR5 3200-4000: Data Strobe Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential high toggle pulse width during WRITE preamble	^{t}DQSH_pre	0.395	0.605	0.395	0.605	0.395	0.605	*n*CK	
DQS_t, DQS_c differential low toggle pulse width during WRITE preamble	^{t}DQSL_pre	0.395	0.605	0.395	0.605	TBD	-0.605	*n*CK	
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c	^{t}DQSCK	-0.240	0.240	-0.252	0.252	-0.270	0.270	^{t}CK	7,10,17
DQS_t, DQS_c rising edge output variance window	^{t}DQSCKi	-	0.410	-	0.430	-	0.460	^{t}CK	8,9,10,17,34

Table 411: DDR5 3200-4000: Write Enable Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
2-^{t}CK WRITE preamble enable window	^{t}WPRE_EN_2^{t}CK	1.5	-	1.5	-	1.5	-	^{t}CK	6
3-^{t}CK WRITE preamble enable window	^{t}WPRE_EN_3^{t}CK	2.5	-	2.5	-	2.5	-	^{t}CK	6
4-^{t}CK WRITE preamble enable window	^{t}WPRE_EN_4^{t}CK	2.5	-	2.5	-	2.5	-	^{t}CK	6
Final trained value of host DQS_t-DQS_c timing relative to CWL CK_t-CK_c edge	^{t}DQSoffset	-0.5	0.5	-0.5	0.5	-0.5	0.5	^{t}CK	27
Write leveling setup time	^{t}WLS	-80	80	-80	80	-80	80	ps	
Write leveling hold time	^{t}WLH	-80	80	-80	80	-80	80	ps	
Voltage/temperature drift window of first rising DQS_t preamble edge relative to CWL CK_t-CK_c edge (x4/x8/x16)	^{t}DQSD	-0.25 x ^{t}WPRE_EN_*n* ^{t}CK(min)	0.25 x ^{t}WPRE_EN_*n* ^{t}CK(min)	-0.25 x ^{t}WPRE_EN_*n* ^{t}CK(min)	0.25 x ^{t}WPRE_EN_*n* ^{t}CK(min)	-0.25 x ^{t}WPRE_EN_*n* ^{t}CK(min)	0.25 x ^{t}WPRE_EN_*n* ^{t}CK(min)	^{t}CK	5
Host and system voltage/temperature drift window of first rising DQS_t pre-amble edge relative to CWL CK_t-CK_c edge (x4/x8/x16)	^{t}DQSS	-0.25 x ^{t}WPRE_EN_*n* ^{t}CK(min)	0.25 x ^{t}WPRE_EN_*n* ^{t}CK(min)	-0.25 x ^{t}WPRE_EN_*n* ^{t}CK(min)	0.25 x ^{t}WPRE_EN_*n* ^{t}CK(min)	-0.25 x ^{t}WPRE_EN_*n* ^{t}CK(min)	0.25 x ^{t}WPRE_EN_*n* ^{t}CK(min)	^{t}CK	5,33

Table 412: DDR5 3200-4000: MPSM Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MPSM exit to first valid command delay	^{t}MPSMX	^{t}MRD	-	^{t}MRD	-	^{t}MRD	-	ns	

Table 413: DDR5 3200-4000: ZQ Calibration Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ZQ calibration time	^{t}ZQCAL	1	-	1	-	1	-	µs	
ZQ calibration latch time	^{t}ZQLAT	max(30ns, 8*n*CK)	-	max(30ns, 8*n*CK)	-	max(30ns, 8*n*CK)	-	TBD	

Table 414: DDR5 3200-4000: Reset Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
RESET_n low time for reset initialization with stable power	^{t}PW_RESET	1	-	1	-	1	-	µs	
Time after RESET_n assertion to ODT off	^{t}RST_ADC	-	50	-	50	-	50	ns	

Table 415: DDR5 3200-4000: Self Refresh Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Command pass disable delay	^{t}CPDED	max(5ns, 8*n*CK)	-	max(5ns, 8*n*CK)	-	max(5ns, 8*n*CK)	-	*n*CK, ns	
Self refresh CS_n low pulse width	^{t}CSL	10	-	10	-	10	-	ns	
Self refresh exit CS_n high pulse width	^{t}CSH_SRexit	13	30	13	30	13	30	ns	
Self refresh exit CS_n low pulse width	^{t}CSL_SRexit	3*n*CK	30ns	3*n*CK	30ns	3*n*CK	30ns	*n*CK, ns	12
Self refresh exit CS_n low pulse width with frequency change	^{t}CSL_FreqChg	V_{REFCA_time}	-	V_{REFCA_time}	-	V_{REFCA_time}	-	ns	13
Valid clock requirement before SRE	^{t}CKSRX	max(3.5ns, 8*n*CK)	-	max(3.5ns, 8*n*CK)	-	max(3.5ns, 8*n*CK)	-	*n*CK, ns	
Valid clock requirement after SRE	^{t}CKLCS	^{t}CPDED + 1*n*CK	-	^{t}CPDED + 1*n*CK	-	^{t}CPDED + 1*n*CK	-	*n*CK, ns	
Self refresh exit CS_n HIGH	^{t}CASRX	0	-	0	-	0	-	ns	

Table 415: DDR5 3200-4000: Self Refresh Timing (Continued)

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Exit self refresh to commands not requiring a locked DLL	^{t}XS	^{t}RFC1	-	^{t}RFC1	-	^{t}RFC1	-	ns	
Exit self refresh to commands requiring a locked DLL	^{t}XS_DLL	^{t}DLLK	-	^{t}DLLK	-	^{t}DLLK	-	nCK	

Table 416: DDR5 3200-4000: Power-Down Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Command pass disable delay	^{t}CPDED	max(5ns,8*n*CK)	-	max(5ns,8*n*CK)	-	max(5ns,8*n*CK)	-		
Power-down time	^{t}PD	max(7.5ns,8 *n*CK)	5*^{t}REFI1 (normal) 9*^{t}REFI2 (FGR)	max(7.5ns,8 *n*CK)	5*^{t}REFI1 (normal) 9*^{t}REFI2 (FGR)	max(7.5ns,8 *n*CK)	5*^{t}REFI1 (normal) 9*^{t}REFI2 (FGR)		29
Exit power-down to next valid command	^{t}XP	max(7.5ns,8 *n*CK)	-	max(7.5ns,8 *n*CK)	-	max(7.5ns,8 *n*CK)			
Timing of ACT command to POWER DOWN ENTRY command	^{t}ACTPDEN	2	-	2	-	2	-	*n*CK	14
Timing of PREab, PREsb or PREpb command to POWER DOWN ENTRY command	^{t}PRPDEN	2	-	2	-	2	-	*n*CK	14
Timing of READ or READ w/ AP command to POWER DOWN ENTRY command	^{t}RDPDEN	CL+RBL/2+1	-	CL+RBL/2+1	-	CL+RBL/2+1	-	*n*CK	25
Timing of WRITE command to POWER DOWN ENTRY command	^{t}WRPDEN	CWL+WBL/ 2+(^{t}WR/^{t}CK (avg))+1	-	CWL+WBL/ 2+(^{t}WR/^{t}CK (avg))+1	-	CWL+WBL/ 2+(^{t}WR/^{t}CK (avg))+1	-	*n*CK	15,24
Timing of WRITE w/ AP command to POWER DOWN ENTRY command	^{t}WRAPDEN	CWL+WBL/ 2+^{t}WR+1		CWL+WBL/ 2+^{t}WR+1		CWL+WBL/ 2+^{t}WR+1		*n*CK	16,25
Timing of REFab or REFsb command to POWER DOWN ENTRY command	^{t}REFPDEN	2	-	2	-	2	-	*n*CK	

Table 416: DDR5 3200-4000: Power-Down Timing (Continued)

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Timing of MRR command to POWER DOWN ENTRY command	^{t}MRRPDEN	CL+8+1	-	CL+8+1	-	CL+8+1	-	*n*CK	25
Timing of MRW command to POWER DOWN ENTRY command	^{t}MRWPDEN	^{t}MRD (MIN)	-	^{t}MRD (MIN)	-	^{t}MRD (MIN)	-	*n*CK	
Timing of MPC command to POWER DOWN ENTRY command	^{t}MPCPDEN	^{t}MPC_delay	-	^{t}MPC_delay	-	^{t}MPC_delay	-	*n*CK	25

Table 417: DDR5 3200-4000: MPC Command Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MPC to any other valid command	^{t}MPC_Delay	^{t}MRD	-	^{t}MRD	-	^{t}MRD	-	*n*CK	
Time between stable MPC command and first falling CS edge (setup)	^{t}MC_MPC_Setup	3	-	3	-	3	-	*n*CK	22
Time between first rising CS edge and stable MPC command (hold)	^{t}MC_MPC_Hold	3	-	3	-	3	-	*n*CK	22
Time CS_n is held LOW to register MPC command	^{t}MPC_CS	3.5	8	3.5	8	3.5	8	*n*CK	21

Table 418: DDR5 3200-4000: PDA Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
PDA ENUMERATE ID command to any other command cycle time	^{t}PDA_DELAY	^{t}PDA_DQS_DELAY (MAX) + BL/2 + 19ns	-	^{t}PDA_DQS_DELAY (MAX) + BL/2 + 19ns	-	^{t}PDA_DQS_DELAY (MAX) + BL/2 + 19ns	-	ns	
Delay to rising strobe edge used for sampling DQ during PDA operation	^{t}PDA_DQS_DELAY	5	18	5	18	5	18	ns	4
DQ setup time during PDA operation	^{t}PDA_S	max(3nCK, 1.875ns)	-	max(3nCK, 1.666ns)	-	max(3nCK, 1.500ns)	-	*n*CK	
DQ hold time during PDA operation	^{t}PDA_H	max(3nCK, 1.875ns)	-	max(3nCK, 1.666ns)	-	max(3nCK, 1.500ns)	-	*n*CK	

Table 419: DDR5 3200-4000: Read Training Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of MRW continuous burst mode exit to next valid command delay	^{t}Cont_Exit_Delay	-	^{t}Cont_Exit + ^{t}MRW	-	^{t}Cont_Exit + ^{t}MRW	-	^{t}Cont_Exit + ^{t}MRW	ns	
Registration of MRW continuous burst mode exit to end of training mode	^{t}Cont_Exit	-	CL+BL/2+10 *n*CK	-	CL+BL/2+10 *n*CK	-	CL+BL/2+10 *n*CK	ns	

Table 420: DDR5 3200-4000: Read Preamble Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay from MRW command to DQS driven	^{t}SDOn	-	max(12*n*CK, 20ns)	-	max(12*n*CK, 20ns)	-	max(12*n*CK, 20ns)		
Delay from MRW command to DQS disabled	^{t}SDOff	-	max(12*n*CK, 20ns)	-	max(12*n*CK, 20ns)	-	max(12*n*CK, 20ns)		

Table 421: DDR5 3200-4000: CA Training Mode Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CATM entry command to start of training samples time	^{t}CATM_Entry	20	-	20	-	20	-	ns	
Registration of CATM exit CS_n assertion to end of training mode (when DQ is no longer driven by the device).	^{t}CATM_Exit	-	14	-	14	-	14	ns	
Registration of CATM exit to next valid command delay	^{t}CATM_Exit_Delay	20	-	20	-	20	-	ns	
Time from sample evaluation to output on DQ bus	^{t}CATM_Valid	-	20	-	20	-	20	ns	
Time output is available on DQ bus	^{t}CATM_DQ_Window	2	-	2	-	2	-	*n*CK	28
CS_n assertion duration to exit CATM	^{t}CATM_CS_Exit	2	8	2	8	2	8	*n*CK	

Table 422: DDR5 3200-4000: CS Training Mode Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CSTM entry command to start of training samples time	^{t}CSTM_Entry	20	-	20	-	20	-	ns	
Registration of CSTM exit command to end of training mode	^{t}CSTM_Exit	-	20	-	20	-	20	ns	

Table 422: DDR5 3200-4000: CS Training Mode Timing (Continued)

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CSTM exit to next valid command delay	^{t}CSTM_Exit_Delay	20	-	20	-	20	-	ns	
Time from sample evaluation to output on DQ bus	^{t}CSTM_Valid	-	20	-	20	-	20	ns	
Time output is available on DQ bus	^{t}CSTM_DQ_Window	2	-	2	-	2	-	*n*CK	28
Min time between last CS_n pulse and first pulse of MPC command to exit CSTM	^{t}CSTM_Min_to_MPC_exit	4	-	4	-	4	-	*n*CK	

Table 423: DDR5 3200-4000: Write Leveling Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Write leveling pulse enable: time from write leveling training enable MRW to when internal write leveling pulse logic level is valid	^{t}WLPEN	–	15	–	15	–	15	ns	
Write leveling output delay	^{t}WLO	–	9.5	–	9.5	–	9.5	ns	
Width of write leveling internal pulse	^{t}WL_Pulse_Width	2	-	2	-	2	-	^{t}CK	18
Write leveling write to subsequent command spacing	^{t}WL_Write	max(CWL, last DQS differential toggle) + ^{t}WLO(MAX) + 2*n*CK)	-	max(CWL, last DQS differential toggle) + ^{t}WLO(MAX) + 2*n*CK)	-	max(CWL, last DQS differential toggle) + ^{t}WLO(MAX) + 2*n*CK)	-		

Table 424: DDR5 3200-4000: V_{REFCA}/V_{REFCS} Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
V_{REFCA}/V_{REFCS} command to any other valid command delay	^{t}VREFCA_Delay/ ^{t}VREFCS_Delay	^{t}MRD	-	^{t}MRD	-	^{t}MRD	-	*n*CK	
Time CS_n is held LOW to register V_{REFCA}/V_{REFCS} command	^{t}VREFCA_CS/ ^{t}VREFCS_CS	3.5	8	3.8	8	3.5	8	*n*CK	19,20
MIN time between stable VREFCA command and first falling CS edge (SETUP)	^{t}MC_VREFCA_Setup	3	-	3	-	3	-	*n*CK	11

Table 424: DDR5 3200-4000: V_{REFCA}/V_{REFCS} Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MIN time between first rising CS edge and stable VREFCA command (HOLD)	^{t}MC_VREF-CA_Hold	3	-	3	-	3	-	*n*CK	11
MIN time between stable VREFCS command and first falling CS edge (SETUP)	^{t}MC_VREFCS_-Setup	3	-	3	-	3	-	*n*CK	11
MIN time between first rising CS edge and stable VREFCS command (HOLD)	^{t}MC_VREFCS_Hold	3	-	3	-	3	-	*n*CK	11

Table 425: DDR5 3200-4000: hPPR/sPPR Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
hPPR programming time (x4/x8)	^{t}PGMa	1000	-	1000	-	1000	-	ms	
hPPR programming time (x16)	^{t}PGMb	2000	-	2000	-	2000	-	ms	
sPPR programming time	^{t}PGM_sPPR	CWL+8^{t}CK+^{t}WR		CWL+8^{t}CK+^{t}WR		CWL+8^{t}CK+^{t}WR		^{t}CK	
hPPR/sPPR recognition time	^{t}PGM_Exit	^{t}RP	-	^{t}RP	-	^{t}RP	-	ns	
hPPR program exit and new address setting time	^{t}PGMPST	50	-	50	-	50	-	µs	
sPPR program exit and new address setting time	^{t}PGMP-ST_sPPR	^{t}MRD	-	^{t}MRD	-	^{t}MRD	-	ns	

Table 426: DDR5 3200-4000: DQS Interval Oscillator Readout Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay time from DQS interval oscillator stop to mode register readout in manual mode	^{t}OSCOM	^{t}MPC_Delay	-	^{t}MPC_Delay	-	^{t}MPC_Delay	-	*n*CK	24
Delay time from DQS interval oscillator stop to mode register readout in automatic mode	^{t}OSCOA	^{t}MRD	-	^{t}MRD	-	^{t}MRD	-	*n*CK	24
DQS interval oscillator start gap in automatic stop mode	^{t}OSCS	^{t}MPC_Delay+DQS interval timer run time						*n*CK	24

Table 427: DDR5 3200-4000: ESC Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ECS operation time	^{t}ECSc	max(176*n*CK, 110ns)	-	max(176*n*CK, 110ns)	-	max(176*n*CK, 110ns)	-		

Table 428: DDR5 3200-4000: CRC Error Reporting Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
CRC error to ALERT_n_latency	^{t}CRC_ALERT	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	12	20	12	20	12	20	*n*CK	

Timing Parameters for DDR5 4400-5200

The analog timing parameters in this section have been defined based on nominal ^{t}CK(avg)min according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

Table 429: DDR5 4400-5200: Clock Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Average clock period	^{t}CK,AVG	0.454	–	0.416	–	0.384		ns	23

Table 430: DDR5 4400-5200: Command and Address Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum READ to READ command delay for same bank group	^{t}CCD_L	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	nCK, ns	
Minimum WRITE to WRITE command delay for same bank group	^{t}CCD_L_WR	max(32*n*CK, 20ns)	-	max(32*n*CK, 20ns)	-	max(32*n*CK, 20ns)	-	nCK, ns	
Minimum WRITE to WRITE command delay for same bank group, second WRITE not RMW	^{t}CCD_L_WR2	max(16*n*CK, 10ns)	-	max(16*n*CK, 10ns)	-	max(16*n*CK, 10ns)	-	nCK, ns	
Minimum READ to WRITE command delay for same bank group	^{t}CCD_L_RTW	CL - CWL + RBL/2 + 2 ^{t}CK - (Read DQS offset) + (^{t}RPST - 0.5 ^{t}CK) + ^{t}WPRE						*n*CK, ns	30, 31, 36
Minimum WRITE to READ command delay for same bank group	^{t}CCD_L_WTR	CWL + WBL/2 + max(16*n*CK,10ns)						nCK, ns	30,32

Table 430: DDR5 4400-5200: Command and Address Timing (Continued)

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum READ to READ command delay for different bank group	^{t}CCD_S_	8	-	8	-	8	-	nCK	
Minimum WRITE to WRITE command delay for different bank group	^{t}CCD_S_WR	8	-	8	-	8	-	*n*CK	
Minimum READ to WRITE command delay for different bank group	^{t}CCD_S_RTW	CL - CWL + RBL/2 + 2 ^{t}CK - (Read DQS offset) + (^{t}RPST - 0.5 ^{t}CK) + ^{t}WPR						*n*CK, ns	30, 31, 36
Minimum WRITE to READ command delay for different bank group	^{t}CCD_S_WTR	CWL + WBL/2 + max(4*n*CK,2.5ns)						*n*CK, ns	30,32
Minimum WRITE to READ with AUTO PRECHARGE command for same bank	^{t}CCD_WTRA	CWL + WBL/2 + ^{t}WR-^{t}RTP						*n*CK, ns	30,32, 35
ACTIVATE to ACTIVATE command delay to same bank group for 1KB page size	^{t}RRD_L,1K	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	*n*CK	
ACTIVATE to ACTIVATE command delay to same bank group for 2KB page size	^{t}RRD_L,2K	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	*n*CK, ns	
ACTIVATE to ACTIVATE command delay to different bank group for 1KB page size	^{t}RRD_S,1K	8	-	8	-	8	-	*n*CK	
ACTIVATE to ACTIVATE command delay to different bank group for 2KB page size	^{t}RRD_S,2K	8	-	8	-	8	-	*n*CK	
Four activate window for 1KB page size	^{t}FAW,1K	max(32*n*CK, 14.545ns)	-	max(32*n*CK, 13.333ns)	-	max(32*n*CK, 12.307ns)	-	*n*CK, ns	
Four activate window for 2KB page size	^{t}FAW,2K	max(40*n*CK, 18.181ns)	-	max(40*n*CK, 16.666ns)	-	max(40*n*CK, 15.384ns)	-	*n*CK, ns	
READ command to PRECHARGE command delay	^{t}RTP	max(12*n*CK, 7.5ns)	-	max(12*n*CK, 7.5ns)	-	max(12*n*CK, 7.5ns)	-	*n*CK, ns	
PRECHARGE to PRECHARGE delay	^{t}PPD	2	-	2	-	2	-	*n*CK	37
WRITE recovery time	^{t}WR	30	–	30	-	30	-	ns	
DLL locking time	^{t}DLLK	1280	-	1536	-	1536	-	*n*CK	

Table 431: DDR5 4400-5200: Mode Register Read/Write Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Mode register READ command period	^{t}MRR	max(14ns,16*n*CK)	-	max(14ns,16*n*CK)	-	max(14ns,16*n*CK)	-		2
Mode register READ pattern to mode register READ pattern command spacing	^{t}MRR_p	8	-	8	-	8	-	*n*CK	
Mode register WRITE command period	^{t}MRW	max(5ns, 8*n*CK)	-	max(5ns, 8*n*CK)	-	max(5ns, 8*n*CK)	-		2
Mode register SET command delay	^{t}MRD	max(14ns,16*n*CK)	-	max(14ns,16*n*CK)	-	max(14ns,16*n*CK)	-		
DFE mode register WRITE update delay time	^{t}DFE	80	-	80	-	80	-	ns	3

Table 432: DDR5 4400-5200: Data Strobe Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential high toggle pulse width during WRITE preamble	^{t}DQSH_pre	0.395	0.605	0.430	0.570	0.430	0.570	*n*CK	
DQS_t, DQS_c differential low toggle pulse width during WRITE preamble	^{t}DQSL_pre	0.395	0.605	0.430	0.570	0.430	0.570	*n*CK	
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c	^{t}DQSCK	-0.286	0.286	-0.300	0.300	-0.313	0.313	^{t}CK	7,10,17
DQS_t, DQS_c rising edge output variance window	^{t}DQSCKI	-	0.475	-	0.490	-	0.510	^{t}CK	8,9,10,17,34

Table 433: DDR5 4400-5200: Write Enable Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
2-^{t}CK WRITE preamble enable window	^{t}WPRE_EN_2^{t}CK	1.5	-	1.5	-	1.5	-	^{t}CK	6
3-^{t}CK WRITE preamble enable window	^{t}WPRE_EN_3^{t}CK	2.5	-	2.5	-	2.5	-	^{t}CK	6
4-^{t}CK WRITE preamble enable window	^{t}WPRE_EN_4^{t}CK	2.5	-	2.5	-	2.5	-	^{t}CK	6
Final trained value of host DQS_t-DQS_c timing relative to CWL CK_t-CK_c edge	^{t}DQSoffset	-0.5	0.5	-0.5	0.5	-0.5	0.5	^{t}CK	27
Write leveling setup time	^{t}WLS	-80	80	-80	80	-80	80	ps	

Table 433: DDR5 4400-5200: Write Enable Timing (Continued)

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Write leveling hold time	^{t}WLH	-80	80	-80	80	-80	80	ps	
Voltage/temperature drift window of first rising DQS_t preamble edge relative to CWL CK_t-CK_c edge (x4/x8/x16)	^{t}DQSD	-0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	-0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	-0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	^{t}CK	5
Host and system voltage/temperature drift window of first rising DQS_t preamble edge relative to CWL CK_t-CK_c edge (x4/x8/x16)	^{t}DQSS	-0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	-0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	-0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	^{t}CK	5,33

Table 434: DDR5 4400-5200: MPSM Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MPSM exit to first valid command delay	^{t}MPSMX	^{t}MRD	-	^{t}MRD	-	^{t}MRD	-	ns	

Table 435: DDR5 4400-5200: ZQ Calibration Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ZQ calibration time	^{t}ZQCAL	1		1		1		µs	
ZQ calibration latch time	^{t}ZQLAT	max(30ns, 8*n*CK)		max(30ns, 8*n*CK)		max(30ns, 8*n*CK)			

Table 436: DDR5 4400-5200: Reset Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
RESET_n low time for reset initialization with stable power	^{t}PW_RESET	1	-	1	-	1	-	µs	
Time after RESET_n assertion to ODT off	^{t}RST_ADC	-	50	-	50	-	50	ns	

Table 437: DDR5 4400-5200: Self Refresh Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Command pass disable delay	^{t}CPDED	max(5ns, 8*n*CK)	-	max(5ns,8 *n*CK)	-	max(5ns,8 *n*CK)	-	*n*CK, ns	
Self refresh CS_n low pulse width	^{t}CSL	10	-	10	-	10	-	ns	

Table 437: DDR5 4400-5200: Self Refresh Timing (Continued)

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Self refresh exit CS_n high pulse width	^{t}CSH_SRexit	13	30	13	30	13	30	ns	
Self refresh exit CS_n low pulse width	^{t}CSL_SRexit	3*n*CK	30ns	3*n*CK	30ns	3*n*CK	30ns	*n*CK, ns	12
Self refresh exit CS_n low pulse width with frequency change	^{t}CSL_FreqChg	V_{REFCA_time}	-	V_{REFCA_time}	-	V_{REFCA_time}	-	ns	13
Valid clock requirement before SRX	^{t}CKSRX	max(3.5ns, 8*n*CK)	-	max(3.5ns, 8*n*CK)	-	max(3.5ns, 8*n*CK)	-	*n*CK, ns	
Valid clock requirement after SRE	^{t}CKLCS	^{t}CPDED + 1*n*CK	-	^{t}CPDED + 1*n*CK	-	^{t}CPDED + 1*n*CK	-	*n*CK, ns	
Self refresh exit CS_n HIGH	^{t}CASRX	0	-	0	-	0	-	ns	
Exit self refresh to commands not requiring a locked DLL	^{t}XS	^{t}RFC1	-	^{t}RFC1	-	^{t}RFC1	-	ns	
Exit self refresh to commands requiring a locked DLL	^{t}XS_DLL	^{t}DLLK	-	^{t}DLLK	-	^{t}DLLK	-	*n*CK	

Table 438: DDR5 4400-5200: Power-Down Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Command pass disable delay	^{t}CPDED	max(5ns,8 *n*CK)	-	max(5ns,8 *n*CK)	-	max(5ns,8 *n*CK)	-		
Power-down time	^{t}PD	max(7.5ns, 8*n*CK)	5*^{t}REFI1 (normal) 9*^{t}REFI2 (FGR)	max(7.5ns, 8*n*CK)	5*^{t}REFI1 (normal) 9*^{t}REFI2 (FGR)	max(7.5ns, 8*n*CK)	5*^{t}REFI1 (normal) 9*^{t}REFI2 (FGR)		29
Exit power-down to next valid command	^{t}XP	max(7.5ns, 8*n*CK)	-	max(7.5ns, 8*n*CK)	-	max(7.5ns, 8*n*CK)			
Timing of ACT command to POWER DOWN ENTRY command	^{t}ACTPDEN	2	-	2	-	2	-	*n*CK	14
Timing of PREab, PREsb or PREpb command to POWER DOWN ENTRY command	^{t}PRPDEN	2	-	2	-	2	-	*n*CK	14
Timing of READ or READ w/ AP command to POWER DOWN ENTRY command	^{t}RDPDEN	CL+RBL/ 2+1	-	CL+RBL/ 2+1	-	CL+RBL/ 2+1	-	*n*CK	25

Table 438: DDR5 4400-5200: Power-Down Timing (Continued)

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Timing of WRITE command to POWER DOWN ENTRY command	tWRPDEN	CWL+WBL / 2+(tWR/tCK(avg))+1	-	CWL+WBL / 2+(tWR/tCK(avg))+1	-	CWL+WBL / 2+(tWR/tCK(avg))+1	-	nCK	15,25
Timing of WRITE w/ AP command to POWER DOWN ENTRY command	tWRAPDEN	CWL+WBL / 2+-tWR+1		CWL+WBL / 2+-tWR+1		CWL+WBL / 2+-tWR+1		nCK	16,25
Timing of REFab or REFsb command to POWER DOWN ENTRY command	tREFPDEN	2	-	2	-	2	-	nCK	
Timing of MRR command to POWER DOWN ENTRY command	tMRRPDEN	CL+8+1	-	CL+8+1	-	CL+8+1	-	nCK	25
Timing of MRW command to POWER DOWN ENTRY command	tMRWPDEN	tMRD (MIN)	-	tMRD (MIN)	-	tMRD (MIN)	-	nCK	
Timing of MPC command to POWER DOWN ENTRY command	tMPCPDEN	tMPC_delay	-	tMPC_delay	-	tMPC_delay	-	nCK	26

Table 439: DDR5 4400-5200: MPC Command Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MPC to any other valid command	tMPC_Delay	tMRD	-	tMRD	-	tMRD	-	nCK	
Time between stable MPC command and first falling CS edge (setup)	tMC_MPC_Setup	3	-	3	-	3	-	nCK	22
Time between first rising CS edge and stable MPC command (HOLD)	tMC_MPC_Hold	3	-	3	-	3	-	nCK	22
Time CS_n is held LOW to register MPC command	tMPC_CS	3.5	8	3.5	8	3.5	8	nCK	21

Table 440: DDR5 4400-5200: PDA Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
PDA ENUMERATE ID command to any other command cycle	tPDA_DELAY	tPDA_DQS_DELAY (MAX) + BL/2 + 19ns	-	tPDA_DQS_DELAY (MAX) + BL/2 + 19ns	-	TBD	-	ns	

Table 440: DDR5 4400-5200: PDA Timing (Continued)

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay to rising strobe edge used for sampling DQ during PDA operation	^{t}PDA_DQS_DELAY	5	18	5	18	TBD	TBD	ns	4
DQS setup time during PDA operation	^{t}PDA_S	3	-	3	-	TBD	-	*n*CK	
DQS hold time during PDA operation	^{t}PDA_H	3	-	3	-	TBD	-	*n*CK	

Table 441: DDR5 4400-5200: Read Training Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of MRW continuous burst mode exit to next valid command delay	^{t}Cont_Exit_Delay	-	^{t}Cont_Exit + ^{t}MRW	-	^{t}Cont_Exit + ^{t}MRW	-	^{t}Cont_Exit + ^{t}MRW	ns	
Registration of MRW continuous burst mode exit to end of training mode	^{t}Cont_Exit	-	CL+BL/2+10 *n*CK	-	CL+BL/2+10 *n*CK	-	CL+BL/2+10 *n*CK	ns	

Table 442: DDR5 4400-5200: Read Preamble Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay from MRW command to DQS driven	^{t}SDOn	-	max(12*n*CK, 20ns)	-	max(12*n*CK, 20ns)	-	max(12*n*CK, 20ns)		
Delay from MRW command to DQS disabled	^{t}SDOff	-	max(12*n*CK, 20ns)	-	max(12*n*CK, 20ns)	-	max(12*n*CK, 20ns)		

Table 443: DDR5 4400-5200: CA Training Mode Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CATM entry command to start of training samples time	^{t}CATM_Entry	20	-	20	-	20	-	ns	
Registration of CATM exit CS_n assertion to end of training mode (when DQ is no longer driven by the device).	^{t}CATM_Exit	-	14	-	14	-	14	ns	
Registration of CATM exit to next valid command delay	^{t}CATM_Exit_Delay	20	-	20	-	20	-	ns	
Time from sample evaluation to output on DQ bus	^{t}CATM_Valid	-	20	-	20	-	20	ns	
Time output is available on DQ bus	^{t}CATM_DQ_Window	2	-	2	-	2	-	*n*CK	28
CS_n assertion duration to exit CATM	^{t}CATM_CS_Exit	2	8	2	8	2	8	*n*CK	

Table 444: DDR5 4400-5200: CS Training Mode Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CSTM entry command to start of training samples time	^{t}CSTM_Entry	20	-	20	-	20	-	ns	
Registration of CSTM exit command to end of training mode	^{t}CSTM_Exit	-	20	-	20	-	20	ns	
Registration of CSTM exit to next valid command delay	^{t}CSTM_Exit_Delay	20	-	20	-	20	-	ns	
Time from sample evaluation to output on DQ bus	^{t}CSTM_Valid	-	20	-	20	-	20	ns	
Time output is available on DQ bus	^{t}CSTM_DQ_Window	2	-	2	-	2	-	*n*CK	28
Min time between last CS_n pulse and first pulse of MPC command to exit CSTM	^{t}CSTM_Min_to_MPC_exit	4	-	4	-	4	-	*n*CK	

Table 445: DDR5 4400-5200: Write Leveling Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Write leveling pulse enable: time from write leveling training enable MRW to when internal write leveling pulse logic level is valid	^{t}WLPEN	–	15	–	15	–	15	ns	
Write leveling output delay	^{t}WLO	–	9.5	–	9.5	–	9.5	ns	
Width of write leveling internal pulse	^{t}WL_-Pulse_Width	2	-	2	-	2	-	^{t}CK	18
Write leveling write to subsequent command spacing	^{t}WL_Write	max(CWL, last DQS differential toggle) + ^{t}WLO (MAX) + 2*n*CK	-	max(CWL, last DQS differential toggle) + ^{t}WLO (MAX) + 2*n*CK	-	max(CWL, last DQS differential toggle) + ^{t}WLO (MAX) + 2*n*CK	-		

Table 446: DDR5 4400-5200: V_{REFCA}/V_{REFCS} Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
VREFCA/VREFCS command to any other valid command delay	^{t}VREFCA_Delay/ ^{t}VREFCS_Delay	^{t}MRD	-	^{t}MRD	-	^{t}MRD	-	*n*CK	
Time CS_n is held LOW to register VREFCA/VREFCS command	^{t}VREFCA_CS/ ^{t}VREFCS_CS	3.5	8	3.8	8	3.5	8	*n*CK	19,20

Table 446: DDR5 4400-5200: V_{REFCA}/V_{REFCS} Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MIN time between stable VREFCA command and first falling CS edge (SETUP)	^{t}MC_VREFCA_-Setup	3	-	3	-	3	-	*n*CK	11
MIN time between first rising CS edge and stable VREFCA command (HOLD)	^{t}MC_VREF-CA_Hold	3	-	3	-	3	-	*n*CK	11
MIN time between stable VREFCS command and first falling CS edge (SETUP)	^{t}MC_VREFCS_-Setup	3	-	3	-	3	-	*n*CK	11
MIN time between first rising CS edge and stable VREFCS command (HOLD)	^{t}MC_VREFCS_Hold	3	-	3	-	3	-	*n*CK	11

Table 447: DDR5 4400-5200: hPPR/sPPR Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
hPPR programming time (x4/x8)	^{t}PGMa	1000	-	1000	-	1000	-	ms	
hPPR programming time (x16)	^{t}PGMb	2000	-	2000	-	2000	-	ms	
sPPR programming time	^{t}PGM_sPPR	CWL+8^{t}CK +^{t}WR		CWL+8^{t}CK +^{t}WR		CWL+8^{t}CK +^{t}WR		^{t}CK	
hPPR/sPPR recognition time	^{t}PGM_Exit	^{t}RP	-	^{t}RP	-	^{t}RP	-	ns	
hPPR program exit and new address setting time	^{t}PGMPST	50	-	50	-	50	-	µs	
sPPR program exit and new address setting time	^{t}PGMPST_sPPR	^{t}MRD	-	^{t}MRD	-	^{t}MRD	-	ns	

Table 448: DDR5 4400-5200: DQS Interval Oscillator Readout Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay time from DQS interval oscillator stop to mode register readout in manual mode	^{t}OSCOM	^{t}MP-C_Delay	-	^{t}MP-C_Delay	-	^{t}MP-C_Delay	-	*n*CK	24
Delay time from DQS interval oscillator stop to mode register readout in automatic mode	^{t}OSCOA	^{t}MRD	-	^{t}MRD	-	^{t}MRD	-	*n*CK	24
DQS interval oscillator start gap in automatic stop mode	^{t}OSCS	^{t}MPC_Delay + DQS interval timer runtime						*n*CK	24

Table 449: DDR5 4400-5200: ESC Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ECS operation time	$^{t}ECSc$	max(176*n*CK, 110ns)	-	max(176*n*CK,110ns)	-	max(176*n*CK,110ns)	-		

Table 450: DDR5 4400-5200: CRC Error Reporting Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
CRC error to ALERT n_latency	$^{t}CRC\_ALERT$	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	12	20	12	20	12	20	*n*CK	

Timing Parameters for DDR5 5600-6400

The analog timing parameters in this section have been defined based on nominal $^{t}CK(avg)min$ according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

Table 451: DDR5 5600-6400: Clock Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Average clock period	$^{t}CK,AVG$	0.357		0.333	–	0.312	–	ns	23

Table 452: DDR5 5600-6400: Command and Address Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum READ to READ command delay for same bank group	$^{t}CCD\_L$	max(8*n*CK,5 ns)	-	max(8*n*CK,5 ns)	-	max(8*n*CK,5 ns)	-	*n*CK, ns	
Minimum WRITE to WRITE command delay for same bank group	$^{t}CCD\_L\_WR$	max(32*n*CK, 20ns)	–	max(32*n*CK, 20ns)	–	max(32*n*CK, 20ns)	–	*n*CK, ns	
Minimum WRITE to WRITE command delay for same bank group, second WRITE not RMW	$^{t}CCD\_L\_WR2$	max(16*n*CK, 10ns)	–	max(16*n*CK, 10ns)	–	max(16*n*CK, 10ns)	–	*n*CK	
Minimum READ to WRITE command delay for same bank group	$^{t}CCD\_L\_RTW$	CL - CWL + RBL/2 + 2 ^{t}CK - (Read DQS offset) + ($^{t}RPST$ - 0.5 ^{t}CK) + $^{t}WPRE$						*n*CK, ns	30,31 ,36
Minimum WRITE to READ command for same bank group	$^{t}CCD\_L\_WTR$	CWL + WBL/2 + 16*n*CK,10ns (MAX)						*n*CK, ns	30,32
READ to READ command delay for different bank group	$^{t}CCD\_S$	8	-	8	-	8	-	*n*CK	

Table 452: DDR5 5600-6400: Command and Address Timing (Continued)

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum WRITE to WRITE command delay for different bank group	tCCD_S_WR	8	-	8	-	8	-	*n*CK	
Minimum READ to WRITE command delay for different bank group	tCCD_S_RTW	CL - CWL + RBL/2 + 2 tCK - (Read DQS offset) + (tRPST - 0.5 tCK) + tWPRE						*nCK, ns*CK	30,31 ,36
Minimum WRITE to READ command delay for different bank group	tCCD_S_WTR	CWL + WBL/2 + 4nCK, 2.5ns (MAX)						*nCK, ns*CK	30,32
Minimum WRITE to READ with AUTO PRECHARGE command for same bank	tCCD_WTRA	CWL + WBL/2 + tWR-tRTP						*n*CK, ns	30,32 ,35
ACTIVATE to ACTIVATE command delay to same bank group for 1KB page size	tRRD_L,1K	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	*n*CK, ns	
ACTIVATE to ACTIVATE command delay to same bank group for 2KB page size	tRRD_L,2K	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	*n*CK, ns	
ACTIVATE to ACTIVATE command delay to different bank group for 1KB page size	tRRD_S,1K	8	-	8	-	8	-	*n*CK	
ACTIVATE to ACTIVATE command delay to different bank group for 2KB page size	tRRD_S,2K	8	-	8	-	8	-	*n*CK	
Four activate window for 2KB page size	tFAW,2K	max(40*n*CK, 14.285ns)	-	max(40*n*CK, 13.333ns)	-	max(40*n*CK, 12.500ns)	-	*n*CK, ns	
Four activate window for 1KB page size	tFAW,1K	max(32*n*CK, 11.428ns)	-	max(32*n*CK, 10.666ns)	-	max(32*n*CK, 10.000ns)	-	*n*CK, ns	
READ command to PRECHARGE command delay	tRTP	max(12*n*CK, 7.5ns)	-	max(12*n*CK, 7.5ns)	-	max(12*n*CK, 7.5ns)	-	*n*CK, ns	
PRECHARGE to PRECHARGE delay	tPPD	2	-	2	-	2	-	*n*CK	37
WRITE recovery time	tWR	30	-	30	-	30	-	ns	
DLL locking time	tDLLK	1792	-	1792	-	2048	-	*n*CK	

Table 453: DDR5 5600-6400: Mode Register Read/Write Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Mode register READ command period	tMRR	max(14ns ,16*n*CK)	-	max(14ns, 16*n*CK)	-	max(14ns, 16*n*CK)	-		2
Mode register READ pattern to mode register READ pattern command spacing	tMRR_p	8	-	8	-	8	-	*n*CK	

Table 453: DDR5 5600-6400: Mode Register Read/Write Timing (Continued)

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Mode register WRITE command period	^{t}MRW	5ns,8*n*CK (MAX)	-	5ns,8*n*CK (MAX)	-	5ns,8*n*CK (MAX)	-		2
Mode register SET command delay	^{t}MRD	14ns,16*n* CK (MAX)	-	14ns,16*n*C K (MAX)	-	14ns,16*n*C K (MAX)	-		
DFE mode register WRITE update delay time	^{t}DFE	80	-	80	-	80	-	ns	3

Table 454: DDR5 5600-6400: Data Strobe Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential high toggle pulse width during WRITE preamble	^{t}DQSH_pre	0.430	0.570	0.430	0.570	0.430	0.570	^{t}CK	
DQS_t, DQS_c differential low toggle pulse width during WRITE preamble	^{t}DQSL_pre	0.430	0.570	0.430	0.570	0.430	0.570	^{t}CK	
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c	^{t}DQSCK	-0.325	0.325	-0.337	0.337	-0.348	0.348	^{t}CK	7,10,17
DQS_t, DQS_c rising edge output variance window	^{t}DQSCKI	-	0.530	-	0.549	-	0.567	^{t}CK	8,9,10, 17,34

Table 455: DDR5 5600-6400: Write Enable Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
2-^{t}CK WRITE preamble enable window	^{t}WPRE_EN_2^{t}CK	1.5	-	1.5	-	1.5	-	^{t}CK	6
3-^{t}CK WRITE preamble enable window	^{t}WPRE_EN_3^{t}CK	2.5	-	2.5	-	2.5	-	^{t}CK	6
4-^{t}CK WRITE preamble enable window	^{t}WPRE_EN_4^{t}CK	2.5	-	2.5	-	2.5	-	^{t}CK	6
DQS_t, DQS_c differential WRITE postamble	^{t}WPST	TBD	-	TBD	-	TBD	-	^{t}CK	
Final trained value of host DQS_t-DQS_c timing relative to CWL CK_t-CK_c edge	^{t}DQSoffset	-0.5	0.5	-0.5	0.5	-0.5	0.5	^{t}CK	26
Write leveling setup time	^{t}WLS	-80	80	-80	80	-80	80	ps	
Write leveling hold time	^{t}WLH	-80	80	-80	80	-80	80	ps	

Table 455: DDR5 5600-6400: Write Enable Timing (Continued)

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Voltage/temperature drift window of first rising DQS_t preamble edge relative to CWL CK_t-CK_c edge (x4/x8/x16)	^{t}DQSD	-0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	-0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	-0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	^{t}CK	5,32
Host and system voltage/temperature drift window of first rising DQS_t pre-amble edge relative to CWL CK_t-CK_c edge (x4/x8/x16)	^{t}DQSS	-0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	-0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	-0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	0.25 x ^{t}WPRE_EN_n^{t}CK (MIN)	^{t}CK	5,32

Table 456: DDR5 5600-6400: MPSM Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MPSM exit to first valid command delay	^{t}MPSMX	^{t}MRD	-	^{t}MRD	-	^{t}MRD	-	ns	

Table 457: DDR5 5600-6400: ZQ Calibration Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ZQ calibration time	^{t}ZQCAL	1		1		1		µs	
ZQ calibration latch time	^{t}ZQLAT	max(30ns, 8nCK)		max(30ns, 8nCK)		max(30ns, 8nCK)			

Table 458: DDR5 5600-6400: Reset Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
RESET_n low time for reset initialization with stable power	^{t}PW_RESET	1	-	1	-	1	-	µs	
Time after RESET_n assertion to ODT off	^{t}RST_ADC	-	50	-	50	-	50	ns	

Table 459: DDR5 5600-6400: Self Refresh Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Command pass disable delay	^{t}CPDED	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-	nCK, ns	
Self refresh CS_n low pulse width	^{t}CSL	10	-	10	-	10	-	ns	

Table 459: DDR5 5600-6400: Self Refresh Timing (Continued)

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Self refresh exit CS_n high pulse width	^{t}CSH_SRexit	13	30	13	30	13	30	ns	
Self refresh exit CS_n low pulse width	^{t}CSL_SRexit	3*n*CK	30ns	3*n*CK	30ns	3*n*CK	30ns	*n*CK, ns	12
Self refresh exit CS_n low pulse width with frequency change	^{t}CSL_FreqChg	V_{REFCA_time}	-	V_{REFCA_time}	-	V_{REFCA_time}	-	ns	13
Valid clock requirement before SRX	^{t}CKSRX	max(3.5ns, 8*n*CK)	-	max(3.5ns, 8*n*CK)	-	max(3.5ns,8*n*CK)	-	*n*CK, ns	
Valid clock requirement after SRE	^{t}CKLCS	^{t}CPDED + 1*n*CK	-	^{t}CPDED + 1*n*CK	-	^{t}CPDED + 1*n*CK	-	*n*CK, ns	
Self refresh exit CS_n HIGH	^{t}CASRX	0	-	0	-	0	-	ns	
Exit self refresh to commands not requiring a locked DLL	^{t}XS	^{t}RFC1	-	^{t}RFC1	-	^{t}RFC1	-	*n*CK	
Exit self refresh to commands requiring a locked DLL	^{t}XS_DLL	^{t}DLLK	-	^{t}DLLK	-	^{t}DLLK	-	ns	

Table 460: DDR5 5600-6400: Power-Down Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Command pass disable delay	^{t}CPDED	max(5ns,8*n*CK)	-	max(5ns,8*n*CK)	-	max(5ns,8*n*CK)	-	ns	
Power-down time	^{t}PD	max(7.5ns, 8*n*CK)	5*^{t}REFI1 (normal) 9*^{t}REFI2 (FGR)	max(7.5ns, 8*n*CK)	5*^{t}REFI1 (normal) 9*^{t}REFI2 (FGR)	max(7.5ns, 8*n*CK)	5*^{t}REFI1 (normal) 9*^{t}REFI2 (FGR)	ns	29
Exit power-down to next valid command	^{t}XP	max(7.5ns, 8*n*CK)	-	max(7.5ns, 8*n*CK)	-	max(7.5ns, 8*n*CK)		ns	
Timing of ACT command to POWER-DOWN ENTRY command	^{t}ACTPDEN	2	-	2	-	2	-	*n*CK	14
Timing of PREab, PREsb or PREpb command to POWER-DOWN ENTRY command	^{t}PRPDEN	2	-	2	-	2	-	*n*CK	14
Timing of READ or READ w/ AP command to POWER-DOWN ENTRY command	^{t}RDPDEN	CL+RBL/2+1	-	CL+RBL/2+1	-	CL+RBL/2+1	-	*n*CK	25

Table 460: DDR5 5600-6400: Power-Down Timing (Continued)

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Timing of WRITE command to POWER-DOWN ENTRY command	^{t}WRPDEN	CWL+WBL/2+(^{t}WR/^{t}CK(avg))+1	-	CWL+WBL/2+(^{t}WR/^{t}CK(avg))+1	-	CWL+WBL/2+(^{t}WR/^{t}CK(avg))+1	-	*n*CK	15,25
Timing of WRITE w/ AP command to POWER-DOWN ENTRY command	^{t}WRAPDEN	CWL+WBL/2+^{t}WR+1		CWL+WBL/2+^{t}WR+1		CWL+WBL/2+^{t}WR+1		*n*CK	16,25
Timing of REFab or REFsb command to POWER-DOWN ENTRY command	^{t}REFPDEN	2	-	2	-	2	-	*n*CK	
Timing of MRR command to POWER-DOWN ENTRY command	^{t}MRRPDEN	CL+8+1	-	CL+8+1	-	CL+8+1	-	*n*CK	25
Timing of MRW command to POWER-DOWN ENTRY command	^{t}MRWPDEN	^{t}MRD (MIN)	-	^{t}MRD (MIN)	-	^{t}MRD (MIN)	-	*n*CK	
Timing of MPC command to POWER-DOWN ENTRY command	^{t}MPCPDEN	^{t}MPC_delay	-	^{t}MPC_delay	-	^{t}MPC_delay	-	*n*CK	26

Table 461: DDR5 5600-6400: MPC Command Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MPC to any other valid command	^{t}MPC_Delay	^{t}MRD	-	^{t}MRD	-	^{t}MRD	-	*n*CK	
Time between stable MPC command and first falling CS edge (setup)	^{t}MC_MPC_Setup	3	-	3	-	3	-	*n*CK	22
Time between first rising CS edge and stable MPC command (HOLD)	^{t}MC_MPC_Hold	3	-	3	-	3	-	*n*CK	22
Time CS_n is held LOW to register MPC command	^{t}MPC_CS	3.5	8	3.5	8	3.5	8	*n*CK	21

Table 462: DDR5 5600-6400: PDA Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
PDA ENUMERATE ID command to any other command cycle	^{t}PDA_DELAY	TBD	-	TBD	-	TBD	-	ns	
Delay to rising strobe edge used for sampling DQ during PDA operation	^{t}PDA_DQS_DELAY	TBD	-	TBD	-	TBD	-	ns	4

Table 462: DDR5 5600-6400: PDA Timing (Continued)

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQS setup time during PDA operation	^{t}PDA_S	TBD	-	TBD	-	TBD	-	*n*CK	
DQS hold time during PDA operation	^{t}PDA_H	TBD	-	TBD	-	TBD	-	*n*CK	

Table 463: DDR5 5600-6400: Read Training Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of MRW continuous burst mode exit to next valid command delay	^{t}Cont_Exit_Delay	-	^{t}Cont_Exit + ^{t}MRW	-	^{t}Cont_Exit + ^{t}MRW	-	^{t}Cont_Exit + ^{t}MRW	ns	
Registration of MRW continuous burst mode exit to end of training mode	^{t}Cont_Exit	-	CL+BL/2+10 *n*CK	-	CL+BL/2+10*n*CK	-	CL+BL/2+10 *n*CK	ns	

Table 464: DDR5 5600-6400: Read Preamble Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay from MRW command to DQS driven	^{t}SDOn	-	max(12*n*CK, 20ns)	-	max(12*n*CK, 20ns)	-	max(12*n*CK, 20ns)		
Delay from MRW command to DQS disabled	^{t}SDOff	-	max(12*n*CK, 20ns)	-	max(12*n*CK, 20ns)	-	max(12*n*CK, 20ns)		

Table 465: DDR5 5600-6400: CA Training Mode Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CATM entry command to start of training samples time	^{t}CATM_Entry	20	-	20	-	20	-	ns	
Registration of CATM exit CS_n assertion to end of training mode (when DQ is no longer driven by the device).	^{t}CATM_Exit	-	14	-	14	-	14	ns	
Registration of CATM exit to next valid command delay	^{t}CATM_Exit_Delay	20	-	20	-	20	-	ns	
Time from sample evaluation to output on DQ bus	^{t}CATM_Valid	-	20	-	20	-	20	ns	
Time output is available on DQ bus	^{t}CATM_DQ_Window	2	-	2	-	2	-	*n*CK	28
CS_n assertion duration to exit CATM	^{t}CATM_CS_Exit	2	8	2	8	2	8	*n*CK	

Table 466: DDR5 5600-6400: CS Training Mode Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CSTM entry command to start of training samples time	tCSTM_Entry	20	-	20	-	20	-	ns	
Registration of CSTM exit command to end of training mode	tCSTM_Exit	-	20	-	20	-	20	ns	
Registration of CSTM exit to next valid command delay	tCSTM_Exit_Delay	20	-	20	-	20	-	ns	
Time from sample evaluation to output on DQ bus	tCSTM_Valid	-	20	-	20	-	20	ns	
Time output is available on DQ bus	tCSTM_DQ_Window	2	-	2	-	2	-	*n*CK	28
Min time between last CS_n pulse and first pulse of MPC command to exit CSTM	tCSTM_Min_to_MPC_exit	4	-	4	-	4	-	*n*CK	

Table 467: DDR5 5600-6400: Write Leveling Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Write leveling pulse enable: time from write leveling training enable MRW to when internal write leveling pulse logic level is valid	tWLPEN	–	15	–	15	–	15	ns	
Write leveling output delay	tWLO	–	9.5	–	9.5	–	9.5	ns	
Width of write leveling internal pulse	tWL_-Pulse_Width	2	-	2	-	2	-	tCK	18
Write leveling write to subsequent command spacing	tWL_Write	max(CWL, last DQS differential toggle) + tWLO (MAX) + 2*n*CK	–	max(CWL, last DQS differential toggle) + tWLO (MAX) + 2*n*CK	–	max(CWL, last DQS differential toggle) + tWLO (MAX) + 2*n*CK	–		

Table 468: DDR5 5600-6400: V_{REFCA}/V_{REFCS} Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
VREFCA/VREFCS command to any other valid command delay	tVREFCA_Delay/ tVREFCS_Delay	tMRD	-	tMRD	-	tMRD	-	*n*CK	

Table 468: DDR5 5600-6400: V_{REFCA}/V_{REFCS} Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Time CS_n is held LOW to register VREFCA/VREFCS command	^{t}VREFCA_CS/ ^{t}VREFCS_CS	3.5	8	3.8	8	3.5	8	*n*CK	19,20
MIN time between stable VREFCA command and first falling CS edge (SETUP)	^{t}MC_VREFCA_Setup	3	-	3	-	3	-	*n*CK	11
MIN time between first rising CS edge and stable VREFCA command (HOLD)	^{t}MC_VREFCA_Hold	3	-	3	-	3	-	*n*CK	11
MIN time between stable VREFCS command and first falling CS edge (SETUP)	^{t}MC_VREFCS_Setup	3	-	3	-	3	-	*n*CK	11
MIN time between first rising CS edge and stable VREFCS command (HOLD)	^{t}MC_VREFCS_Hold	3	-	3	-	3	-	*n*CK	11

Table 469: DDR5 5600-6400: hPPR/sPPR Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
hPPR programming time (x4/x8)	^{t}PGMa	1000	-	1000	-	1000	-	ms	
hPPR programming time (x16)	^{t}PGMb	2000	-	2000	-	2000	-	ms	
sPPR programming time	^{t}PGM_sPPR	CWL+8^{t}CK+ ^{t}WR		CWL+8^{t}CK+ ^{t}WR		CWL+8^{t}CK +^{t}WR		^{t}CK	
hPPR/sPPR recognition time	^{t}PGM_Exit	^{t}RP	-	^{t}RP	-	^{t}RP	-	ns	
hPPR program exit and new address setting time	^{t}PGMPST	50	-	50	-	50	-	µs	
sPPR program exit and new address setting time	^{t}PGMP-ST_sPPR	^{t}MRD	-	^{t}MRD	-	^{t}MRD	-	ns	

Table 470: DDR5 5600-6400: DQS Interval Oscillator Readout Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay time from DQS interval oscillator stop to mode register readout in manual mode	^{t}OSCOM	^{t}MPC_Delay	-	^{t}MPC_Delay	-	^{t}MPC_Delay	-	*n*CK	24
Delay time from DQS interval oscillator stop to mode register readout in automatic mode	^{t}OSCOA	^{t}MRD	-	^{t}MRD	-	^{t}MRD	-	*n*CK	24
DQS interval oscillator start gap in automatic stop mode	^{t}OSCS	^{t}MPC_Delay + DQS interval timer run time						*n*CK	24

Table 471: DDR5 5600-6400: ESC Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ECS operation time	$^{t}ECSc$	max(76*n*CK,110ns)	-	max(176*n*CK, 110ns)	-	max(176*n*CK, 110ns)	-		

Table 472: DDR5 5600-6400: CRC Error Reporting Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
CRC error to ALERT n_latency	$^{t}CRC\_ALERT$	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	12	20	12	20	12	20	*n*CK	

Timing Parameters for DDR5 6800-7600

Analog timing parameters are to be rounded to 1ps of accuracy. Parameter minimum values, which scale with ^{t}CK (MIN), are to be defined using the ^{t}CK (MIN) in the associated data rate.

Table 473: DDR5 6800-7600: Clock Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Average clock period	$^{t}CK,AVG$	0.294		0.277	–	0.263	–	ns	23

Table 474: DDR5 6800-7600: Command and Address Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum READ to READ command delay for same bank group	$^{t}CCD\_L$	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK, ns	
Minimum WRITE to WRITE command delay for same bank group	$^{t}CCD\_L\_WR$	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK, ns	
Minimum WRITE to WRITE command delay for same bank group, second WRITE not RMW	$^{t}CCD\_L\_WR2$	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK	
Minimum READ to WRITE command delay for same bank group	$^{t}CCD\_L\_RTW$	TBD						*n*CK, ns	30,31,36
Minimum WRITE to READ command for same bank group	$^{t}CCD\_L\_WTR$	TBD						*n*CK, ns	30,32
READ to READ command delay for different bank group	$^{t}CCD\_S$	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK	

Table 474: DDR5 6800-7600: Command and Address Timing (Continued)

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum WRITE to WRITE command delay for different bank group	^{t}CCD_S_WR	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK	
Minimum READ to WRITE command delay for different bank group	^{t}CCD_S_RTW	TBD						*nCK, ns*CK	30,31 ,36
Minimum WRITE to READ command delay for different bank group	^{t}CCD_S_WTR	TBD						*nCK, ns*CK	30,32
Minimum WRITE to READ with AUTO PRE-CHARGE command for same bank	^{t}CCD_WTRA	TBD						*n*CK, ns	30,32 ,35
ACTIVATE to ACTIVATE command delay to same bank group for 1KB page size	^{t}RRD_L,1K	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK, ns	
ACTIVATE to ACTIVATE command delay to same bank group for 2KB page size	^{t}RRD_L,2K	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK, ns	
ACTIVATE to ACTIVATE command delay to different bank group for 1KB page size	^{t}RRD_S,1K	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK	
ACTIVATE to ACTIVATE command delay to different bank group for 2KB page size	^{t}RRD_S,2K	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK	
Four activate window for 2KB page size	^{t}FAW,2K	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK, ns	
Four activate window for 1KB page size	^{t}FAW,1K	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK, ns	
READ command to PRE-CHARGE command delay	^{t}RTP	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK, ns	
PRECHARGE to PRE-CHARGE delay	^{t}PPD	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK	37
WRITE recovery time	^{t}WR	TBD	TBD	TBD	TBD	TBD	TBD	ns	
DLL locking time	^{t}DLLK	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK	

Table 475: DDR5 6800-7600: Mode Register Read/Write Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Mode register READ command period	^{t}MRR	max(14ns, 16*n*CK)	-	max(14ns, 16*n*CK)	-	max(14ns, 16*n*CK)	-		2

Table 475: DDR5 6800-7600: Mode Register Read/Write Timing (Continued)

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Mode register READ pattern to mode register READ pattern command spacing	^{t}MRR_p	8	-	8	-	8	-	*n*CK	
Mode register WRITE command period	^{t}MRW	max(5ns, 8*n*CK)	-	max(5ns, 8*n*CK)	-	max(5ns, 8*n*CK)	-		2
Mode register SET command delay	^{t}MRD	max(14ns, 16*n*CK)	-	max(14ns, 16*n*CK)	-	max(14ns, 16*n*CK)	-		
DFE mode register WRITE update delay time	^{t}DFE	80	-	80	-	80	-	ns	3

Table 476: DDR5 6800-7600: Data Strobe Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential high toggle pulse width during WRITE preamble	^{t}DQSH_pre	TBD	-	TBD	-	TBD	-	*n*CK	
DQS_t, DQS_c differential low toggle pulse width during WRITE preamble	^{t}DQSL_pre	TBD	-	TBD	-	TBD	-	*n*CK	
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c	^{t}DQSCK	TBD	TBD	TBD	TBD	TBD	TBD	^{t}CK	7,10,17
DQS_t, DQS_c rising edge output variance window	^{t}DQSCKI	-	TBD	-	TBD	-	TBD	^{t}CK	8,9,10, 17,34

Table 477: DDR5 6800-7600: Write Enable Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
2-^{t}CK WRITE preamble enable window	^{t}WPRE_EN_2^{t}CK	TBD	-	TBD	-	TBD	-	^{t}CK	6
3-^{t}CK WRITE preamble enable window	^{t}WPRE_EN_3^{t}CK	TBD	-	TBD	-	TBD	-	^{t}CK	6
4-^{t}CK WRITE preamble enable window	^{t}WPRE_EN_4^{t}CK	TBD	-	TBD	-	TBD	-	^{t}CK	6
Final trained value of host DQS_t-DQS_c timing relative to CWL CK_t-CK_c edge	^{t}DQSoffset	TBD	TBD	TBD	TBD	TBD	TBD	^{t}CK	26
Write leveling setup time	^{t}WLS	-80	80	-80	80	-80	80	ps	
Write leveling hold time	^{t}WLH	-80	80	-80	80	-80	80	ps	

Table 477: DDR5 6800-7600: Write Enable Timing (Continued)

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Voltage/temperature drift window of first rising DQS_t preamble edge relative to CWL CK_t-CK_c edge (x4/x8/x16)	^{t}DQSD	TBD	TBD	TBD	TBD	TBD	TBD	^{t}CK	5,32
Host and system voltage/temperature drift window of first rising DQS_t pre-amble edge relative to CWL CK_t-CK_c edge (x4/x8/x16)	^{t}DQSS	TBD	TBD	TBD	TBD	TBD	TBD	^{t}CK	5,32

Table 478: DDR5 6800-7600: MPSM Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MPSM exit to first valid command delay	^{t}MPSMX	^{t}MRD	-	^{t}MRD	-	^{t}MRD	-	ns	

Table 479: DDR5 6800-7600: ZQ Calibration Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ZQ calibration time	^{t}ZQCAL	1		1		1		µs	
ZQ calibration latch time	^{t}ZQLAT	max(30ns, 8*n*CK)		max(30ns, 8*n*CK)		max(30ns, 8*n*CK)			

Table 480: DDR5 6800-7600: Reset Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
RESET_n low time for reset initialization with stable power	^{t}PW_RESET	1	-	1	-	1	-	µs	
Time after RESET_n assertion to ODT off	^{t}RST_ADC	-	50	-	50	-	50	ns	

Table 481: DDR5 6800-7600: Self Refresh Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Command pass disable delay	^{t}CPDED	max(5ns, 8*n*CK)	-	max(5ns, 8*n*CK)	-	max(5ns, 8*n*CK)	-	*n*CK, ns	
Self refresh CS_n low pulse width	^{t}CSL	10	-	10	-	10	-	ns	

Table 481: DDR5 6800-7600: Self Refresh Timing (Continued)

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Self refresh exit CS_n high pulse width	^{t}CSH_SRexit	13	30	13	30	13	30	ns	
Self refresh exit CS_n low pulse width	^{t}CSL_SRexit	3*n*CK	30ns	3*n*CK	30ns	3*n*CK	30ns	*n*CK, ns	12
Self refresh exit CS_n low pulse width with frequency change	^{t}CSL_FreqChg	V_{REFCA_time}	-	V_{REFCA_time}	-	V_{REFCA_time}	-	ns	13
Valid clock requirement before SRX	^{t}CKSRX	max(3.5ns, 8*n*CK)	-	max(3.5ns, 8*n*CK)	-	max(3.5ns,8 *n*CK)	-	*n*CK, ns	
Valid clock requirement after SRE	^{t}CKLCS	^{t}CPDED + 1*n*CK	-	^{t}CPDED + 1*n*CK	-	^{t}CPDED + 1*n*CK	-	*n*CK, ns	
Self refresh exit CS_n HIGH	^{t}CASRX	0	-	0	-	0	-	ns	
Exit self refresh to commands not requiring a locked DLL	^{t}XS	^{t}RFC1	-	^{t}RFC1	-	^{t}RFC1	-	*n*CK	
Exit self refresh to commands requiring a locked DLL	^{t}XS_DLL	^{t}DLLK	-	^{t}DLLK	-	^{t}DLLK	-	ns	

Table 482: DDR5 6800-7600: Power-Down Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Command pass disable delay	^{t}CPDED	max(5ns, 8*n*CK)	-	max(5ns, 8*n*CK)	-	max(5ns, 8*n*CK)	-	ns	
Power-down time	^{t}PD	max(7.5ns, 8*n*CK)	5*^{t}REFI1 (normal) 9*^{t}REFI2 (FGR)	max(7.5ns, 8*n*CK)	5*^{t}REFI1 (normal) 9*^{t}REFI2 (FGR)	max(7.5ns, 8*n*CK)	5*^{t}REFI1 (normal) 9*^{t}REFI2 (FGR)	ns	28
Exit power-down to next valid command	^{t}XP	max(7.5ns, 8*n*CK)	-	max(7.5ns, 8*n*CK)	-	max(7.5ns, 8*n*CK)		ns	
Timing of ACT command to POWER-DOWN ENTRY command	^{t}ACTPDEN	2	-	2	-	2	-	*n*CK	14
Timing of PREab, PREsb or PREpb command to POWER-DOWN ENTRY command	^{t}PRPDEN	2	-	2	-	2	-	*n*CK	14
Timing of READ or READ w/ AP command to POWER-DOWN ENTRY command	^{t}RDPDEN	CL+RBL/2+1	-	CL+RBL/2+ 1	-	CL+RBL/2+ 1	-	*n*CK	24

Table 482: DDR5 6800-7600: Power-Down Timing (Continued)

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Timing of WRITE command to POWER-DOWN ENTRY command	tWRPDEN	CWL+WBL/2+(tWR/tCK(avg))+1	-	CWL+WBL/2+(tWR/tCK(avg))+1	-	CWL+WBL/2+(tWR/tCK(avg))+1	-	nCK	15,24
Timing of WRITE w/ AP command to POWER-DOWN ENTRY command	tWRAPDEN	CWL+WBL/2+tWR+1		CWL+WBL / 2+tWR+1		CWL+WBL / 2+tWR+1		nCK	16,24
Timing of REFab or REFsb command to POWER-DOWN ENTRY command	tREFPDEN	2	-	2	-	2	-	nCK	
Timing of MRR command to POWER-DOWN ENTRY command	tMRRPDEN	CL+8+1	-	CL+8+1	-	CL+8+1	-	nCK	24
Timing of MRW command to POWER-DOWN ENTRY command	tMRWPDEN	tMRD (MIN)	-	tMRD (MIN)	-	tMRD (MIN)	-	nCK	
Timing of MPC command to POWER-DOWN ENTRY command	tMPCPDEN	tMPC_delay	-	tMPC_delay	-	tMPC_delay	-	nCK	25

Table 483: DDR5 6800-7600: MPC Command Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MPC to any other valid command	tMPC_Delay	tMRD	-	tMRD	-	tMRD	-	nCK	
Time between stable MPC command and first falling CS edge (setup)	tMC_MPC_Setup	3	-	3	-	3	-	nCK	22
Time between first rising CS edge and stable MPC command (HOLD)	tMC_MPC_Hold	3	-	3	-	3	-	nCK	22
Time CS_n is held LOW to register MPC command	tMPC_CS	3.5	8	3.5	8	3.5	8	nCK	21

Table 484: DDR5 6800-7600: PDA Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
PDA ENUMERATE ID command to any other command cycle	tPDA_DELAY	TBD	-	TBD	-	TBD	-	ns	
Delay to rising strobe edge used for sampling DQ during PDA operation	tPDA_DQS_DELAY	TBD	-	TBD	-	TBD	-	ns	4
DQS setup time during PDA operation	tPDA_S	TBD	-	TBD	-	TBD	-	nCK	

Table 484: DDR5 6800-7600: PDA Timing (Continued)

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQS hold time during PDA operation	^{t}PDA_H	TBD	-	TBD	-	TBD	-	*n*CK	

Table 485: DDR5 6800-7600: Read Training Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of MRW continuous burst mode exit to next valid command delay	^{t}Cont_Exit_Delay	-	^{t}Cont_Exit + ^{t}MRW	-	^{t}Cont_Exit + ^{t}MRW	-	^{t}Cont_Exit + ^{t}MRW	ns	
Registration of MRW continuous burst mode exit to end of training mode	^{t}Cont_Exit	-	CL+BL/2+10 *n*CK	-	CL+BL/2+10*n*CK	-	CL+BL/2+10 *n*CK	ns	

Table 486: DDR5 6800-7600: Read Preamble Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay from MRW command to DQS driven	^{t}SDOn	-	max(12*n*CK, 20ns)	-	max(12*n*CK, 20ns)	-	max(12*n*CK, 20ns)		
Delay from MRW command to DQS disabled	^{t}SDOff	-	max(12*n*CK, 20ns)	-	max(12*n*CK, 20ns)	-	max(12*n*CK, 20ns)		

Table 487: DDR5 6800-7600: CA Training Mode Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CATM entry command to start of training samples time	^{t}CATM_Entry	20	-	20	-	20	-	ns	
Registration of CATM exit CS_n assertion to end of training mode (when DQ is no longer driven by the device).	^{t}CATM_Exit	-	14	-	14	-	14	ns	
Registration of CATM exit to next valid command delay	^{t}CATM_Exit_Delay	20	-	20	-	20	-	ns	
Time from sample evaluation to output on DQ bus	^{t}CATM_Valid	-	20	-	20	-	20	ns	
Time output is available on DQ bus	^{t}CATM_DQ_Window	2	-	2	-	2	-	*n*CK	27
CS_n assertion duration to exit CATM	^{t}CATM_CS_Exit	2	8	2	8	2	8	*n*CK	

Table 488: DDR5 6800-7600: CS Training Mode Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CSTM entry command to start of training samples time	^{t}CSTM_Entry	20	-	20	-	20	-	ns	
Min time between last CS_n pulse and first pulse of MPC command to exit CSTM	^{t}CSTM_Min_to_MPC_exit	4	-	4	-	4	-	*n*CK	
Registration of CSTM exit command to end of training mode	^{t}CSTM_Exit	-	20	-	20	-	20	ns	
Time from sample evaluation to output on DQ bus	^{t}CSTM_Valid	-	20	-	20	-	20	ns	
Time output is available on DQ bus	^{t}CSTM_DQ_Window	2	-	2	-	2	-	*n*CK	27
Registration of CSTM exit to next valid command delay	^{t}CSTM_Exit_Delay	20	-	20	-	20	-	ns	

Table 489: DDR5 6800-7600: Write Leveling Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Write leveling pulse enable: time from write leveling training enable MRW to when internal write leveling pulse logic level is valid	^{t}WLPEN	–	15	–	15	–	15	ns	
Write leveling output delay	^{t}WLO	–	9.5	–	9.5	–	9.5	ns	
Width of write leveling internal pulse	^{t}WL_-Pulse_Width	2	-	2	-	2	-	^{t}CK	18
Write leveling write to subsequent command spacing	^{t}WL_Write	max(CWL, last DQS differential toggle) + ^{t}WLO (MAX) + 2*n*CK	–	max(CWL, last DQS differential toggle) + ^{t}WLO (MAX) + 2*n*CK	–	max(CWL, last DQS differential toggle) + ^{t}WLO (MAX) + 2*n*CK	–		

Table 490: DDR5 6800-7600: V_{REFCA}/V_{REFCS} Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
VREFCA/VREFCS command to any other valid command delay	^{t}VREFCA_Delay/ ^{t}VREFCS_Delay	^{t}MRD	-	^{t}MRD	-	^{t}MRD	-	*n*CK	

Table 490: DDR5 6800-7600: V_{REFCA}/V_{REFCS} Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Time CS_n is held LOW to register VREFCA/VREFCS command	^{t}VREFCA_CS/ ^{t}VREFCS_CS	3.5	8	3.8	8	3.5	8	*n*CK	19,20
MIN time between stable VREFCA command and first falling CS edge (SETUP)	^{t}MC_VREFCA_Setup	3	-	3	-	3	-	*n*CK	11
MIN time between first rising CS edge and stable VREFCA command (HOLD)	^{t}MC_VREFCA_Hold	3	-	3	-	3	-	*n*CK	11
MIN time between stable VREFCS command and first falling CS edge (SETUP)	^{t}MC_VREFCS_Setup	3	-	3	-	3	-	*n*CK	11
MIN time between first rising CS edge and stable VREFCS command (HOLD)	^{t}MC_VREFCS_Hold	3	-	3	-	3	-	*n*CK	11

Table 491: DDR5 6800-7600: hPPR/sPPR Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
hPPR programming time (x4/x8)	^{t}PGMa	1000	-	1000	-	1000	-	ms	
hPPR programming time (x16)	^{t}PGMb	2000	-	2000	-	2000	-	ms	
sPPR programming time	^{t}PGM_sPPR	CWL+8^{t}CK+ ^{t}WR		CWL+8^{t}CK+ ^{t}WR		CWL+8^{t}CK +^{t}WR		^{t}CK	
hPPR/sPPR recognition time	^{t}PGM_Exit	^{t}RP	-	^{t}RP	-	^{t}RP	-	ns	
hPPR program exit and new address setting time	^{t}PGMPST	50	-	50	-	50	-	µs	
sPPR program exit and new address setting time	^{t}PGMP-ST_sPPR	^{t}MRD	-	^{t}MRD	-	^{t}MRD	-	ns	

Table 492: DDR5 6800-7600: DQS Interval Oscillator Readout Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay time from DQS interval oscillator stop to mode register readout in manual mode	^{t}OSCOM	^{t}MPC_Delay	-	^{t}MPC_Delay	-	^{t}MPC_Delay	-	*n*CK	
Delay time from DQS interval oscillator stop to mode register readout in automatic mode	^{t}OSCOA	^{t}MRD	-	^{t}MRD	-	^{t}MRD	-	*n*CK	
DQS interval oscillator start gap in automatic stop mode	^{t}OSCS	^{t}MPC_Delay + DQS interval timer run time						*n*CK	22

Table 493: DDR5 6800-7600: ESC Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ECS operation time	^{t}ECSc	max(45*n*CK, 110ns)	-	max(45*n*CK, 110ns)	-	max(45*n*CK, 110ns)	-		

Table 494: DDR5 6800-7600: CRC Error Reporting Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
CRC error to ALERT n_latency	^{t}CRC_ALERT	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	12	20	12	20	12	20	*n*CK	

Timing Parameters for DDR5 8000-8800

Analog timing parameters are to be rounded to 1ps of accuracy. Parameter minimum values, which scale with ^{t}CK (MIN), are to be defined using the ^{t}CK (MIN) in the associated data rate.

Table 495: DDR5 8000-8800: Clock Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Average clock period	^{t}CK,AVG	0.250		0.238	–	0.227	–	ns	23

Table 496: DDR5 8000-8800: Command and Address Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum READ to READ command delay for same bank group	^{t}CCD_L	TBD	-	TBD	-	TBD	-	*n*CK, ns	
Minimum WRITE to WRITE command delay for same bank group	^{t}CCD_L_WR	TBD	–	TBD	–	TBD	–	*n*CK, ns	
Minimum WRITE to WRITE command delay for same bank group, second WRITE not RMW	^{t}CCD_L_WR2	TBD	–	TBD	–	TBD	–	*n*CK	
Minimum READ to WRITE command delay for same bank group	^{t}CCD_L_RTW	TBD						*n*CK, ns	30,31,36
Minimum WRITE to READ command for same bank group	^{t}CCD_L_WTR	TBD						*n*CK, ns	30,32
READ to READ command delay for different bank group	^{t}CCD_S	TBD	-	TBD	-	TBD	-	*n*CK	

Table 496: DDR5 8000-8800: Command and Address Timing (Continued)

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum WRITE to WRITE command delay for different bank group	^{t}CCD_S_WR	TBD	-	TBD	-	TBD	-	*n*CK	
Minimum READ to WRITE command delay for different bank group	^{t}CCD_S_RTW	TBD						*nCK, ns*CK	30,31 ,36
Minimum WRITE to READ command delay for different bank group	^{t}CCD_S_WTR	TBD						*nCK, ns*CK	30,32
Minimum WRITE to READ with AUTO PRE-CHARGE command for same bank	^{t}CCD_WTRA	TBD						*n*CK, ns	30,32 ,35
ACTIVATE to ACTIVATE command delay to same bank group for 1KB page size	^{t}RRD_L,1K	TBD	-	TBD	-	TBD	-	*n*CK, ns	
ACTIVATE to ACTIVATE command delay to same bank group for 2KB page size	^{t}RRD_L,2K	TBD	-	TBD	-	TBD	-	*n*CK, ns	
ACTIVATE to ACTIVATE command delay to different bank group for 1KB page size	^{t}RRD_S,1K	TBD	-	TBD	-	TBD	-	*n*CK	
ACTIVATE to ACTIVATE command delay to different bank group for 2KB page size	^{t}RRD_S,2K	TBD	-	TBD	-	TBD	-	*n*CK	
Four activate window for 2KB page size	^{t}FAW,2K	TBD	-	TBD	-	TBD	-	*n*CK, ns	
Four activate window for 1KB page size	^{t}FAW,1K	TBD	-	TBD	-	TBD	-	*n*CK, ns	
READ command to PRE-CHARGE command delay	^{t}RTP	TBD	-	TBD	-	TBD	-	*n*CK, ns	
PRECHARGE to PRE-CHARGE delay	^{t}PPD	TBD	-	TBD	-	TBD	-	*n*CK	37
WRITE recovery time	^{t}WR	TBD	-	TBD	-	TBD	-	ns	
DLL locking time	^{t}DLLK	TBD	-	TBD	-	TBD	-	*n*CK	

Table 497: DDR5 8000-8800: Mode Register Read/Write Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Mode register READ command period	^{t}MRR	max(14ns, 16*n*CK)	-	max(14ns, 16*n*CK)	-	max(14ns, 16*n*CK)	-		2
Mode register READ pattern to mode register READ pattern command spacing	^{t}MRR_p	8	-	8	-	8	-	*n*CK	
Mode register WRITE command period	^{t}MRW	max(5ns, 8*n*CK)	-	max(5ns, 8*n*CK)	-	max(5ns, 8*n*CK)	-		2
Mode register SET command delay	^{t}MRD	max(14ns, 16*n*CK)	-	max(14ns, 16*n*CK)	-	max(14ns, 16*n*CK)	-		
DFE mode register WRITE update delay time	^{t}DFE	80	-	80	-	80	-	ns	3

Table 498: DDR5 8000-8800: Data Strobe Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential high toggle pulse width during WRITE preamble	^{t}DQSH_pre	TBD	-	TBD	-	TBD	-	*n*CK	
DQS_t, DQS_c differential low toggle pulse width during WRITE preamble	^{t}DQSL_pre	TBD	-	TBD	-	TBD	-	*n*CK	
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c	^{t}DQSCK	TBD	TBD	TBD	TBD	TBD	TBD	^{t}CK	7,10,17
DQS_t, DQS_c rising edge output variance window	^{t}DQSCKI	-	TBD	-	TBD	-	TBD	^{t}CK	8,9,10,17,34

Table 499: DDR5 8000-8800: Write Enable Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
2-^{t}CK WRITE preamble enable window	^{t}WPRE_EN_2^{t}CK	TBD	-	TBD	-	TBD	-	^{t}CK	6
3-^{t}CK WRITE preamble enable window	^{t}WPRE_EN_3^{t}CK	TBD	-	TBD	-	TBD	-	^{t}CK	6
4-^{t}CK WRITE preamble enable window	^{t}WPRE_EN_4^{t}CK	TBD	-	TBD	-	TBD	-	^{t}CK	6
Final trained value of host DQS_t-DQS_c timing relative to CWL CK_t-CK_c edge	^{t}DQSoffset	TBD	TBD	TBD	TBD	TBD	TBD	^{t}CK	26
Write leveling setup time	^{t}WLS	-80	80	-80	80	-80	80	ps	

Table 499: DDR5 8000-8800: Write Enable Timing (Continued)

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Write leveling hold time	^{t}WLH	-80	80	-80	80	-80	80	ps	
Voltage/temperature drift window of first rising DQS_t preamble edge relative to CWL CK_t-CK_c edge (x4/x8/x16)	^{t}DQSD	TBD	TBD	TBD	TBD	TBD	TBD	^{t}CK	5,32
Host and system voltage/temperature drift window of first rising DQS_t pre-amble edge relative to CWL CK_t-CK_c edge (x4/x8/x16)	^{t}DQSS	TBD	TBD	TBD	TBD	TBD	TBD	^{t}CK	5,32

Table 500: DDR5 8000-8800: MPSM Timing

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MPSM exit to first valid command delay	^{t}MPSMX	^{t}MRD	-	^{t}MRD	-	^{t}MRD	-	ns	

Table 501: DDR5 8000-8800: ZQ Calibration Timing

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ZQ calibration time	^{t}ZQCAL	1		1		1		µs	
ZQ calibration latch time	^{t}ZQLAT	max(30ns, 8*n*CK)		max(30ns, 8*n*CK)		max(30ns, 8*n*CK)			

Table 502: DDR5 8000-8800: Reset Timing

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
RESET_n low time for reset initialization with stable power	^{t}PW_RESET	1	-	1	-	1	-	µs	
Time after RESET_n assertion to ODT off	^{t}RST_ADC	-	50	-	50	-	50	ns	

Table 503: DDR5 8000-8800: Self Refresh Timing

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Command pass disable delay	^{t}CPDED	max(5ns, 8*n*CK)	-	max(5ns, 8*n*CK)	-	max(5ns, 8*n*CK)	-	*n*CK, ns	

Table 503: DDR5 8000-8800: Self Refresh Timing (Continued)

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Self refresh CS_n low pulse width	^{t}CSL	10	-	10	-	10	-	ns	
Self refresh exit CS_n high pulse width	$^{t}CSH\_SRexit$	13	30	13	30	13	30	ns	
Self refresh exit CS_n low pulse width	$^{t}CSL\_SRexit$	3*n*CK	30ns	3*n*CK	30ns	3*n*CK	30ns	*n*CK, ns	12
Self refresh exit CS_n low pulse width with frequency change	$^{t}CSL\_FreqChg$	V_{REFCA_time}	-	V_{REFCA_time}	-	V_{REFCA_time}	-	ns	13
Valid clock requirement before SRX	$^{t}CKSRX$	max(3.5ns, 8*n*CK)	-	max(3.5ns, 8*n*CK)	-	max(3.5ns,8 *n*CK)	-	*n*CK, ns	
Valid clock requirement after SRE	$^{t}CKLCS$	$^{t}CPDED$ + 1*n*CK	-	$^{t}CPDED$ + 1*n*CK	-	$^{t}CPDED$ + 1*n*CK	-	*n*CK, ns	
Self refresh exit CS_n HIGH	$^{t}CASRX$	0	-	0	-	0	-	ns	
Exit self refresh to commands not requiring a locked DLL	^{t}XS	$^{t}RFC1$	-	$^{t}RFC1$	-	$^{t}RFC1$	-	*n*CK	
Exit self refresh to commands requiring a locked DLL	$^{t}XS\_DLL$	$^{t}DLLK$	-	$^{t}DLLK$	-	$^{t}DLLK$	-	ns	

Table 504: DDR5 8000-8800: Power-Down Timing

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Command pass disable delay	$^{t}CPDED$	max(5ns, 8*n*CK)	-	max(5ns, 8*n*CK)	-	max(5ns, 8*n*CK)	-	ns	
Power-down time	^{t}PD	max(7.5ns, 8*n*CK)	5*$^{t}REFI1$ (normal) 9*$^{t}REFI2$ (FGR)	max(7.5ns, 8*n*CK)	5*$^{t}REFI1$ (normal) 9*$^{t}REFI2$ (FGR)	max(7.5ns, 8*n*CK)	5*$^{t}REFI1$ (normal) 9*$^{t}REFI2$ (FGR)	ns	28
Exit power-down to next valid command	^{t}XP	max(7.5ns, 8*n*CK)	-	max(7.5ns, 8*n*CK)	-	max(7.5ns, 8*n*CK)		ns	
Timing of ACT command to POWER-DOWN ENTRY command	$^{t}ACTPDEN$	2	-	2	-	2	-	*n*CK	14
Timing of PREab, PREsb or PREpb command to POWER-DOWN ENTRY command	$^{t}PRPDEN$	2	-	2	-	2	-	*n*CK	14
Timing of READ or READ w/ AP command to POWER-DOWN ENTRY command	$^{t}RDPDEN$	CL+RBL/2+1	-	CL+RBL/2+ 1	-	CL+RBL/2+ 1	-	*n*CK	24

Table 504: DDR5 8000-8800: Power-Down Timing (Continued)

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Timing of WRITE command to POWER-DOWN ENTRY command	tWRPDEN	CWL+WBL/2+(tWR/tCK(avg))+1	-	CWL+WBL/2+(tWR/tCK(avg))+1	-	CWL+WBL/2+(tWR/tCK(avg))+1	-	nCK	15,24
Timing of WRITE w/ AP command to POWER-DOWN ENTRY command	tWRAPDEN	CWL+WBL/2+tWR+1		CWL+WBL / 2+tWR+1		CWL+WBL / 2+tWR+1		nCK	16,24
Timing of REFab or REFsb command to POWER-DOWN ENTRY command	tREFPDEN	2	-	2	-	2	-	nCK	
Timing of MRR command to POWER-DOWN ENTRY command	tMRRPDEN	CL+8+1	-	CL+8+1	-	CL+8+1	-	nCK	24
Timing of MRW command to POWER-DOWN ENTRY command	tMRWPDEN	tMRD (MIN)	-	tMRD (MIN)	-	tMRD (MIN)	-	nCK	
Timing of MPC command to POWER-DOWN ENTRY command	tMPCPDEN	tMPC_delay	-	tMPC_delay	-	tMPC_delay	-	nCK	25

Table 505: DDR5 8000-8800: MPC Command Timing

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MPC to any other valid command	tMPC_Delay	tMRD	-	tMRD	-	tMRD	-	nCK	
Time between stable MPC command and first falling CS edge (setup)	tMC_MPC_Setup	3	-	3	-	3	-	nCK	22
Time between first rising CS edge and stable MPC command (HOLD)	tMC_MPC_Hold	3	-	3	-	3	-	nCK	22
Time CS_n is held LOW to register MPC command	tMPC_CS	3.5	8	3.5	8	3.5	8	nCK	21

Table 506: DDR5 8000-8800: PDA Timing

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
PDA ENUMERATE ID command to any other command cycle	tPDA_DELAY	TBD	-	TBD	-	TBD	-	ns	
Delay to rising strobe edge used for sampling DQ during PDA operation	tPDA_DQS_DELAY	TBD	-	TBD	-	TBD	-	ns	4
DQS setup time during PDA operation	tPDA_S	TBD	-	TBD	-	TBD	-	nCK	

Table 506: DDR5 8000-8800: PDA Timing (Continued)

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQS hold time during PDA operation	^{t}PDA_H	TBD	-	TBD	-	TBD	-	*n*CK	

Table 507: DDR5 8000-8800: Read Training Timing

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of MRW continuous burst mode exit to next valid command delay	^{t}Cont_Exit_Delay	-	^{t}Cont_Exit + ^{t}MRW	-	^{t}Cont_Exit + ^{t}MRW	-	^{t}Cont_Exit + ^{t}MRW	ns	
Registration of MRW continuous burst mode exit to end of training mode	^{t}Cont_Exit	-	CL+BL/2+10 *n*CK	-	CL+BL/2+10 *n*CK	-	CL+BL/2+10 *n*CK	ns	

Table 508: DDR5 8000-8800: Read Preamble Timing

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay from MRW command to DQS driven	^{t}SDOn	-	max(12*n*CK, 20ns)	-	max(12*n*CK, 20ns)	-	max(12*n*CK, 20ns)		
Delay from MRW command to DQS disabled	^{t}SDOff	-	max(12*n*CK, 20ns)	-	max(12*n*CK, 20ns)	-	max(12*n*CK, 20ns)		

Table 509: DDR5 8000-8800: CA Training Mode Timing

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CATM entry command to start of training samples time	^{t}CATM_Entry	20	-	20	-	20	-	ns	
Registration of CATM exit CS_n assertion to end of training mode (when DQ is no longer driven by the device).	^{t}CATM_Exit	-	14	-	14	-	14	ns	
Registration of CATM exit to next valid command delay	^{t}CATM_Exit_Delay	20	-	20	-	20	-	ns	
Time from sample evaluation to output on DQ bus	^{t}CATM_Valid	-	20	-	20	-	20	ns	
Time output is available on DQ bus	^{t}CATM_DQ_Window	2	-	2	-	2	-	*n*CK	27
CS_n assertion duration to exit CATM	^{t}CATM_CS_Exit	2	8	2	8	2	8	*n*CK	

Table 510: DDR5 8000-8800: CS Training Mode Timing

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CSTM entry command to start of training samples time	tCSTM_Entry	20	-	20	-	20	-	ns	
Min time between last CS_n pulse and first pulse of MPC command to exit CSTM	tCSTM_Min_to_MPC_exit	4	-	4	-	4	-	*n*CK	
Registration of CSTM exit command to end of training mode	tCSTM_Exit	-	20	-	20	-	20	ns	
Time from sample evaluation to output on DQ bus	tCSTM_Valid	-	20	-	20	-	20	ns	
Time output is available on DQ bus	tCSTM_DQ_Window	2	-	2	-	2	-	*n*CK	27
Registration of CSTM exit to next valid command delay	tCSTM_Exit_Delay	20	-	20	-	20	-	ns	

Table 511: DDR5 8000-8800: Write Leveling Timing

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Write leveling pulse enable: time from write leveling training enable MRW to when internal write leveling pulse logic level is valid	tWLPEN	–	15	–	15	–	15	ns	
Write leveling output delay	tWLO	–	9.5	–	9.5	–	9.5	ns	
Width of write leveling internal pulse	tWL_-Pulse_Width	2	-	2	-	2	-	tCK	18
Write leveling write to subsequent command spacing	tWL_Write	max(CWL, last DQS differential toggle) + tWLO (MAX) + 2*n*CK	–	max(CWL, last DQS differential toggle) + tWLO (MAX) + 2*n*CK	–	max(CWL, last DQS differential toggle) + tWLO (MAX) + 2*n*CK	–		

Table 512: DDR5 8000-8800: V_{REFCA}/V_{REFCS} Timing

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
VREFCA/VREFCS command to any other valid command delay	tVREFCA_Delay/ tVREFCS_Delay	tMRD	-	tMRD	-	tMRD	-	*n*CK	

Table 512: DDR5 8000-8800: V_{REFCA}/V_{REFCS} Timing

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Time CS_n is held LOW to register VREFCA/VREFCS command	^{t}VREFCA_CS/ ^{t}VREFCS_CS	3.5	8	3.8	8	3.5	8	*n*CK	19,20
VREFCS command to any other valid command delay	^{t}VREFCS_Delay	^{t}MRD	-	^{t}MRD	-	^{t}MRD	-	*n*CK	
Time CS_n is held LOW to register VREFCS command	^{t}VREFCS_CS	3.5	8	3.8	8	3.5	8	*n*CK	19,20
MIN time between stable VREFCA command and first falling CS edge (SETUP)	^{t}MC_VREFCA_Setup	3	-	3	-	3	-	*n*CK	11
MIN time between first rising CS edge and stable VREFCA command (HOLD)	^{t}MC_VREFCA_Hold	3	-	3	-	3	-	*n*CK	11
MIN time between stable VREFCS command and first falling CS edge (SETUP)	^{t}MC_VREFCS_Setup	3	-	3	-	3	-	*n*CK	11
MIN time between first rising CS edge and stable VREFCS command (HOLD)	^{t}MC_VREFCS_Hold	3	-	3	-	3	-	*n*CK	11

Table 513: DDR5 8000-8800: hPPR/sPPR Timing

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
hPPR programming time (x4/x8)	^{t}PGMa	TBD	-	TBD	-	TBD	-	ms	
hPPR programming time (x16)	^{t}PGMb	TBD	-	TBD	-	TBD	-	ms	
sPPR programming time	^{t}PGM_sPPR	TBD		TBD		TBD		^{t}CK	
hPPR/sPPR recognition time	^{t}PGM_Exit	TBD	-	TBD	-	TBD	-	ns	
hPPR program exit and new address setting time	^{t}PGMPST	TBD	-	TBD	-	TBD	-	µs	
sPPR program exit and new address setting time	^{t}PGMP-ST_sPPR	TBD	-	TBD	-	TBD	-	ns	

Table 514: DDR5 8000-8800: DQS Interval Oscillator Readout Timing

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay time from DQS interval oscillator stop to mode register readout in manual mode	^{t}OSCOM	TBD	-	TBD	-	TBD	-	*n*CK	
Delay time from DQS interval oscillator stop to mode register readout in automatic mode	^{t}OSCOA	TBD	-	TBD	-	TBD	-	*n*CK	

Table 514: DDR5 8000-8800: DQS Interval Oscillator Readout Timing (Continued)

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQS interval oscillator start gap in automatic stop mode	^{t}OSCS	TBD						*n*CK	22

Table 515: DDR5 8000-8800: ESC Timing

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ECS operation time	^{t}ECSc	max(45*n*CK, 110ns)	-	max(45*n*CK, 110ns)	-	max(45*n*CK, 110ns)	-		

Table 516: DDR5 8000-8800: CRC Error Reporting Timing

Parameter	Symbol	8000		8400		8600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
CRC error to ALERT n_latency	^{t}CRC_ALERT	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	12	20	12	20	12	20	*n*CK	

Notes:
1. Start of internal write transaction is defined as follows: For BL16 (fixed by MRS and on-the-fly), rising clock edge 4-clock cycles after CWL. For BC8 (on-the-fly), rising clock edge 4 clock cycles after CWL.
2. MRR and MRW commands are not allowed with pages open.
3. Applies only to MRWs to DFE registers and is defined as the settling time before a new DFE setting is active.
4. The range of ^{t}PDA_DQS_DELAY specifies the full range of when the minimum of 16 strobe edges can be sent by the host controller.
5. Measured relative to the write leveling feedback, after write leveling training has been completed.
6. Includes min DQS and CK timing terms TBD.
7. Measured over full V_{DD} and temperature spec ranges.
8. Measured for a given part and for each DQS_t/DQS_c pair in case of x16 (part variation is excluded).
9. These parameters are verified by design and characterization, and may not be subject to production test.
10. Assume no jitter on input clock signals to the DRAM device.
11. Applies only to multicycle VREFCS/VREFCA commands when MR2:OP[4]=0b.
12. While in 2N mode, ^{t}CSL_SRexit is not statically held LOW, it pulses for each 2-cycle period for a min of 6*n*CK. See the 2N mode section for more details.
13. Since frequency can require $V_{REF,CA}$ and CA/CK/CS ODT changes, the min time is longer than the traditional t^{C}SL when the SRE command with CA9=L is used.
14. POWER DOWN command can be sent while operations such as row activation, precharge, auto-precharge or refresh are in progress; however, IDD spec is not applied until the operations are finished.
15. ^{t}WR is defined in ns, for calculation of ^{t}WRPDEN it is necessary to round up ^{t}WR/^{t}CK.
16. WR in clock cycles, as programmed in MR6.
17. Refer to Read Timing definition.
18. There is no max limit for the ^{t}WL_Pulse_Width; however, the write leveling internal pulse must begin at zero for each WRITE command.
19. Multiple cycles are used to avoid possible metastability of CS_n.
20. At the end of CSTM, it is assumed the host can place the CS_n appropriately and the VREFCA/VREFCS command can be issued as a single-cycle command.
21. The minimum ^{t}MPC_CS constraint applies only when the CS assertion duration setting is 0. The CS assertion duration MR setting must be set to enable single-cycle MPC commands. The earliest time to set the CS assertion duration MR is after CA training is complete, when MRW commands can be sent to the device.
22. Applies only to multicycle MPC commands when MR2:OP[2] = 0b.
23. ^{t}CK(AVG) MIN listed for reference only; refer to Speed Bin tables and Operations section for valid ^{t}CK(AVG) values.

24. In manual stop mode, DQS OSC START command must be followed by DQS OSC STOP command (MPC). Otherwise, DQS OSC reset value (MR46,47) cannot be guaranteed.
25. RD/WR/MRR can refer to both target command and non-target command when CA11 = H during PDE command.
26. ^{t}MPC_delay is a valid timing parameter for all MPC commands except:
    - Enter CS Training mode, Enter CA Training mode, PDA Enumerate ID, Enter PDA Enumerate Program mode because power-down entry is not supported for these MPC commands.
    - Apply VrefCA, VrefCS and RTT_CA/CS/CK because this MPC command requires waiting for VrefCA_time/VrefCS_time.
27. When measuring the ^{t}DQSoffset, ^{t}WLS and ^{t}WLH are reflected in the ^{t}DQSoffset value.
28. This timing parameter is applied to each DQ independently, not all-DQs valid window perspective.
29. Refresh to refresh max time interval limits ^{t}PD(MAX) to 5 x ^{t}REFI1 in normal refresh mode, 9 x ^{t}REFI2 in FGR mode.
30. CWL = CL-2.
31. RBL: Read burst length associated with READ command:
    - RBL = 32 (36 w/ RCRC on) for fixed 32 and BL32 in BL32 OTF mode
    - RBL = 16 (18 w/ RCRC on) for fixed 16 and BL16 in BL32 OTF mode
    - RBL = 16 (18 w/ RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
32. WBL: Write burst length associated with Write command:
    - WBL = 32 (36 w/ WCRC on) for fixed 32 and BL32 in BL32 OTF mode
    - WBL = 16 (18 w/ WCRC on) for fixed 16 and BL16 in BL32 OTF mode
    - WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
33. DDR5-3200 timings apply for data rates <2933 MT/s. For example, at 2000 MT/s, ^{t}DQSS(max) = (2000/2933)*0.25*^{t}WPRE_EN_ntck(min) = 0.17*^{t}WPRE_EN_ntck(min).
34. Measured at a fixed and constant V_{DD} and temperature condition.
35. ^{t}CCD_WRTA(min) is always greater than or equal to CWL + WBL/2 + ^{t}WR(min) - ^{t}RTP(min). When using the appropriate rounding algorithms, nCCD_WTRA(min) is always greater than or equal to CWL + WBL/2 + nWR(min) - nRTP(min).
36. The following is considered for ^{t}RTW equation:
    - 1 ^{t}CK must be added due to ^{t}DQS2CK.
    - Read DQS offset timing can pull in the ^{t}RTW timing.
    - 1 ^{t}CK must be added when 1.5 ^{t}CK postamble.
37. ^{t}PPD applies to any combination of precharge commands (PREab, PREsb, PREpb). ^{t}PPD also applies to any combination of precharge commands to a different die in a 3DS device.

Timing Parameters by Speed Grade: 3DS

Timing Parameters for 2H and 4H 3DS DDR5 3200-4000

The analog timing parameters in this section have been defined based on nominal ^{t}CK(avg)min according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

Table 517: 3DS DDR5 3200-4000: Clock Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Average clock period	^{t}CK,AVG	0.625	-0.681	0.555	-0.625	0.500	-0.555	ns	23

Table 518: 3DS DDR5 3200-4000: Command and Address Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum READ to READ command delay for same bank group in same logical rank	^{t}CCD_L_slr	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	*n*CK, ns	
Minimum WRITE to WRITE command delay for same bank group in same logical rank	^{t}CCD_L_WR_slr	max(32*n*CK, 20ns)	-	max(32*n*CK, 20ns)		max(32*n*CK, 20ns)		*n*CK, ns	
Minimum WRITE to WRITE command delay for same bank group, second WRITE not RMW, same logical rank	^{t}CCD_L_WR2_slr	max(16*n* CK, 10ns)	-	max(16*n* CK, 10ns)	-	max(16*n* CK, 10ns)	-	*n*CK, ns	
Minimum READ to WRITE command delay for same bank group in same logical rank	^{t}CCD_L_RTW_slr	CL - CWL + RBL/2 + 2^{t}CK - (READ DQS offset) + (^{t}RPST - 0.5^{t}CK) + ^{t}WPRE						*n*CK, ns	24,31,36
Minimum WRITE to READ command delay for same bank group in same logical rank	^{t}CCD_L_WTR_slr	CWL + WBL/2 + max(16 nCK,10ns)						*n*CK, ns	24,32
Minimum READ to READ command delay for different bank group in same logical rank	^{t}CCD_S_slr	8	-	8	-	8	-	*n*CK	

Table 518: 3DS DDR5 3200-4000: Command and Address Timing (Continued)

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum WRITE to WRITE command delay for different bank group in same logical rank	^{t}CCD_S_WR_slr	8	-	8	-	8	-	*n*CK	
Minimum READ to WRITE command delay for different bank group in same logical rank	^{t}CCD_S_RTW_slr	CL - CWL + RBL/2 + 2^{t}CK - (READ DQS offset) + (^{t}RPST - 0.5^{t}CK) + ^{t}WPRE						*n*CK, ns	24,31,36
Minimum WRITE to READ command delay for different bank group in same logical rank	^{t}CCD_S_WTR_slr	CWL + WBL/2 + max(4nCK,2.5ns)						*n*CK, ns	24,32
WRITE to READ with AUTO PRECHARGE command for same bank in same logic rank	^{t}CCD_WTRA_slr	CWL + WBL/2 + ^{t}WR_slr - ^{t}RTP_slr						*n*CK, ns	24,32,35
ACTIVATE to ACTIVATE command delay to same bank group in same logical rank	^{t}RRD_L_slr (1K)	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	*n*CK, ns	
ACTIVATE to ACTIVATE command delay to different bank group in same logical rank	^{t}RRD_S_slr (1K)	8	-	8	-	8	-	*n*CK	
Four activate window to same logical rank	^{t}FAW_slr (1K)	max(32*n*CK, 20.000ns)	-	max(32*n*CK, 17.777ns)	-	max(32*n*CK, 16.000ns)	-	*n*CK, ns	41
READ to PRECHARGE command delay in same logical rank	^{t}RTP_slr	max(12*n*CK, 7ns)	-	max(12*n*CK, 7.5ns)	-	max(12*n*CK, 7.5ns)	-	*n*CK, ns	
PRECHARGE to PRECHARGEdelay in same logical rank	^{t}PPD_slr	2	-	2	-	2	-	*n*CK, ns	37
WRITE recovery time in same logical rank	^{t}WR_slr	30	-	30	-	30	-	ns	
Minimum READ to READ command delay in different logical ranks	^{t}CCD_dlr	max(8*n*CK, 5.000ns)	-	max(8*n*CK, 4.444ns)	-	max(8*n*CK, 4.000ns)	-	*n*CK, ns	

Table 518: 3DS DDR5 3200-4000: Command and Address Timing (Continued)

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum WRITE to WRITE command delay in different logical ranks	^{t}CCD_WR_dlr	max(8*n*CK, 5.000ns)	-	max(8*n*CK, 4.444ns)	-	max(8*n*CK, 4.000ns)	-	*n*CK, ns	44
Minimum READ to WRITE command delay for different logical ranks	^{t}CCD_RTW_dlr	CL - CWL + RBL/2 + 2^{t}CK - (READ DQS offset) + (^{t}RPST - 0.5^{t}CK) + ^{t}WPRE						*n*CK, ns	24,31, 36
Minimum WRITE to READ command delay for different logical ranks	^{t}CCD_WTR_dlr	CWL + WBL/2 + max(4nCK,2.5ns)						*n*CK, ns	24,32
ACTIVATE to ACTIVATE command delay to different logical ranks	^{t}RRD_dlr	max(4nCK, 2.500ns)	-	max(4nCK, 2.222ns)	-	max(4nCK, 2.000ns)	-	*n*CK, ns	
Four activate window to different logical ranks	^{t}FAW_dlr	max(16nCK, 10.000ns)	-	max(16nCK, 8.888ns)	-	max(16nCK, 8.000ns)	-	*n*CK, ns	
PRECHARGE to PRECHARGE delay in same logic rank									
Minimum WRITE to WRITE command delay in different physical ranks	^{t}CCD_WR_dpr	8	-	8	-	8	-	*n*CK	44,45
Activate window by DIMM channel	^{t}DCAW	128	-	128	-	128	-	*n*CK	42,43, 45,46
DIMM CHANNEL ACTIVATE command count in ^{t}DCAW	^{n}DCAC	-	32	-	32	-	32	ACT	42,43, 45,46

Table 519: 3DS DDR5 3200-4000: Self-Refresh Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Exit Self-Refresh to next valid command not requiring a DLL in same logic layer	^{t}XS_slr	^{t}RFC1_slr +10ns	-	^{t}RFC1_slr +10ns	-	^{t}RFC1_slr +10ns	-	ns	39,40, 41
Exit Self-Refresh to next valid command not requiring a DLL in different logic layer	^{t}XS_dlr	^{t}RFC1_slr +10ns	-	^{t}RFC1_slr +10ns	-	^{t}RFC1_slr +10ns	-	ns	39,40, 41

Timing Parameters for 2H and 4H 3DS DDR5 4400-5200

The analog timing parameters in this section have been defined based on nominal ^{t}CK(avg)min according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

Table 520: 3DS DDR5 4400-5200: Clock Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Average clock period	^{t}CK,AVG	0.454	-	0.416	-	0.384	-	ns	23

Table 521: 3DS DDR5 4400-5200: Command and Address Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum READ to READ command delay for same bank group in same logical rank	^{t}CCD_L_slr	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	*n*CK, ns	
Minimum WRITE to WRITE command delay for same bank group in same logical rank	^{t}CCD_L_WR_slr	max(32*n*CK, 20ns)	-	max(32*n*CK, 20ns)	-	max(32*n*CK, 20ns)	-	*n*CK, ns	
Minimum WRITE to WRITE command delay for same bank group, second WRITE not RMW, same logical rank	^{t}CCD_L_WR2_slr	16*n*CK,10ns (MAX)	-	16*n*CK,10ns (MAX)	-	16*n*CK,10ns (MAX)	-	*n*CK, ns	
Minimum READ to WRITE command delay for same bank group in same logical rank	^{t}CCD_L_RTW_slr	CL - CWL + RBL/2 + 2^{t}CK - (READ DQS offset) + (^{t}RPST - 0.5^{t}CK) + ^{t}WPRE						*n*CK, ns	24,31, 36
Minimum WRITE to READ command delay for same bank group in same logical rank	^{t}CCD_L_WTR_slr	CWL + WBL/2 + max(16nCK,10ns)						*n*CK, ns	24,32
Minimum READ to READ command delay for different bank group in same logical rank	^{t}CCD_S_slr	8	-	8	-	8	-	*n*CK	
Minimum WRITE to WRITE command delay for different bank group in same logical rank	^{t}CCD_S_WR_slr	8	-	8	-	8	-	*n*CK	
Minimum READ to WRITE command delay for different bank group in same logical rank	^{t}CCD_S_RTW_slr	CL - CWL + RBL/2 + 2^{t}CK - (READ DQS offset) + (^{t}RPST - 0.5^{t}CK) + ^{t}WPRE						*n*CK, ns	24,31, 36

Table 521: 3DS DDR5 4400-5200: Command and Address Timing (Continued)

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum WRITE to READ command delay for different bank group in same logical rank	^{t}CCD_S_WTR_slr	CWL + WBL/2 + max(4nCK,2.5ns)						*n*CK, ns	24,32
WRITE to READ with AUTO PRECHARGE command for same bank in same logic rank	^{t}CCD_WTRA_slr	CWL + WBL/2 + ^{t}WR_slr - ^{t}RTP_slr						*n*CK, ns	24,32, 35
ACTIVATE to ACTIVATE command delay to same bank group in same logical rank	^{t}RRD_L_slr (1K)	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	*n*CK, ns	
ACTIVATE to ACTIVATE command delay to different bank group in same logical rank	^{t}RRD_S_slr (1K)	8	-	8	-	8	-	*n*CK	
Four activate window to same logical rank	^{t}FAW_slr (1K)	max(32*n*CK, 14.545ns)	-	max(32*n*CK,13.333ns)	-	max(32*n*CK, 12.308ns)	-	*n*CK, ns	
READ to PRECHARGE command delay in same logical rank	^{t}RTP_slr	max(12*n*CK, 7.5ns)	-	max(12*n*CK,7.5ns)	-	max(12*n*CK, 7.5ns)	-	*n*CK, ns	
PRECHARGE to PRECHARGE delay in same logical rank	^{t}RTP_slr	2	-	2	-	2	-	*n*CK	37
WRITE recovery time in same logical rank	^{t}WR_slr	30	-	30	-	30	-	ns	
Minimum READ to READ command delay in different logical ranks	^{t}CCD_dlr	max(8*n*CK, 3.636ns)	-	max(8*n*CK, 3.333ns)	-	max(8*n*CK, 3.333ns)	-	*n*CK, ns	
Minimum WRITE to WRITE command delay in different logical ranks	^{t}CCD_WR_dlr	max(8*n*CK, 3.636ns)	-	max(8*n*CK, 3.333ns)	-	max(8*n*CK, 3.333ns)	-	*n*CK, ns	44
Minimum READ to WRITE command delay for different logical ranks	^{t}CCD_RTW_dlr	CL - CWL + RBL/2 + 2^{t}CK - (READ DQS offset) + (^{t}RPST - 0.5^{t}CK) + ^{t}WPRE						*n*CK, ns	24,31, 36
Minimum WRITE to READ command delay for different logical ranks	^{t}CCD_WTR_dlr	CWL + WBL/2 + max(4nCK,2.5ns)						*n*CK, ns	24,32
ACTIVATE to ACTIVATE command delay in different logical ranks	^{t}RRD_dlr	max(4*n*CK, 1.818ns)	-	max(4*n*CK, 1.666ns)	-	max(4*n*CK, 1.666ns)	-	*n*CK, ns	
Four activate window to different logical ranks	^{t}FAW_dlr	max(16*n*CK, 7.272ns)	-	max(16*n*CK,6.666ns)	-	max(16*n*CK, 6.666ns)	-	*n*CK, ns	
PRECHARGE to PRECHARGE delay in same logic rank	^{t}PPD_dlr	2	-	2	-	2	-	*n*CK	37

Table 521: 3DS DDR5 4400-5200: Command and Address Timing (Continued)

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum WRITE to WRITE command delay in different physical ranks	^{t}CCD_S_WR_dpr	8	-	8	-	8	-	*n*CK	44,45
Activate window by DIMM channel	^{t}DCAW	128	-	128	-	128		*n*CK	42,43, 45,46
DIMM CHANNEL ACTIVATE command count in ^{t}DCAW	^{n}DCAC	-	32	-	32	-	32	ACT	42,43, 45,46

Table 522: 3DS DDR5 4400-5200: Self-Refresh Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Exit Self-Refresh to next valid command not requiring a DLL in same logic layer	^{t}XS_slr	^{t}RFC1_slr +10ns	-	^{t}RFC1_slr +10ns	-	^{t}RFC1_slr +10ns	-	ns	39,40,41
Exit Self-Refresh to next valid command not requiring a DLL in different logic layer	^{t}XS_dlr	^{t}RFC1_slr +10ns	-	^{t}RFC1_slr +10ns	-	^{t}RFC1_slr +10ns	-	ns	39,40, 41

Timing Parameters for 2H and 4H 3DS DDR5 5600-6400

The analog timing parameters in this section have been defined based on nominal ^{t}CK(avg)min according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

Table 523: 3DS DDR5 5600-6400: Clock Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Average clock period	^{t}CK,AVG	0.357	-0.384	0.333	-0.357	0.312	-0.333	ns	13

Table 524: 3DS DDR5 5600-6400: Command and Address Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum READ to READ command delay for same bank group in same logical rank	^{t}CCD_L_slr	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	*n*CK, ns	
Minimum WRITE to WRITE command delay for same bank group in same logical rank	^{t}CCD_L_WR_slr	max(32*n*CK, 20ns)		max(32*n*CK, 20ns)		max(32*n*CK,20ns)		*n*CK, ns	

Table 524: 3DS DDR5 5600-6400: Command and Address Timing (Continued)

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum WRITE to WRITE command delay for same bank group, second WRITE not RMW, same logical rank	^{t}CCD_L_WR2_slr	max(16*n*CK, 10ns)		max(16*n*CK, 10ns)		max(16*n*CK,10ns)		*n*CK, ns	
Minimum READ to WRITE command delay for same bank group in same logical rank	^{t}CCD_L_RTW_slr	CL - CWL + RBL/2 + 2^{t}CK - (Read DQS offset) + (^{t}RPST - 0.5^{t}CK) + ^{t}WPRE						*n*CK, ns	24,31, 36
Minimum WRITE to READ command delay for same bank group in same logical rank	^{t}CCD_L_WTR_slr	CWL + WBL/2 + max(16nCK,10ns)						*n*CK, ns	24,32
Minimum READ to READ command delay for different bank group in same logical rank	^{t}CCD_S_slr	8	-	8	-	8	-	*n*CK	
Minimum WRITE to WRITE command delay for different bank group in same logical rank	^{t}CCD_S_WR_slr	8	-	8	-	8	-	*n*CK	
Minimum READ to WRITE command delay for different bank group in same logical rank	^{t}CCD_S_RTW_slr	CL - CWL + RBL/2 + 2^{t}CK - (Read DQS offset) + (^{t}RPST - 0.5^{t}CK) + ^{t}WPRE						*n*CK, ns	24,31, 36
Minimum WRITE to READ command delay for different bank group in same logical rank	^{t}CCD_S_WTR_slr	CWL + WBL/2 + max(4nCK,2.5ns)						*n*CK, ns	24,32
WRITE to READ with AUTO PRECHARGE command for same bank in same logic rank	tCCD_WTRA_slr	CWL + WBL/2 + ^{t}WR_slr - ^{t}RTP_slr						*n*CK, ns	24,32, 35
ACTIVATE to ACTIVATE command delay to same bank group in same logical rank	^{t}RRD_L_slr (1K)	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	max(8*n*CK, 5ns)	-	*n*CK, ns	
ACTIVATE to ACTIVATE command delay to different bank group in same logical rank	^{t}RRD_S_slr (1K)	8	-	8	-	TBD	-	*n*CK	

Table 524: 3DS DDR5 5600-6400: Command and Address Timing (Continued)

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Four activate window to same logical rank	^{t}FAW_slr (1K)	max(32*n*CK, 11.428ns)	-	32*n*CK, 10.666ns (MAX)	-	max(32*n*CK, 10.000ns)	-	*n*CK, ns	41
READ to PRECHARGE command delay in same logical rank	^{t}RTP_slr	max(12*n*CK, 7.5ns)	-	max(12*n*CK, 7.5ns)	-	max(12*n*CK, 7.5ns)	-	*n*CK, ns	
PRECHARGE to PRE-CHARGE delay in same logical rank	^{t}PPD_slr	2	-	2	-	2	-	*n*CK	37
WRITE recovery time in same logical rank	^{t}WR_slr	30	-	30	-	30	-	ns	
Minimum READ to READ command delay in different logical ranks	^{t}CCD_dlr	max(8*n*CK, 3.214ns)	-	max(8*n*CK, 3.214ns)	-	max(8*n*CK, 3.215ns)	-	*n*CK, ns	
Minimum WRITE to WRITE command delay in different logical ranks	^{t}CCD_S_WR_dlr	max(8*n*CK, 3.214ns)	-	max(8*n*CK, 3.214ns)	-	max(8*n*CK, 3.215ns)	-	*n*CK, ns	44
Minimum READ to WRITE command delay for different logical ranks	^{t}CDD_RTW_dlr	CL - CWL + RBL/2 + 2^{t}CK - (Read DQS offset) + (^{t}RPST - 0.5^{t}CK) + ^{t}WPRE						*n*CK, ns	24,31, 36
Minimum WRITE to READ command delay for different logical ranks	^{t}CCD_WTR_dlr	CWL + WBL/2 + max(4nCK,2.5ns)						*n*CK, ns	24,32
ACTIVATE to ACTI-VATE command delay in different logical ranks	^{t}RRD_dlr	max(4*n*CK, 1.666ns)	-	max(4*n*CK, 1.666ns)	-	max(4*n*CK, 1.666ns)	-	*n*CK, ns	
Four activate window to different logical ranks	^{t}FAW_dlr	max(16*n*CK, 6.666ns)	-	max(16*n*CK, 6.666ns)	-	max(16*n*CK, 6.666ns)	-	*n*CK, ns	
Minimum WRITE to WRITE command delay in different physical ranks	^{t}PPD_dlr	2	-	2	-	2	-	*n*CK	37
Activate window by DIMM channel	^{t}DCAW	128	-	128	-	128		*n*CK	42,43, 45,46
DIMM channel ACTI-VATE command count in ^{t}DCAW	^{n}DCAC	-	32	-	32	-	32	ACT	42,43, 45,46

Table 525: 3DS DDR5 5600-6400: Self-Refresh Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Exit Self-Refresh to next valid command not requiring DLL in same logic layer	^{t}XS_slr	^{t}RFC1_slr + 10ns	-	^{t}RFC1_slr + 10ns	-	^{t}RFC1_slr + 10ns	-	ns	39,40,41
Exit Self-Refresh to next valid command not requiring DLL in different logic layer	^{t}XS_dlr	^{t}RFC1_slr + 10ns	-	^{t}RFC1_slr + 10ns	-	^{t}RFC1_slr + 10ns	-	ns	39,40,41

Timing Parameters for 2H and 4H 3DS DDR5 6800-7600

The analog timing parameters in this section have been defined based on nominal ^{t}CK(avg)min according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

Table 526: 3DS DDR5 6800-7600: Clock Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Average clock period	^{t}CK,AVG	TBD	-	TBD	–	TBD	–	ns	23

Table 527: 3DS DDR5 6800-7600: Command and Address Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum READ to READ command delay for same bank group in same logical rank	^{t}CCD_L_sir	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK, ns	
Minimum WRITE to WRITE command delay for same bank group in same logical rank	^{t}CCD_L_WR_slr	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK, ns	
Minimum WRITE to WRITE command delay for same bank group, second WRITE not RMW, same logical rank	^{t}CCD_L_WR2_slr	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK	
Minimum READ to WRITE command delay for same bank group in same logical rank	^{t}CCD_L_RTW_slr	TBD						*n*CK, ns	TBD
Minimum WRITE to READ command delay for same bank group in same logical rank	^{t}CCD_L_WTR_slr	TBD						*n*CK, ns	TBD

Table 527: 3DS DDR5 6800-7600: Command and Address Timing (Continued)

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum READ to READ command delay for different bank group in same logical rank	^{t}CCD_S_slr	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK	
Minimum WRITE to WRITE command delay for different bank group in same logical rank	^{t}CCD_S_WR_slr	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK	
Minimum READ to WRITE command delay for different bank group in same logical rank	^{t}CCD_S_RTW_slr	TBD						*nCK*, *ns*CK	TBD
Minimum WRITE to READ command delay for different bank group in same logical rank	^{t}CCD_S_WTR_slr	TBD						*nCK*, *ns*CK	TBD
WRITE to READ with AUTO PRECHARGE command for same bank in same logic rank	^{t}CCD_WTRA_slr	TBD						*n*CK, ns	TBD
ACTIVATE to ACTIVATE command delay to same bank group in same logical rank	^{t}RRD_L_slr(1K)	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK, ns	
ACTIVATE to ACTIVATE command delay to different bank group in same logical rank	^{t}RRD_S_slr(1K)	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK	
Four activate window to same logical rank	^{t}FAW_slr (1K)	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK, ns	
READ command to PRECHARGE command delay in same logical rank	^{t}RTP_slr	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK, ns	
PRECHARGE to PRECHARGE delay in same logical rank	^{t}PPD_slr	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK	TBD
WRITE recovery time in same logical rank	^{t}WR_slr	TBD	TBD	TBD	TBD	TBD	TBD	ns	
Minimum READ to READ command delay in different logical ranks	^{t}CCD_dlr	TBD	TBD	TBD	TBD	TBD	TBD		

Table 527: 3DS DDR5 6800-7600: Command and Address Timing (Continued)

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum WRITE to WRITE command delay in different logical ranks	^{t}CCD_WR_dlr	TBD	TBD	TBD	TBD	TBD	TBD		
Minimum READ to WRITE command delay for different logical ranks	^{t}CCD_RTW_dlr	TBD							
Minimum WRITE to READ command delay for different logical ranks	^{t}CCD_WTR_dlr	TBD							
ACTIVATE to ACTIVATE command delay to different logical ranks	^{t}RRD_dlr	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK, ns	
Four activate window to different logical ranks	^{t}FAW_dlr	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK, ns	
PRECHARGE to PRECHARGE delay in same logic rank	^{t}PPD_dlr	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK	
Minimum WRITE to WRITE command delay in different physical ranks	^{t}CCD_S_WR_dpr	TBD	TBD	TBD	TBD	TBD	TBD		
Activate window by DIMM channel	^{t}DCAW	TBD	TBD	TBD	TBD	TBD	TBD		
DIMM channel ACTIVE command count in ^{t}DCAW	^{n}DCAW	TBD	TBD	TBD	TBD	TBD	TBD		

Table 528: 3DS DDR5 6800-7600: Self Refresh Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Exit self refresh to next valid command not requiring a DLL in same logic layer	^{t}XS_slr	TBD	-	TBD	-	TBD	-	*n*CK	
Exit self refresh to next valid command not requiring a DLL in different logic layer	^{t}XS_dlr	TBD	-	TBD	-	TBD	-	ns	

Timing Parameters for 2H and 4H 3DS DDR5 8000-8800

The analog timing parameters in this section have been defined based on nominal ^{t}CK(avg)min according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

Table 529: 3DS DDR5 8000-8800: Clock Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Average clock period	^{t}CK,AVG	TBD	-	TBD	–	TBD	–	ns	23

Table 530: 3DS DDR5 8000-8800: Command and Address Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum READ to READ command delay for same bank group in same logical rank	^{t}CCD_L_sir	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK, ns	
Minimum WRITE to WRITE command delay for same bank group in same logical rank	^{t}CCD_L_WR_slr	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK, ns	
Minimum WRITE to WRITE command delay for same bank group, second WRITE not RMW, same logical rank	^{t}CCD_L_WR2_slr	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK	
Minimum READ to WRITE command delay for same bank group in same logical rank	^{t}CCD_L_RTW_slr	TBD						*n*CK, ns	TBD
Minimum WRITE to READ command delay for same bank group in same logical rank	^{t}CCD_L_WTR_slr	TBD						*n*CK, ns	TBD
Minimum READ to READ command delay for different bank group in same logical rank	^{t}CCD_S_slr	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK	
Minimum WRITE to WRITE command delay for different bank group in same logical rank	^{t}CCD_S_WR_slr	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK	
Minimum READ to WRITE command delay for different bank group in same logical rank	^{t}CCD_S_RTW_slr	TBD						*nCK, ns*CK	TBD

Table 530: 3DS DDR5 8000-8800: Command and Address Timing (Continued)

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum WRITE to READ command delay for different bank group in same logical rank	^{t}CCD_S_WTR_slr	TBD						*n*CK, *ns*CK	TBD
WRITE to READ with AUTO PRECHARGE command for same bank in same logic rank	^{t}CCD_WTRA_slr	TBD						*n*CK, ns	TBD
ACTIVATE to ACTIVATE command delay to same bank group in same logical rank	^{t}RRD_L_slr(1K)	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK, ns	
ACTIVATE to ACTIVATE command delay to different bank group in same logical rank	^{t}RRD_S_slr(1K)	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK	
Four activate window to same logical rank	^{t}FAW_slr (1K)	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK, ns	
READ command to PRECHARGE command delay in same logical rank	^{t}RTP_slr	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK, ns	
PRECHARGE to PRECHARGE delay in same logical rank	^{t}PPD_slr	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK	TBD
WRITE recovery time in same logical rank	^{t}WR_slr	TBD	TBD	TBD	TBD	TBD	TBD	ns	
Minimum READ to READ command delay in different logical ranks	^{t}CCD_dlr	TBD	TBD	TBD	TBD	TBD	TBD		
Minimum WRITE to WRITE command delay in different logical ranks	^{t}CCD_WR_dlr	TBD	TBD	TBD	TBD	TBD	TBD		
Minimum READ to WRITE command delay for different logical ranks	^{t}CCD_RTW_dlr	TBD							
Minimum WRITE to READ command delay for different logical ranks	^{t}CCD_WTR_dlr	TBD							
ACTIVATE to ACTIVATE command delay to different logical ranks	^{t}RRD_dlr	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK, ns	

Table 530: 3DS DDR5 8000-8800: Command and Address Timing (Continued)

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Four activate window to different logical ranks	^{t}FAW_dlr	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK, ns	
PRECHARGE to PRECHARGE delay in same logic rank	^{t}PPD_dlr	TBD	TBD	TBD	TBD	TBD	TBD	*n*CK	
Minimum WRITE to WRITE command delay in different physical ranks	^{t}CCD_S_WR_dpr	TBD	TBD	TBD	TBD	TBD	TBD		
Activate window by DIMM channel	^{t}DCAW	TBD	TBD	TBD	TBD	TBD	TBD		
DIMM channel ACTIVE command count in ^{t}DCAW	^{n}DCAW	TBD	TBD	TBD	TBD	TBD	TBD		

Table 531: 3DS DDR5 8000-8800: Self Refresh Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Exit self refresh to next valid command not requiring a DLL in same logic layer	^{t}XS_slr	TBD	-	TBD	-	TBD	-	*n*CK	
Exit self refresh to next valid command not requiring a DLL in different logic layer	^{t}XS_dlr	TBD	-	TBD	-	TBD	-	ns	

Notes: 1. Start of internal write transaction is defined as:
- For BL16 (fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after CWL.
- For BC8 (on-the-fly): Rising clock edge 4 clock cycles after CWL.

2. MRR and MRW commands are not allowed with pages open.
3. This parameter applies only to MRWs to DFE registers and is defined as the settling time before a new DFE setting is active.
4. The range of ^{t}PDA_DQS_DELAY specifies the full range of when the minimum of 16 strobe edges can be sent by the host controller.
5. Measured relative to the write leveling feedback, after write leveling training has completed.
6. Includes min DQS and CK timing terms TBD.
7. Measured over full VDD and temperature spec ranges.
8. Measured for a given DRAM part, and for each DQS_t/DQS_c pair in case of x16 (part variation is excluded).
9. These parameters are verified by design and characterization, and may not be subject to production test.
10. Assume no jitter on input clock signals to the device.
11. This applies only to multicycle VREFCS/VREFCA commands when MR2:OP[4]=0b.
12. While in 2N mode, ^{t}CSL_SRexit is not statically held LOW, as it will pulse for each 2-cycle period for a min of 6 nCK. Refer to the 2N mode section for more details.
13. Since frequency can require VREFCA and CA/CK/CS ODT changes, the min time is longer than the traditional ^{t}CSL when the SRE command with CA9=L is used.

14. POWER DOWN command can be sent while operations such as row activation, precharge, auto-precharge or refresh are in progress; however, IDD spec is not applied until the operations are finished.
15. ^{t}WR is defined in ns, for calculation of tWRPDEN it is necessary to round up ^{t}WR/^{t}CK.
16. WR in clock cycles as programmed in MR6.
17. Refer to Read Timing Definition.
18. There is no max limit for ^{t}WL_Pulse_Width; however, the Write Leveling Internal Pulse must begin at zero for each WRITE command.
19. Multiple cycles are used to avoid possible metastability of CS_n.
20. At the end of CSTM, it is assumed the host should be able to place the CS_n appropriately and the VREFCA command could be issued as a single-cycle command.
21. The minimum ^{t}MPC_CS constraint only applies when the CS assertion duration setting is 0. The CS assertion duration MR setting must be set to enable single-cycle MPC commands. The earliest time to set the CS assertion duration MR is after CA training is complete, when MRW commands can be sent to the device.
22. This applies only to multicycle MPC commands when MR2:OP[2]=0b.
23. ^{t}CK(AVG),MIN listed for reference only, refer to the Speed Bins and Operations section which lists all valid ^{t}CK(avg) values.
24. CWL=CL-2.
25. In manual stop mode, DQS OSC START command should be followed by the DQS OSC STOP command (MPC). Otherwise, DQS OSC result value (MR46 and 47) cannot be guaranteed.
26. RD/WR/MRR can refer to both target command and non-target command when CA11=HIGH during PDE command.
27. ^{t}MPC_delay is a valid timing parameter for all MPC commands except:
    - Enter CS Training mode, Enter CA Training mode, PDA Enumerate ID, Enter PDA Enumerate Program mode because POWER DOWN ENTRY is not supported for these MPC commands.
    - APPLY VREFCA, VREFCS and RTT_CA/CS/CK because this MPC command requires waiting for VREFCA_time/VREFCS_time.
28. When measuring the ^{t}DQSoffset, ^{t}WLS and ^{t}WLH are reflected in the ^{t}DQSoffset value.
29. This timing parameter is applied to each DQ independently, not all-DQs valid window perspective.
30. Refresh to refresh max time interval limits ^{t}PD(MAX) to 5X ^{t}REFI1 if in normal refresh mode and 9X ^{t}REFI2 if in FGR mode.
31. RBL: Read burst length associated with READ command:
    - RBL = 32 (36 with RCRC on) for fixed 32 and BL32 in BL32 OTF mode
    - RBL = 16 (18 with RCRC on) for fixed 16 and BL16 in BL32 OTF mode
    - RBL = 16 (18 with RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
32. WBL: Write burst length associated with Write command:
    - WBL = 32 (36 w/ WCRC on) for fixed 32 and BL32 in BL32 OTF mode
    - WBL = 16 (18 w/ WCRC on) for fixed 16 and BL16 in BL32 OTF mode
    - WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
33. DDR5-3200 timings apply for data rates <2933 MT/s. For example, at 2000 MT/s, ^{t}DQSS(max) = (2000/2933)*0.25*^{t}WPRE_EN_ntck(min) = 0.17*^{t}WPRE_EN_ntck(min).
34. Measured at a fixed and constant VDD and temperature condition.
35. ^{t}CCD_WRTA(min) is always be greater than or equal to CWL + WBL/2 + ^{t}WR(min) - ^{t}RTP(min). When using the appropriate rounding algorithms, ^{n}CCD_WTRA(min) is always be greater than or equal to CWL + WBL/2 + ^{n}WR(min) - ^{n}RTP(min).
36. The following is considered for ^{t}RTW equation:
    - 1 ^{t}CK needs to be added due to ^{t}DQS2CK
    - Read DQS offset timing can pull in the ^{t}RTW timing
    - 1 ^{t}CK needs to be added when 1.5 ^{t}CK postamble

37. ^{t}PPD applies to any combination of PRECHARGE commands (PREab, PREsb, PREpb). ^{t}PPD also applies to any combination of PRECHARGE commands to a different die in a 3DS device.
38. For x4 devices only. x8 device timings are TBD.
39. Upon exit from self-refresh, the 3DS device requires a minimum of one extra REFRESH command to all logical ranks before it is put back into self-refresh mode.
40. This parameter utilizes a value that varies based on density. Refer to the 3DS Refresh section for more information.
41. The timings contained in this table are for x4 2H and 4H 3DS devices.
42. ACTIVATE commands to different channels on the same DIMM may be issued on the same cycle, not requiring any stagger.
43. ACTIVATE commands to the same channel on a DIMM are subject to ^{t}DCAW. No more than ^{n}DCAC ACTIVATE commands may be issued to the same channel on a DIMM within ^{t}DCAW
44. ^{t}CCD_ WR_dlr and ^{t}CCD_ WR_dpr also apply to the WRITE PATTERN command.
45. Parameter applies to dual physical rank (36 and 40 placement) 3DS-based DIMMs built with JEDEC PMICXXXX, but may not apply to DIMMs built with higher current capacity PMICs.
46. ACTIVATE commands to a DIMM channel include all ACTIVATE commands to the same logical rank (SLR), all ACTIVATE commands to different logical ranks (DLR), and all ACTIVATE commands to different physical ranks (DPR).

Rounding Definition and Algorithm

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 2200 MHz (4400 MT/s) for the DDR5-4400 speed bin, which mathematically yields a clock period of 0.454545... ns). In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be used. The device specification establishes a minimum granularity for timing parameters of 1ps.

Rules for rounding must be defined to allow optimization of device performance without violating device parameters. All timing parameters specified in the time domain (ns, ps, etc.) which must then be converted to the clock domain (nCK units)are defined to align with these rules. The key point is, the minimum timing parameters generally use the same rounding rules used to define ^{t}CK(AVG)min. The resulting rounding algorithms rely on results that are within correction factors of device testing and specification to avoid losing performance due to rounding errors. The rules are:

- Minimum timing parameter values, including ^{t}CK (AVG)min, are to be rounded down and defined to 1ps of accuracy in the specification based on the non-rounded nominal ^{t}CK (AVG)min for a given speed bin. If the nominal minimum timing parameter values require more than 1ps of accuracy, they can be rounded down (faster) to the next 1ps according to the rounding algorithms. The device is responsible for absorbing this small minimum parameter extension. In other words, the device specification only lists the nominal minimum parameters values rounded down to the next 1ps. For example, this extends the DDR5-4400 ^{t}CK (AVG)min definition to be exactly 0.454ns, which is slightly smaller (faster) than the nominal memory clock period of 0.454545...ns by less than 1ps.
- For minimum timing parameters (other than ^{t}CK (AVG)min) to avoid losing performance due to additional erroneous nCKs, and to calculate the true real minimum values, their nominal values listed in this specification must be reduced (faster) by the same or greater percentage reduction (correction factor) that was used to define ^{t}CK (AVG)min. The device is responsible for absorbing these parameter extensions. For example, ^{t}WR MIN has a nominal value of 30.000ns; however, applying the 0.30% correction factor enables a more aggressive timing (for example, 29.910ns) to be supported, which allows the intended smaller (faster) nCK value to be maintained when rounding ^{t}CK (AVG)min down to the next 1ps. Note, parameter values defined to be 0ps do not need to be reduced by a correction factor, and therefore, do not require these rounding algorithms.
- Using real number math, nominal minimum parameters like ^{t}WRmin, ^{t}RCDmin, etc. — which are programmed in systems in numbers of clock (nCK) but expressed in units of time — are divided by the real application memory clock period (tCK (AVG)real), yielding a ratio of clock units (nCK), which is reduced by a correction factor of 0.30% (multiply by 99.70%), then the result is rounded up to the next integer number of clocks:

$$nCK = ceiling\left[\frac{parameter\_nominal \times 0.997}{tCK(AVG)\ real}\right]$$

- Round-down only integer number math is commonly used in the industry to calculate nCK values. This second algorithm uses scaling by 1000 to allow use of integer math. With this algorithm, the nominal minimum parameters (in ps) is multiplied by the scaled correction factor (1000-3=997) prior to division by the application memory clock period, and 1 scaled by 1000 added to that result effectively rounds the result up. Division by 1000 undos the scaling effects, resulting in a simple integer number of clocks as the final answer. The caveat is, effectively adding 1 prior to rounding down is mostly equivalent to rounding up, except when the result is equal to an integer (whole number), in which case the result won't be rounded down as intended, and therefore, performance would be lost. To address this, the largest correction factor of 0.28% needed for 3600 MHz (7200

MT/s) operation has been increased slightly to 0.30% in these rounding algorithms. This accounts for all boundary conditions except for the specific case when the nominal minimum timing parameter value is defined to be 0ps. This round-down only integer number math algorithm is not required and not optimized for 0ps parameter values, and will result in lost performance if used for 0ps parameter values.

$$nCK = truncate\left[\frac{\left(\frac{truncate[parameter\_in\_ps] \times 997}{truncate[tCK(AVG)real\_in\_ps}\right) + 1000}{1000}\right]$$

- Both the real number math rounding algorithm and the rounded down only integer number math rounding algorithm yields similar results. In case of conflicting results, the round-down only integer number math algorithm prevails.
- The real number math and round down only integer number math rounding algorithms are to be used for all minimum timing parameters when converting from the time domain (ns, ps, etc.) to the clock domain (nCK units), except for when converting ^{t}AA to CL. If these rounding algorithms are used to convert ^{t}AA to CL, they will return invalid CLs for some cases when down clocking (the DIMM SPD CL mask does not protect against all of these cases). The proper setting of CL is determined by the memory controller, either by using the speed bin tables or the CL algorithm, or by some other means. Refer to the Speed Bins and Operations section for more information. Note, the CL algorithm replaces the need to use the DIMM SPD CL Mask.
- If the device supports non-standard ^{t}CK, ^{t}AA, ^{t}RCD, and ^{t}RP speed bin timings, the CL algorithm will still only return valid CLs as defined in the speed bin tables, which may not be the intended CLs for non-standard speed bins. In these cases, the rounding algorithms may need to be used to convert ^{t}AA to CL, instead of the CL algorithm. The CL returned by the rounding algorithms is incremented up to the next supported CL according to the DIMM SPD CL mask. Consult the memory vendor for more information

.

Example 1: Using Real Number Math to Convert ^{t}WR(MIN) from ns to nCK

```
// This algorithm reduces the nominal minimum timing parameter value by a 0.30%
// correction factor, and rounds nCK up to the next integer value


real TwrMin, Correction, ClockPeriod, TempTwr, TempNck
int TwrInNck;

TwrMin = 30.000;                          // tWRmin in ns
Correction = 0.003                        // 0.30% per the rounding algorithm
ClockPeriod = ApplicationTck;             // Clock period in ns is application-specific
TempTwr = TwrMin * (1 - Correction);      // Apply correction factor
TempNck = TempTwr / ClockPeriod;          // Initial nCK calculation
TwrInNck = (int) ceiling(TempNck);        // Round up to next integer value
```

Table 532: Example 1: Using Real Number Math

DDR5 Device Operating at Standard Application Frequencies Timing Parameter: ^{t}WR(min) = 30.00ns					
Application Speed Grade	Device ^{t}WR	Application ^{t}CK	Device ^{t}WR / Application ^{t}CK	Device (^{t}WR * 1 - Correction) / Application ^{t}CK	Ceiling Result
	ns	ns	Ratio (Real)	Ration (Real)	nCK (Integer)
3200	30.000	0.625	48.00	47.86	48
3600	30.000	0.555	54.05	53.89	54
4000	30.000	0.500	60.00	59.82	60
4400	30.000	0.454	66.08	65.88	66
4800	30.000	0.416	72.12	71.90	72

Example 2: Using Round-Down Only Integer Number Math to Convert ^{t}WR (MIN) from ps to nCK

```
// This algorithm reduces the nominal minimum timing parameter value by a 0.30%
//correction factor, adds 1nCK, and rounds nCK down to the next integer value.
int TwrMin, Correction, ClockPeriod, TempTwr, TempNck, TwrInNck;

TwrMin = 30000;                          // tWRmin in ps
Correction = 3                           // 0.30% per the rounding algorithm
ClockPeriod = ApplicationTck;            // Clock period in ps is application-specific
TempTwr = TwrMin * (1000 - Correction);  // Apply correction factor, scaled by 1000
TempNck = TempTwr / ClockPeriod;         // Initial nCK calculation, scaled by 1000
TempNck = TempNck + 1000;                // Add 1, scaled by 1000, to effectively round up
TwrInNck = (int)(TempNck / 1000);        // Truncate to next lower integer
```

Table 533: Example 2: Using Round-Down Only Integer Number Math

DDR5 Device Operating at Standard Application Frequencies Timing Parameter: ^{t}WR(min) = 30.00ns					
Application Speed Grade	Device ^{t}WR	Application ^{t}CK	Device ^{t}WR / Application ^{t}CK	Device (^{t}WR * 1 - Correction) / Application ^{t}CK	Truncate Corrected nCK / 1000
	ps	ps	nCK (Real)	Scaled nCK (Corrected)	nCK (Integer)
3200	30000	625	48.00	48856	48
3600	30000	555	54.05	54891	54
4000	30000	500	60.00	60820	60
4400	30000	454	66.08	66881	66
4800	30000	416	72.12	72899	72

Revision History

Rev. B – 09/2021

- Updates are to align with JEDEC full draft spec Rev 2.0
- Added MBIST/mPPR section
- Added sPPR undo and lock features
- Updated sPPR and hPPR to only have to drive DQ0-3
- Added Adaptive RFM feature
- Added Directed RFM feature, details still pending in JEDEC
- Moved several items from the DDR5 Core data sheet into the DDR5 Die Revision specific data sheet addendum
  - Features and options page
  - Pinouts and ballouts section
  - pin description section
  - Package mechanical drawings section
- Updates to on-die ECC to cover the bounded fault improvements
- Added features like ECS scan mode to provide flexibility for controllers to better control ECS use cases.
- Added Refresh Interval Rate feature
- Updated Write leveling with the 1/2 step WICA feature to enhance WL training
- Added mode registers to account for authentication serial numbers on DRAMs
- Added MR4 wide refresh rate
- Updated and improved data sheet with many clarifications and editorial corrections.

Rev. A – 06/2020

- Initial release — based on JEDEC full draft specification Rev 1.0

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