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1) Identify the properties for each memory type 10 pts

	R/W	Static/Dynamic	Storage Element	Relative Density 1= high, 5=low
ROM				
SRAM				
SDRAM				
NAND Flash				
NOR Flash				

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2) Using the DDR3 DRAM from the class/notes, provide the latency from Activate to data out in clock cycles and ns assuming 933MHz operation and CL=12 - 10 pts

How long does it take to completely output an 8 beat burst - 10 pts

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3) Briefly explain 20 pts

a) Why is the signal swing on a DRAM bitline so small

b) How is a DRAM cell refreshed (at the bit/cell level)

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4) Calculate the approximate time it would take a 50fF dram capacitor to discharge to 80% of it's programmed value (0.9v) assuming leakage of $40x10^{-15}$A/cell - 5 pts

Assuming a 256Mb array and only 1 bit is refreshed each cycle, how fast would the refresh clock need to run to prevent the programmed value to not drop below 80% - 5 pts

How many bits would need to be refreshed to keep the refresh clock under 50KHz - 5 pts

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5) Memory Architecture 15 pts

a) How many bits are stored in each memory below

16Mb, x4

32Mbx16

b) Assuming a 4Gb, x4 memory with 4 banks, a RAS/CAS addressing structure, and a square array

How many total address pins does this memory need

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6) Search and Think 20 pts

Intel hypes its “OPTANE” memory, provide a short description of how this memory stores its bits and how they are accessed (read/write)