1) Identify the properties for each memory type   10 pts

	R/W	Static/Dynamic	Storage Element	Relative Density 1= high, 5=low
ROM	R	Static	MOSFET	2
SRAM	R/W	Static	Latch	5
SDRAM	R/W	Dynamic	Capacitor	4
NAND Flash	R/W	Static	Floating Gate	1
NOR Flash	R/W	Static	Floating Gate	3

2) Using the DDR3 DRAM from the class/notes, provide the latency from Activate to data out in clock cycles and ns assuming 933MHz operation and CL=12 -   10 pts

TRCD + CL
TRCD = 12 clock cycle   ACTIVATE to internal READ or WRITE delay
CL: Read to DQ – 12 clock cycles

Activate to data out = 24 clock cycles

1 clock cycle = 1.071ns
24 clock cycles = 25.7ns

How long does it take to completely output an 8 beat burst -   10 pts

Unrelated to read clock cycles – only dependent on clock freq/2 (ddr)
1/1866MHz x 8 = 4.29ns

Or 4.29ns + 25.7ns = 29.99ns

3) Briefly explain   20 pts

a) Why is the signal swing on a DRAM bitline so small

The small charge stored on the bit capacitor gets spread
across a larger bitline capacitance during a read → low voltage swing
$Q = CV$,   fixed Q + ↑C → ↓V

b) How is a DRAM cell refreshed (at the bit/cell level)

By reading the cell

Every time the cell is read, the circuit enhances the small voltage
read to full strength – rewriting the original data back to the cell

4) Calculate the approximate time it would take a 50fF dram capacitor to discharge to 80% of it's programmed value (0.9v) assuming leakage of 40×10^{-15}A/cell   -   5 pts

$$I \qquad = \qquad C\ dv/dt$$
$$dt \qquad = \qquad C\ dv\ /\ I$$
$$\qquad = \qquad 50fF \times 0.18v\ /\ 40 \times 10^{-15}A/cell = 225ms$$

Assuming a 256Mb array and only 1 bit is refreshed each cycle, how fast would the refresh clock need to run to prevent the programmed value to not drop below 80% -   5 pts

$$225ms/(2^{28}) = 839ps \quad \rightarrow \quad 1.2GHz$$

$$F_{cycle,} = b_{total}/(n_{cycle} * t_{decay}) = 2^{28}/(1 * 225ms) = 1.2GHz$$

How many bits would need to be refreshed to keep the refresh clock under 50KHz -   5 pts

$$n = b/(t * F) = 2^{28}/(225ms * 50KHz) = 23.860$$

5) Memory Architecture   15 pts

a) How many bits are stored in each memory below

16Mb, x4   16Mb in a by 4 configuration → 16Mb or 16,777,216b

32Mbx16   32Mb by 16 → 512Mb or 536,870,912b

b) Assum[...]ddressing
structure[...]

How man[...]

4Gb total / 4 banks → 1Gb / bank
4b / column → 256M addressable locations

For a square array/bank – 4 rows for every 4b column
→ Row address = 4x column addresses
→ Row address bits = 2 + column address bits

256M location → 28 address bits
--> 13 column address bit, 15 row address bits

15 + 2 for the bank + RAS + CAS → 19 pins

6) Search and Think   20 pts

Intel hypes its "OPTANE" memory, provide a short description of how this memory stores its bits and how they are accessed (read/write)

3D Cross-Point memory
Phase change material sandwiched between 2 orthogonal layers
Write – apply voltage to make material conducting or non-conducting
Read – sense a short or open between orthogonal conductors

3D XPoint™ Technology:
An Innovative, High-Density Design

Cross Point Structure
Perpendicular wires connect submicroscopic columns. An individual memory cell can be addressed by selecting its top and bottom wire.

Stackable
These thin layers of memory can be stacked to further boost density.

Non-Volatile
3D XPoint™ Technology is non-volatile—which means your data doesn't go away when your power goes away—making it a great choice for storage.

Selector
Whereas DRAM requires a transistor at each memory cell—making it big and expensive—the amount of voltage sent to each 3D XPoint™ Technology selector enables its memory cell to be written to or read without requiring a transistor.

High Endurance
Unlike other storage memory technologies, 3D XPoint™ Technology is not significantly impacted by the number of write cycles it can endure, making it more durable.

Memory Cell
Each memory cell can store a single bit of data.