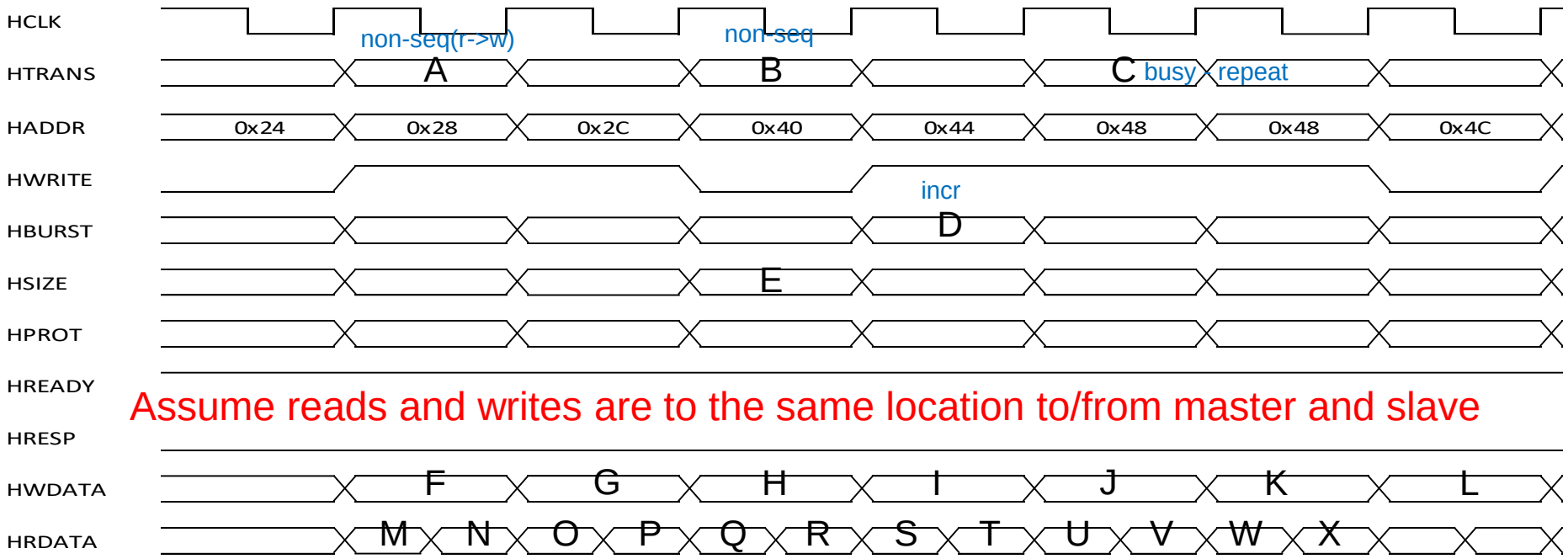
ELE 4142 HW7 Name_____

Below is a trace from an APB bus, fill in the table below (leave unknowns empty) after completion of this trace. 32 bit address and data 15pts

Address	Data: Master (via the bridge)	Data: Slave (peripheral)
0x1234		
0x12AB		0x1111
0x4321		
0xAB12		
0xABCD		0x9876
0xDCBA		0x8732

ELE 4142 HW7 Name_____

Below is a trace from an AHB-Lite bus, fill in the values below (leave unknowns empty) 35 pts



Assume reads and writes are to the same location to/from master and slave

Data - Prior to beginning of trace

Address	Master	Slave
0x24	0x00	0x11
0x28	0x01	0x22
0x2C	0x02	0x33
0x40	0x03	0x44
0x44	0x04	0x55
0x48	0x05	0x66
0x4C	0x06	0x77

	Location	Value (hex)	Location	Value (hex)
	A	0x02	M	memS(24)
	B	0x02	N	0x11
	C	0x01	O	
	D	0x01	P	
	E	unknown	Q	
in read mem(28)	F		R	
mem(2C)	G	0x01	S	memS(40)
in read mem(44)	H	0x02	T	0x44
busy mem(48)	I		U	
	J	0x04	V	
	K	05???	W	
	L	0x05	X	

ELE 4142 HW7 Name_____

Assume a PCIe Link operating a 8GT/s 30pts

a) In a 1x configuration what is the Link bandwidth using 8b/10b encoding (don't use the table from the notes – it will not be right)

8GT/s * (8b/10T) = 6.4Gb/s → 800MB/s

b) In a 4x configuration what is the Link BW using 128b/130b encoding

(8GT/s * 4) * (128b/130T) = 31,507,692b/s → 3,938,462B/s

c) Assuming a 1x configuration, 8b/10b encoding, a 4DW header, 32 Bytes of data and no ECRC or End, how many bits would transfer in a single read request?

32 Bytes of data + 16 bytes of header + 2 bytes of sequence + 4 bytes of LCRC + 2 bytes of STP
= 56 bytes = 448 bits 448 bits *10T/8b = 560 bits

d) Assuming a 4x configuration, 8b/10b encoding, a 4DW header, 32 Bytes of data and no ECRC or End, how long would a single read request take?

560 bits from part C split across 4 lanes = 140 bits / lane (simultaneous)
140bits / (8GT/s / 2) = 35ns

ELE 4142 HW7 Name_____

Search and Think 20 pts

Identify and explain 3 advantages of using differential signaling

2x signal swing at the same supply voltage

→ better noise immunity

→ opportunity to operate at lower voltages

Matched signals create less electromagnetic interference EMI

Matched signals are less susceptible to electromagnetic interference EMI

No required common mode voltage

Identify at least 1 disadvantage of differential signaling

Requires 2 wires or twice the board space + any addition spacing to protect 2 wires