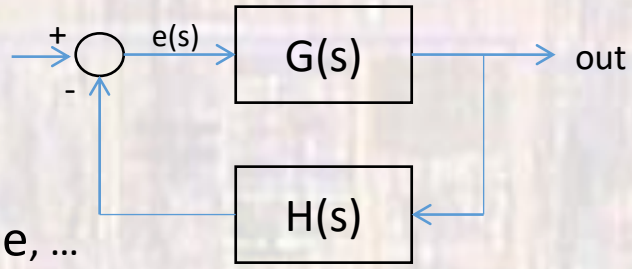
Locked Loops

Last updated 1/11/24

PLL Basics

- Phase Locked Loop (PLL)
  - Control System Perspective
    - Negative Feedback forces e(s) to zero
    - Signals can be voltages, currents, phase, …

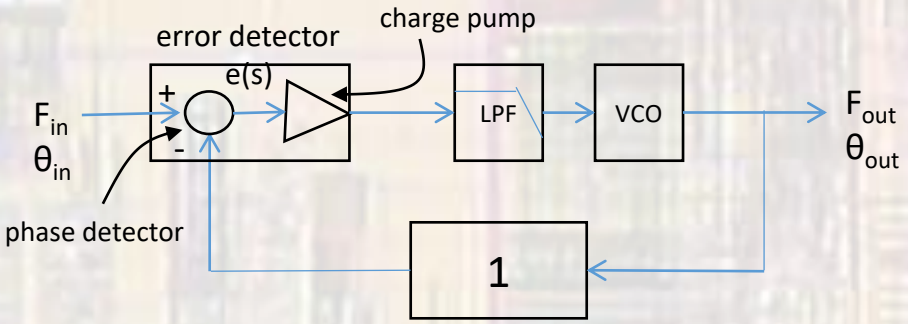


  - Phase Locked Loop
    - Designed to match an output signal to the frequency and phase of an input signal
    - Signals must be periodic (clocks)
    - By using input and feedback dividers the PLL can create an output that is a fractional frequency of the input

$$F_{out} = F_{in}\left(\frac{m}{n}\right)$$

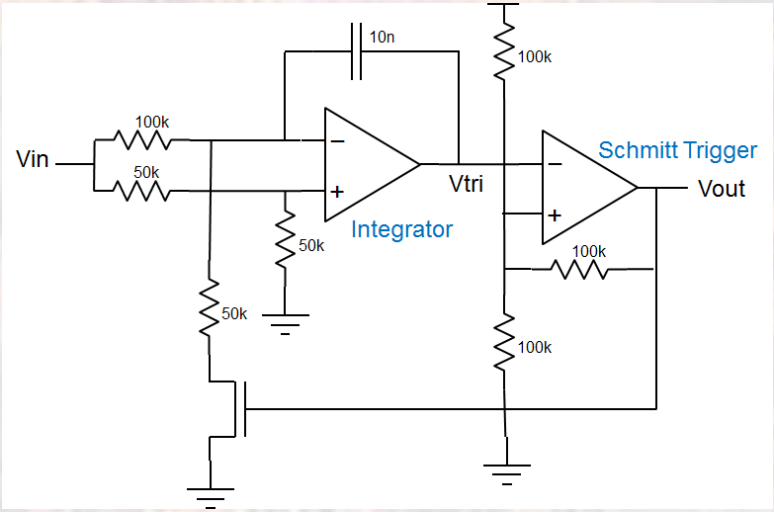
PLL Basics

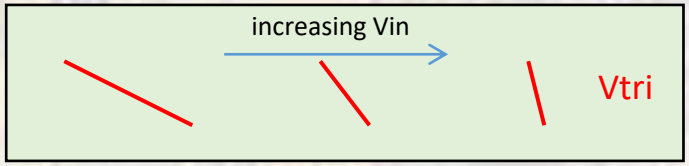
- Phase Locked Loop (PLL)
  - Phase Locking
    - Phase detector creates an error signal based on the difference between the input and the feedback signals
    - Charge pump creates pulses directed to reduce the error
    - The LPF smooths the pulses
    - The VCO creates a frequency signal proportional to the voltage input
    - The created frequency is fed back to compare to the input frequency



PLL Basics

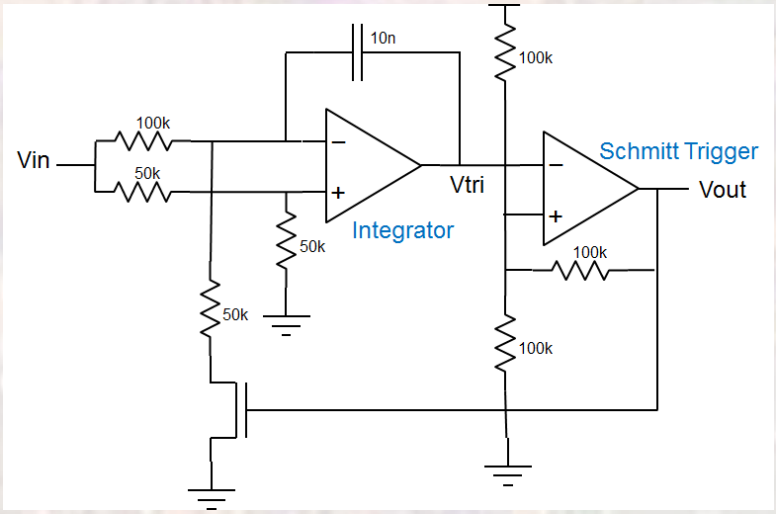
- Voltage Controlled Oscillator (VCO)
  - Integrator
    - Opamp wants v+input = v-input
    - When the MOSFET is off
      - + input is Vin/2 (minus input wants to be Vin/2)
      - current through 100K resistor must go through C
      - current through C Ic = -Cdv/dt
      - -dv/dt is proportional to Vin → the opamp slews down

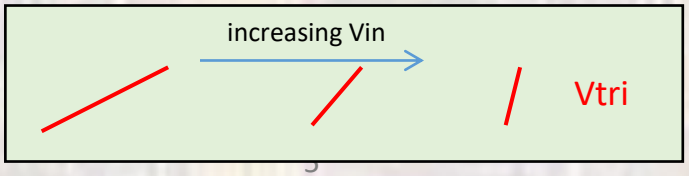




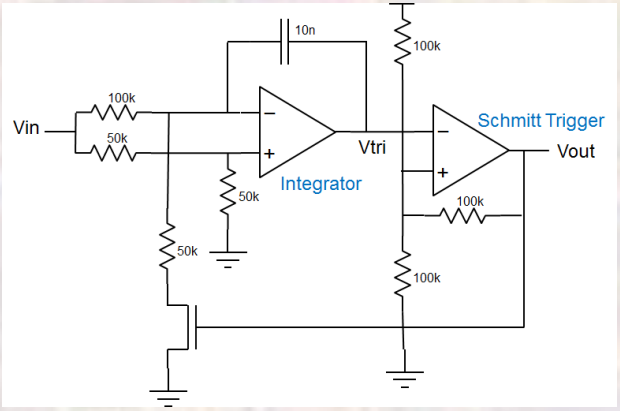
PLL Basics

- Voltage Controlled Oscillator (VCO)
  - Integrator
    - Opamp wants v+input = v-input
    - When the MOSFET is on
      - + input is Vin/2 (minus input wants to be Vin/2)
      - current through the 100K resistor is ½ the current through 50K and MOSFET
      - the other half the current through the MOSFET must come from the C
      - current through C Ic = Cdv/dt
      - dv/dt is proportional to Vin → the opamp slews up

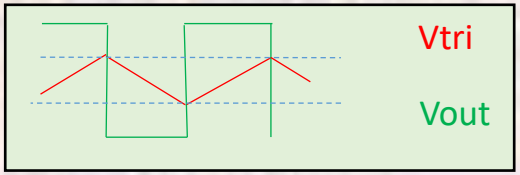


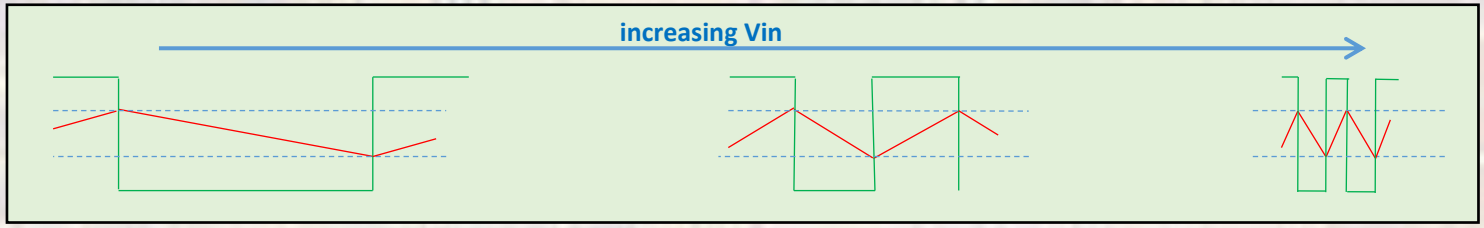


PLL Basics



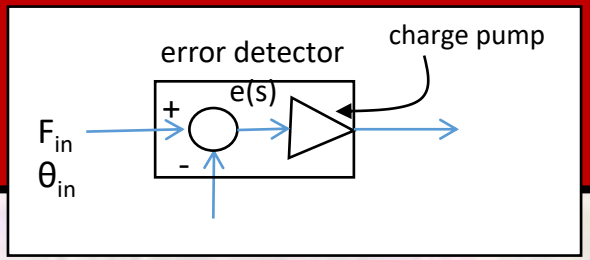
- Voltage Controlled Oscillator (VCO)
  - Schmitt Trigger
    - When Vout is high
      - Mosfet is on → Vtri is slewing up
      - + input is Vdd*2/3
      - When Vtri goes above Vdd*2/3 the opamp switches to Vout = 0
      - mosfet turns off → Vtri slews down
    - When Vout is low
      - Mosfet is off → Vtri is slewing down
      - + input is Vdd*1/3
      - When Vtri goes below Vdd*1/3 the opamp switches to Vout = high
      - mosfet turns on → Vtri slews up



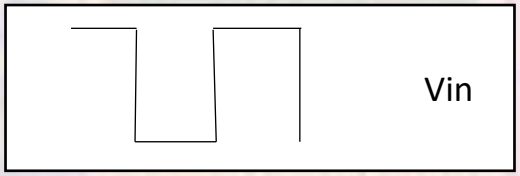


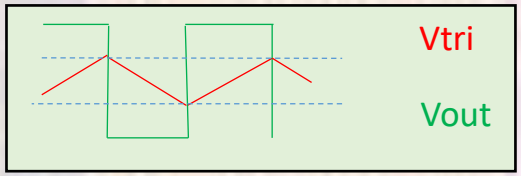
VCO

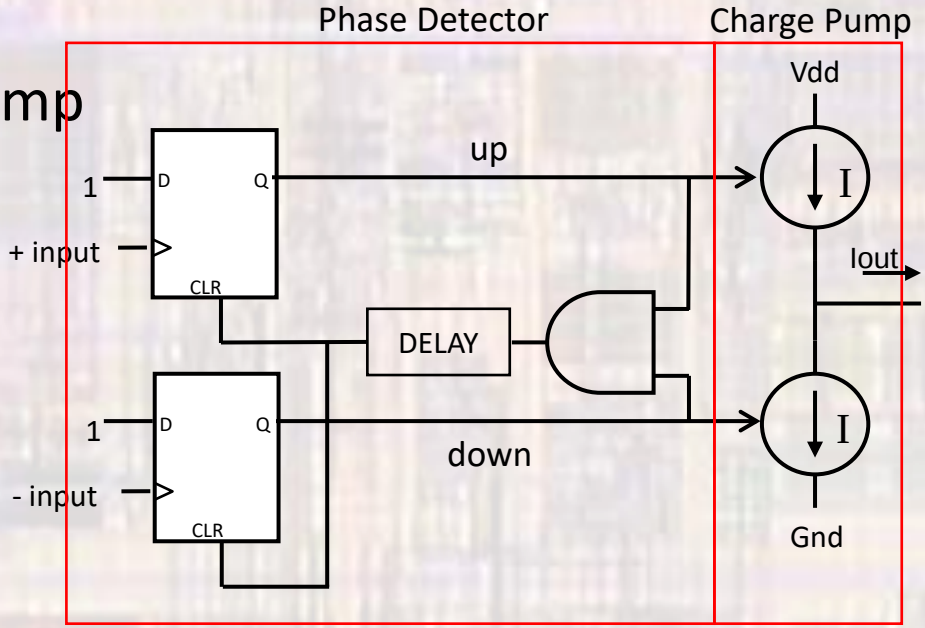
PLL Basics



- Error Detector
  - Phase detector + charge pump





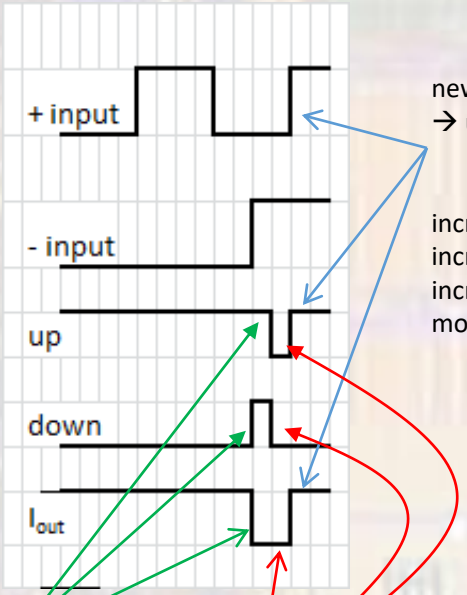


  - Charge Pump

Up	Down	Upper I src	Lower I src	I out
0	0	off	off	0
0	1	off	on	sink (-I)
1	0	on	off	src (+I)
1	1	on	on	0

PLL Basics

- Error Detector
  - Phase detector

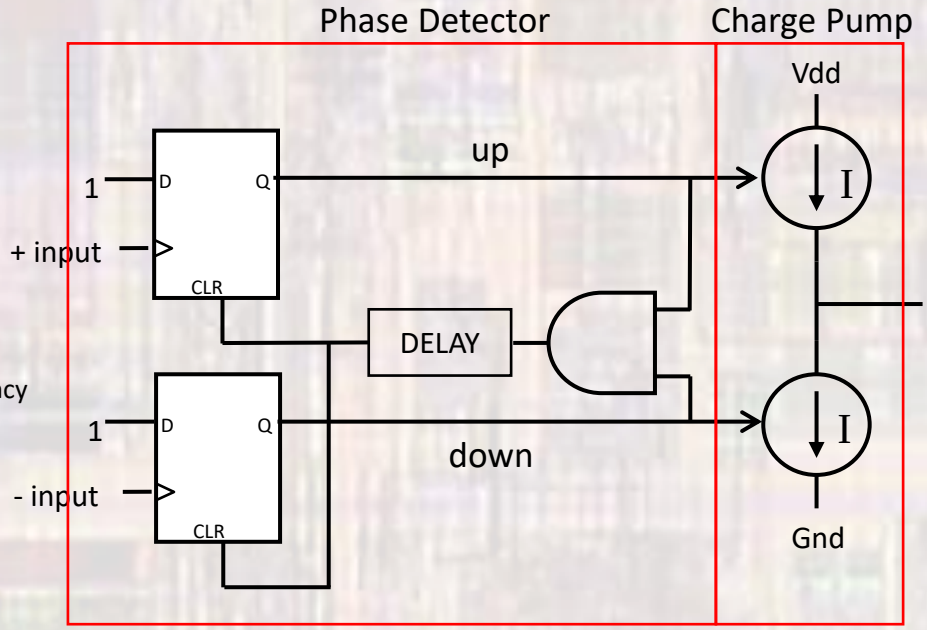


new input clock
→ up turns on

increases filter voltage
increases VCO voltage
increases feedback frequency
moves toward lock

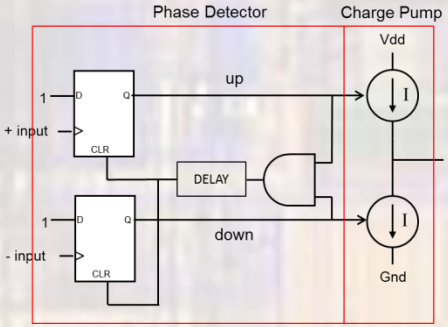
both I sources on
no current flows out

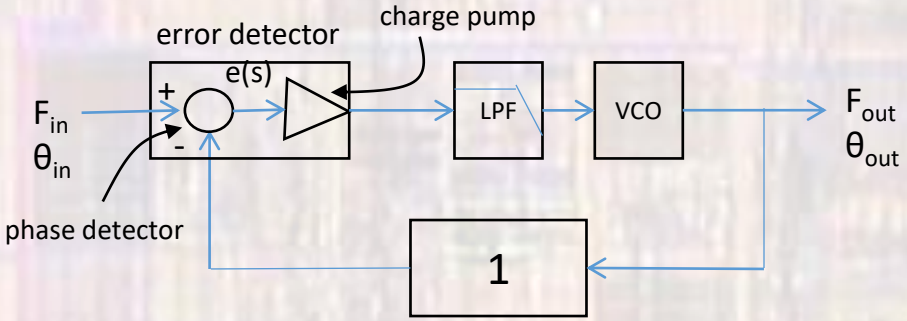
after delay both FF reset
both I sources off
no current flows out

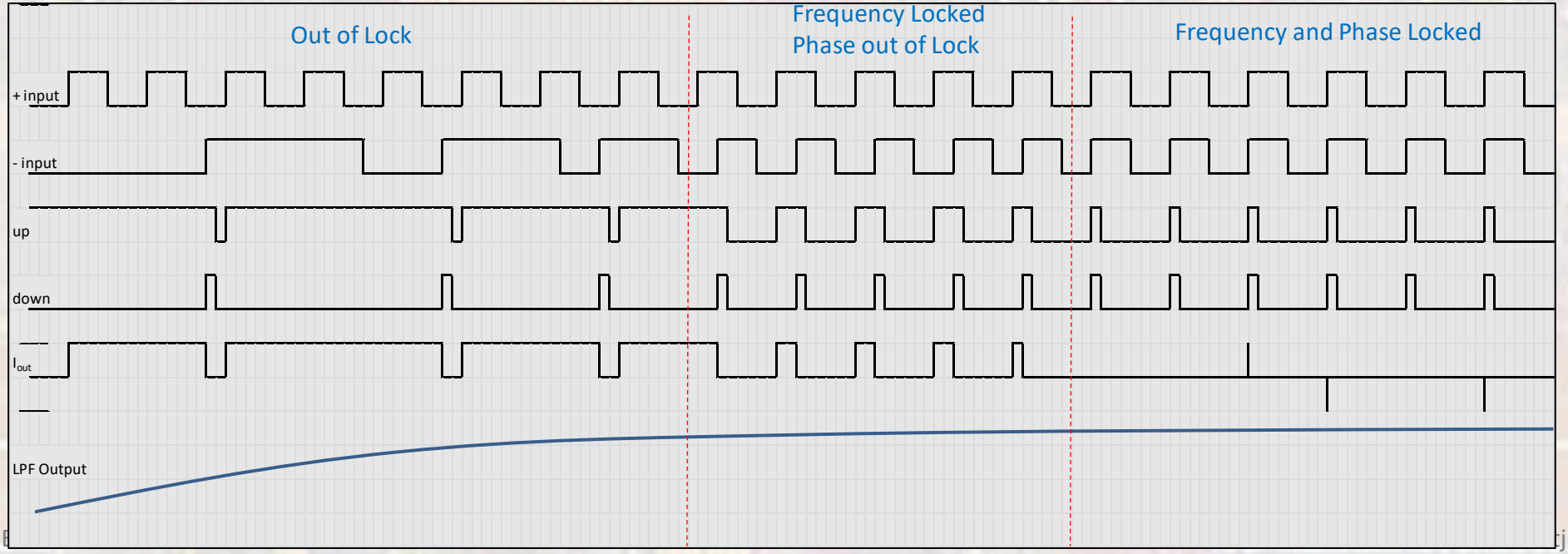


PLL Basics

- Phase Locked Loop

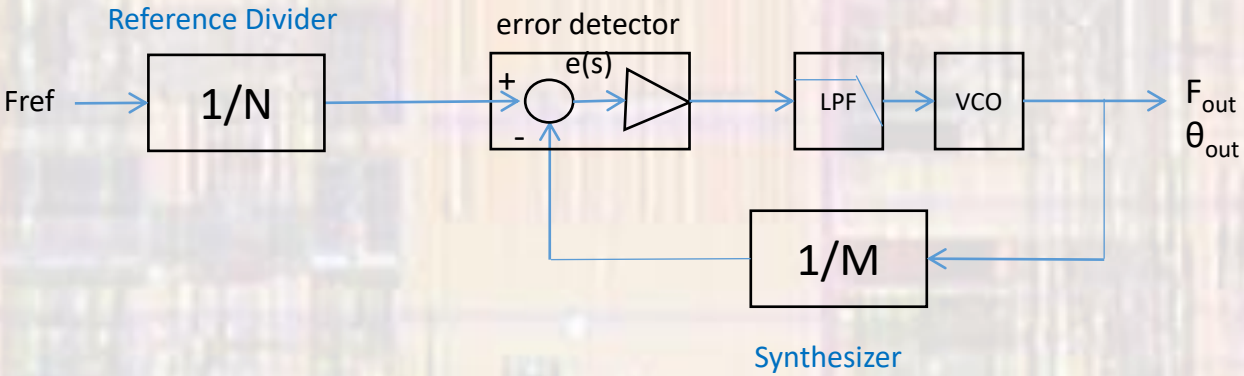


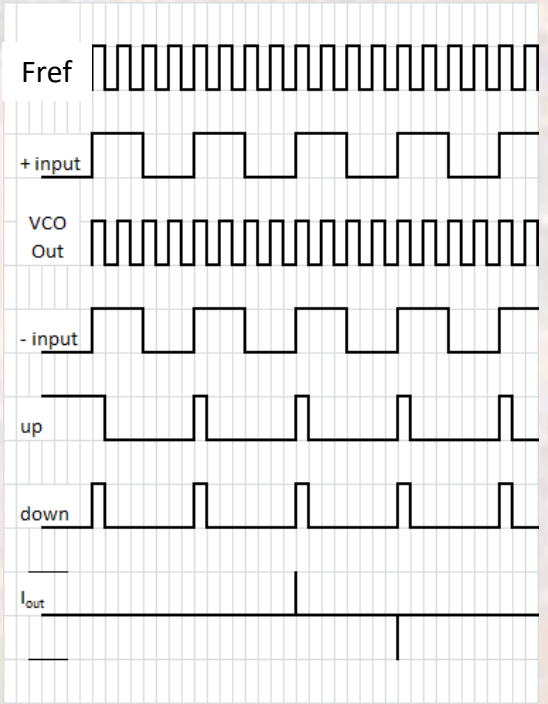




PLL Basics

- Phase Locked Loop
  - Unity feedback is not very interesting
  - Want to be able to vary frequency
    - Selectable operating frequency
    - DVFS for power/performance tradeoff

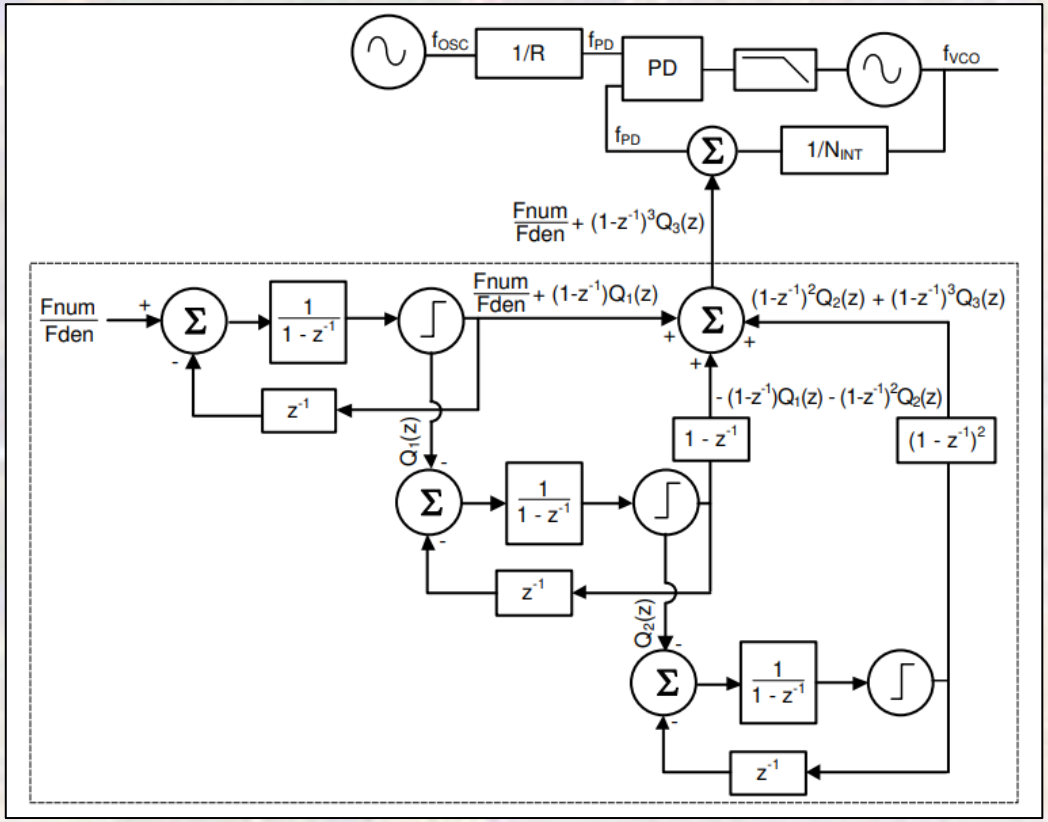




$$Fout = Fref \times \frac{M}{N}$$

Fractional N PLL

- Allow the feedback divider to be have a fractional part
  - Fout = Fin(N_{INT} + Fnum/Fden) / R



Delay Locked Loop (DLL)

- Used for clock synchronization
  - Similar to a PLL but all digital
    - Replace the VCO with a variable Delay Line