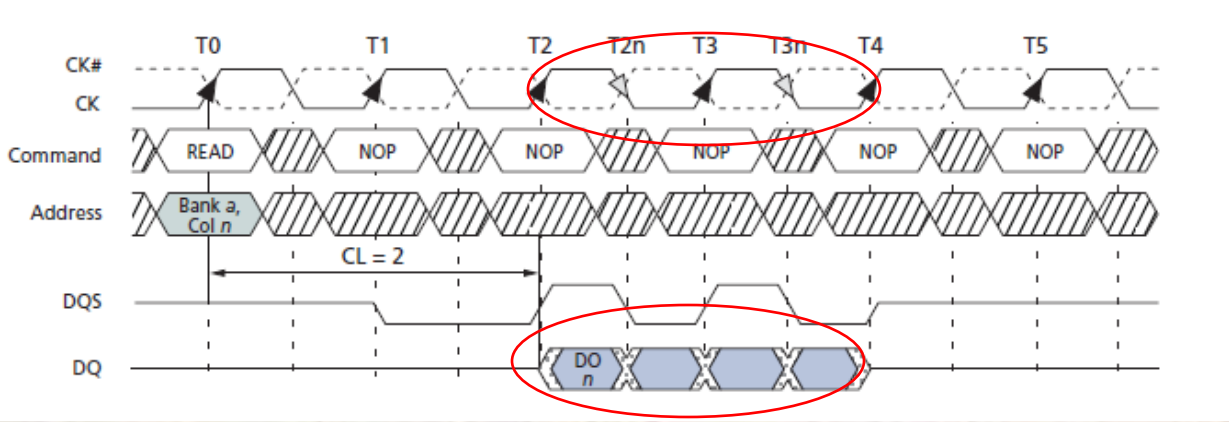
DDR SDRAM Operation

Last updated 2/8/24

DDR SDRAM - Operation

- DDR
  - Double Data Rate
  - Data I/O on clk and clkb
  - Pre-fetches 2 words per read
    - Provides 2 words / array access
  - Allows for data to flow at 2x the memory access speed



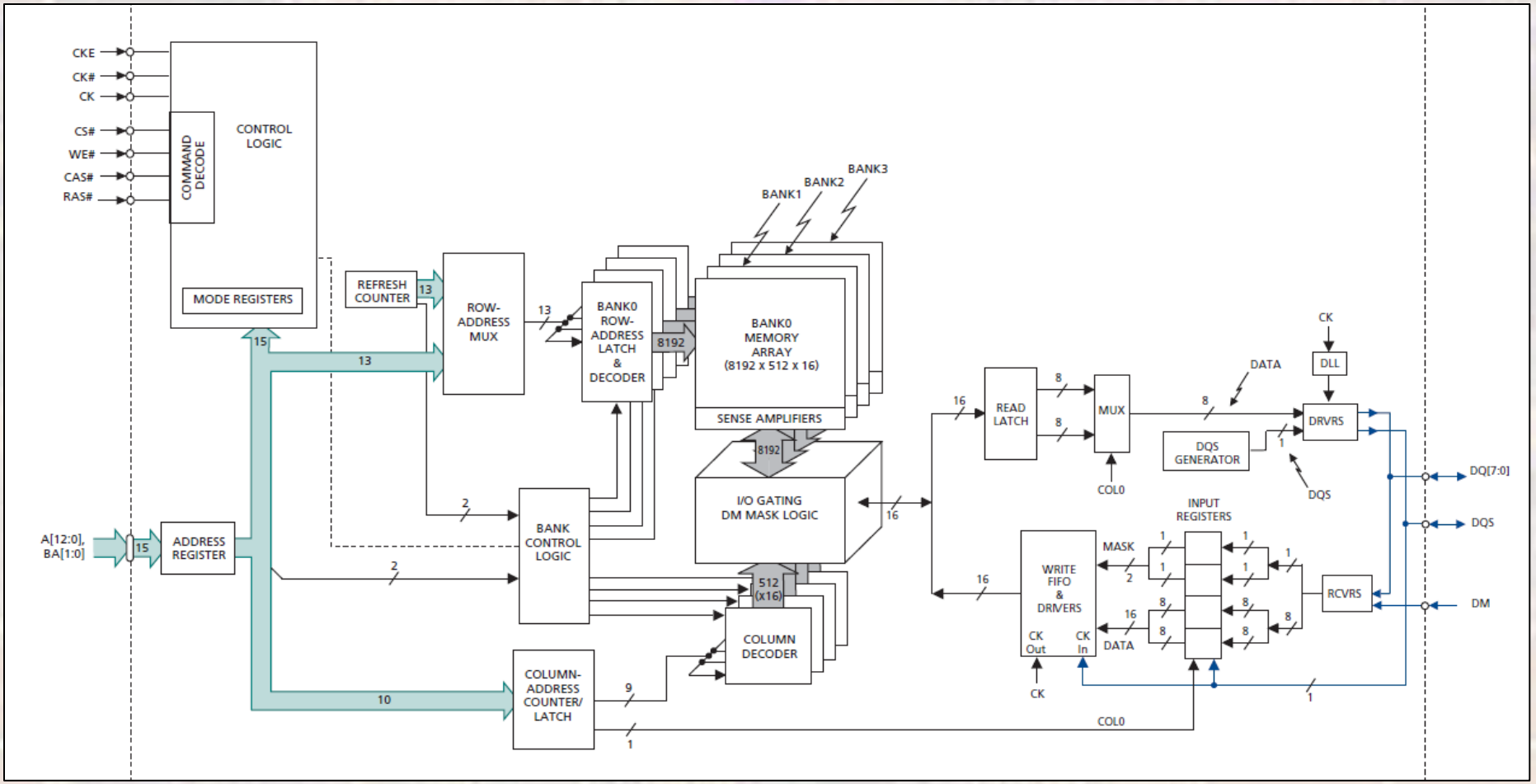
DDR SDRAM - Operation

- DDR SDRAM - Additional Signal
  - D/Q Strobe – DQS
    - Generated by the memory chip on reads
      - Matches timing of data
      - Receiver (MMU for example) uses this to generate its latch signal (mid DQS)
    - Externally generated on writes
      - Must be near center of write data
      - Used by the memory to latch the input data

FBGA Numbers	TSOP Numbers	Symbol	Type	Description
E3 E7 E3	51 16 51	DQS LDQS UDQS	I/O	**Data strobe:** Output with read data, input with write data. DQS is edge-aligned with read data, centered in write data. It is used to capture data. For the x16, LDQS is DQS for DQ[7:0] and UDQS is DQS for DQ[15:8]. Pin 16 (E7) is NC on x8.

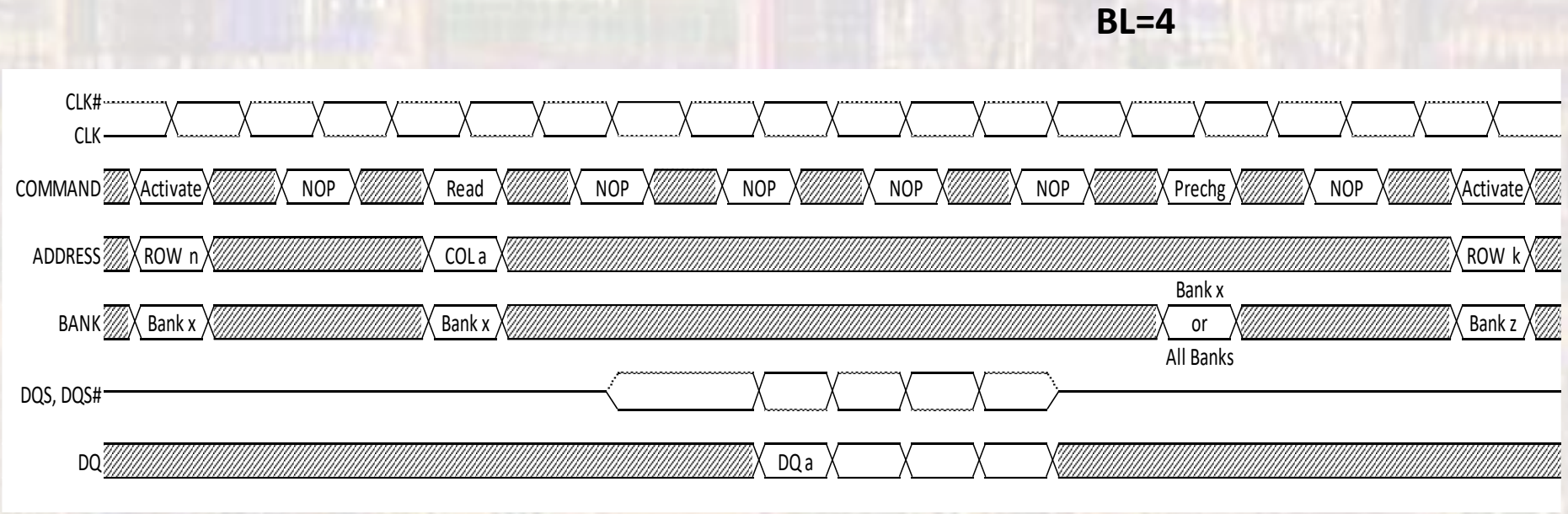
DDR SDRAM - Operation

- DDR SDRAM
  - 256Mb : 32Mx8



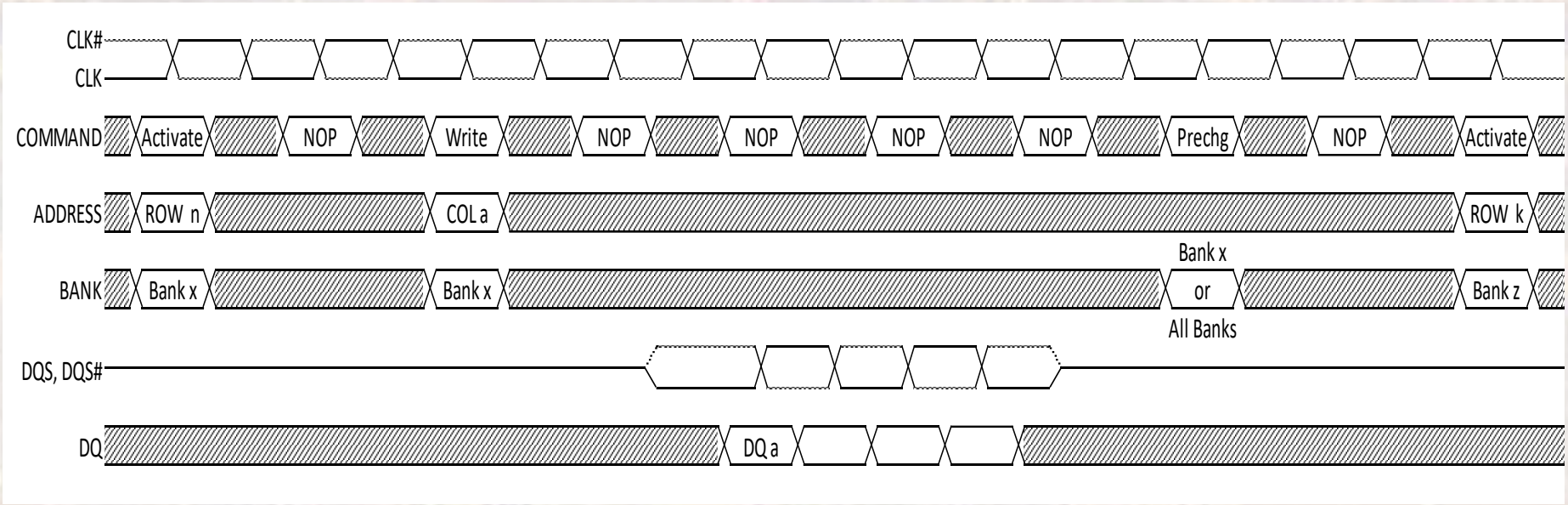
DDR SDRAM - Operation

- DDR SDRAM – Timing
  - Read



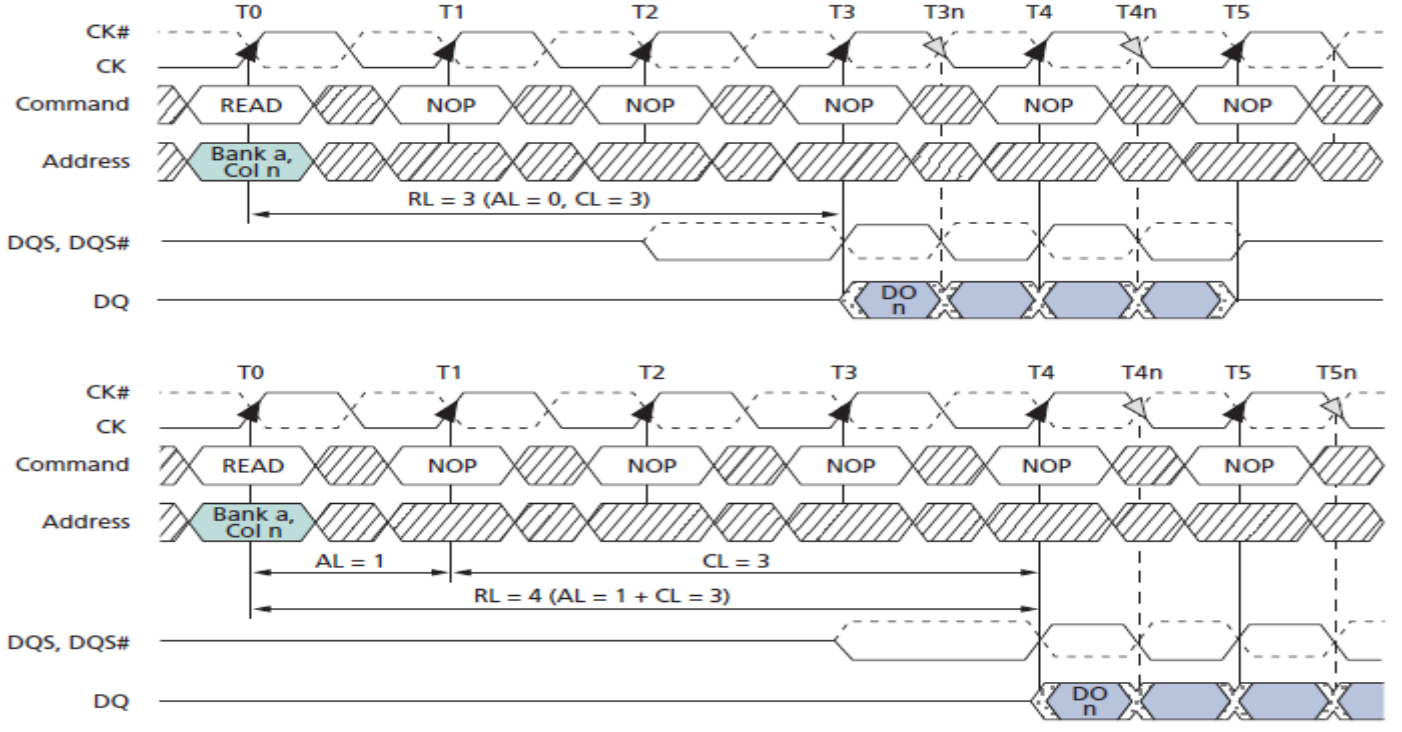
DDR SDRAM - Operation

- DDR SDRAM – Timing
  - Write



DDR SDRAM - Operation

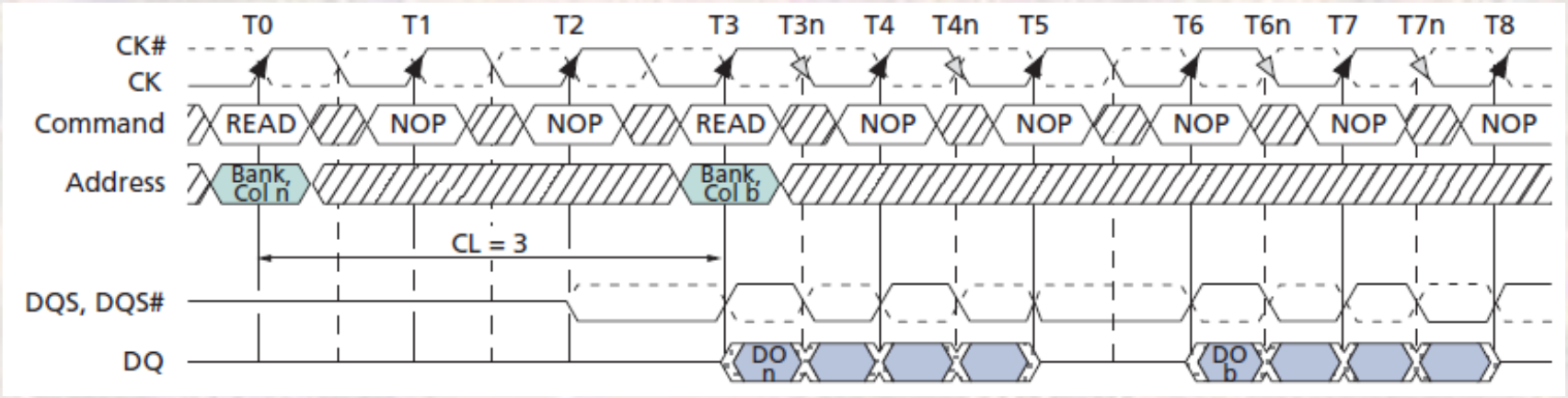
- DDR SDRAM – Timing
  - Read Latency
    - CL – CAS latency – clock cycles from CAS to data out
    - AL – Additional Latency – pipeline commands or to match parts



BL=4

DDR SDRAM - Operation

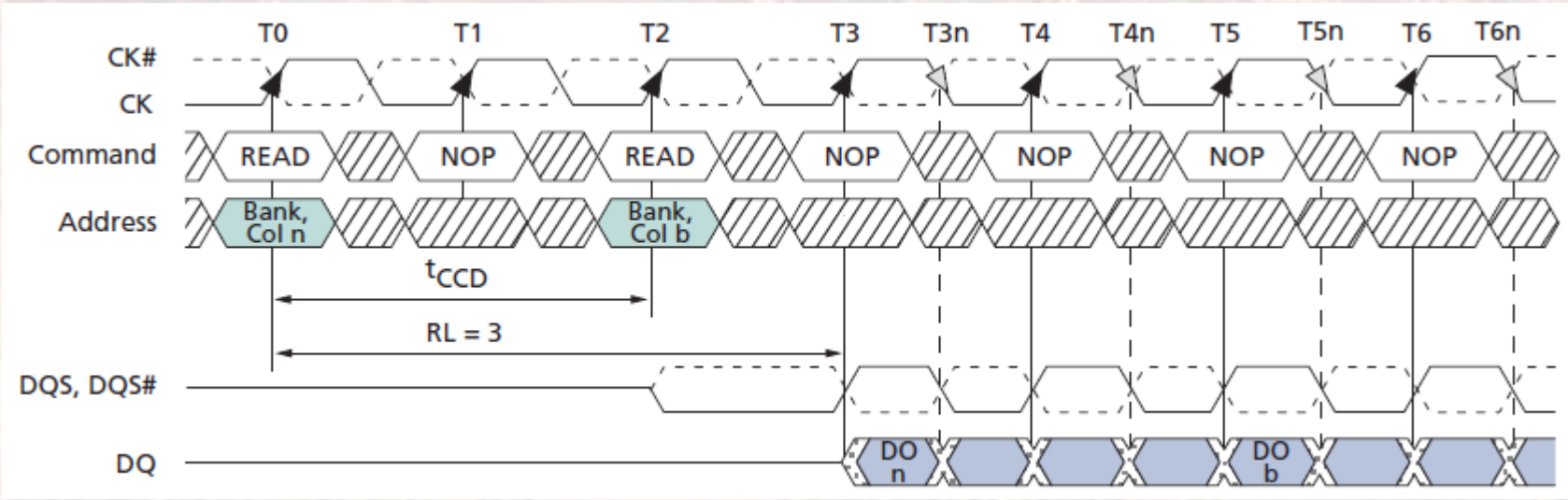
- SDRAM – Timing
  - Non-consecutive Read bursts



BL=4

DDR SDRAM - Operation

- DDR SDRAM – Timing
  - Consecutive Read bursts

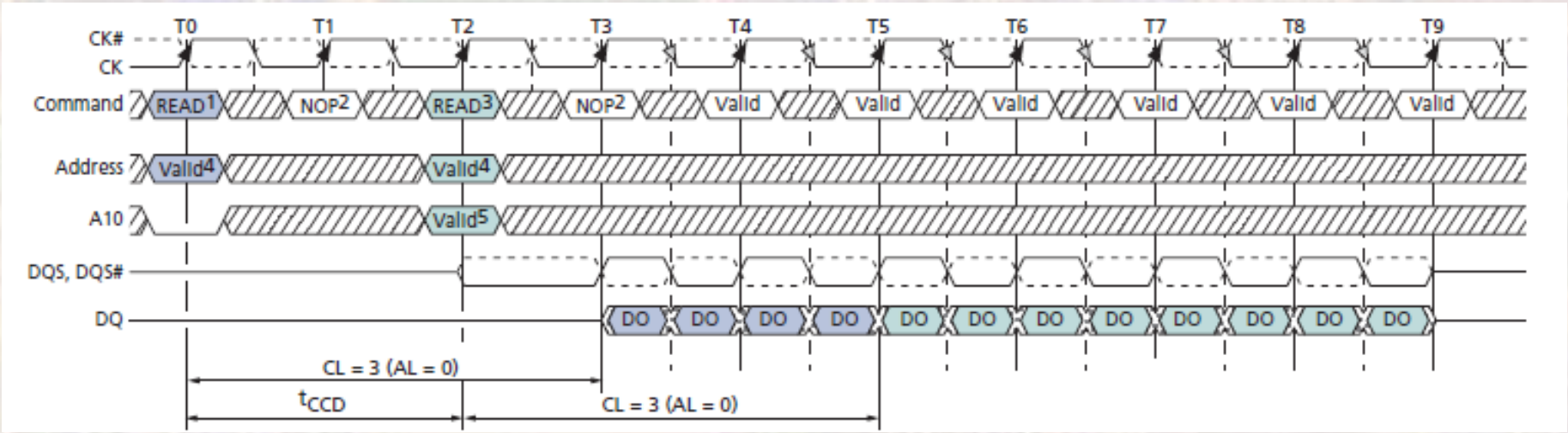


BL=4

DDR SDRAM - Operation

- DDR SDRAM – Timing
  - Read interrupted by read

BL=8

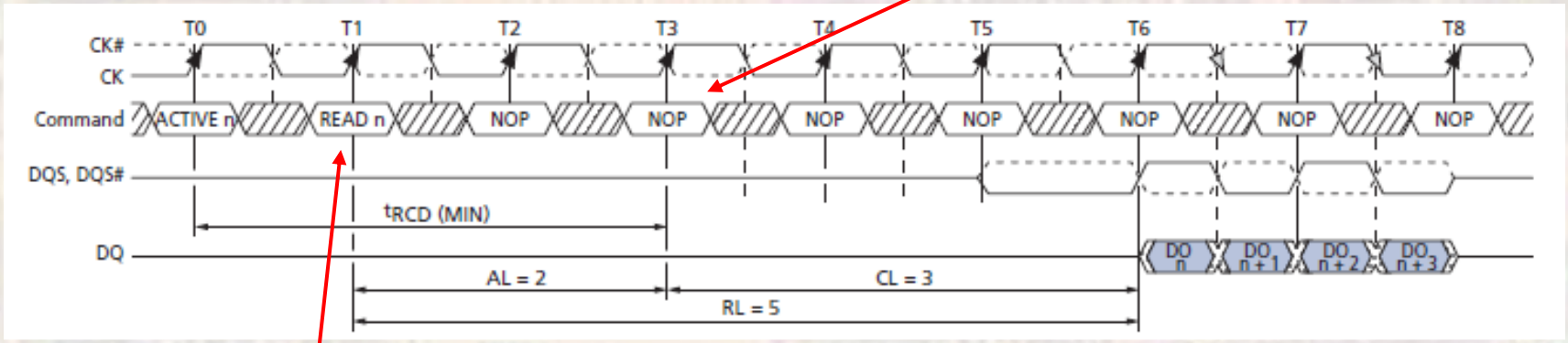


  - Valid addresses include
    - Same bank, same row w/o precharge
    - Different bank – assuming precharged

DDR SDRAM - Operation

- DDR SDRAM – Timing
  - POSTED CAS
    - For CL=3, set AL=2 and move the READ command forward 2 clocks

Normally the read would be here

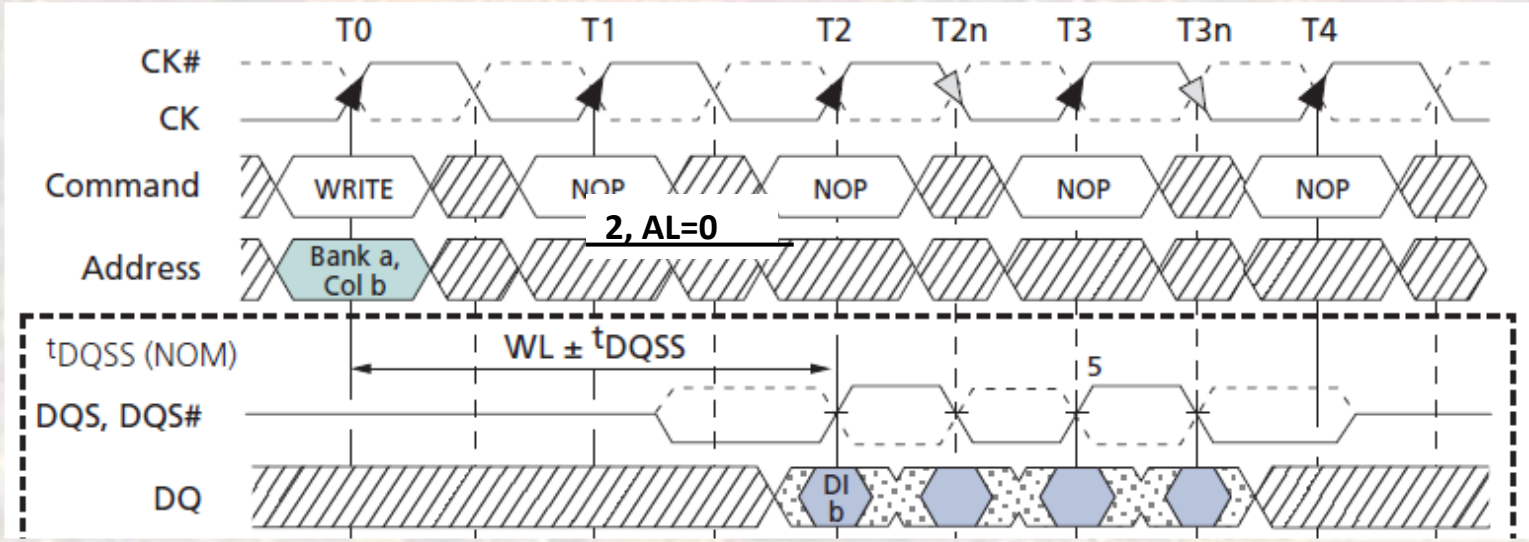


BL=4

Move the read forward to complete the cycle and do something else

DDR SDRAM - Operation

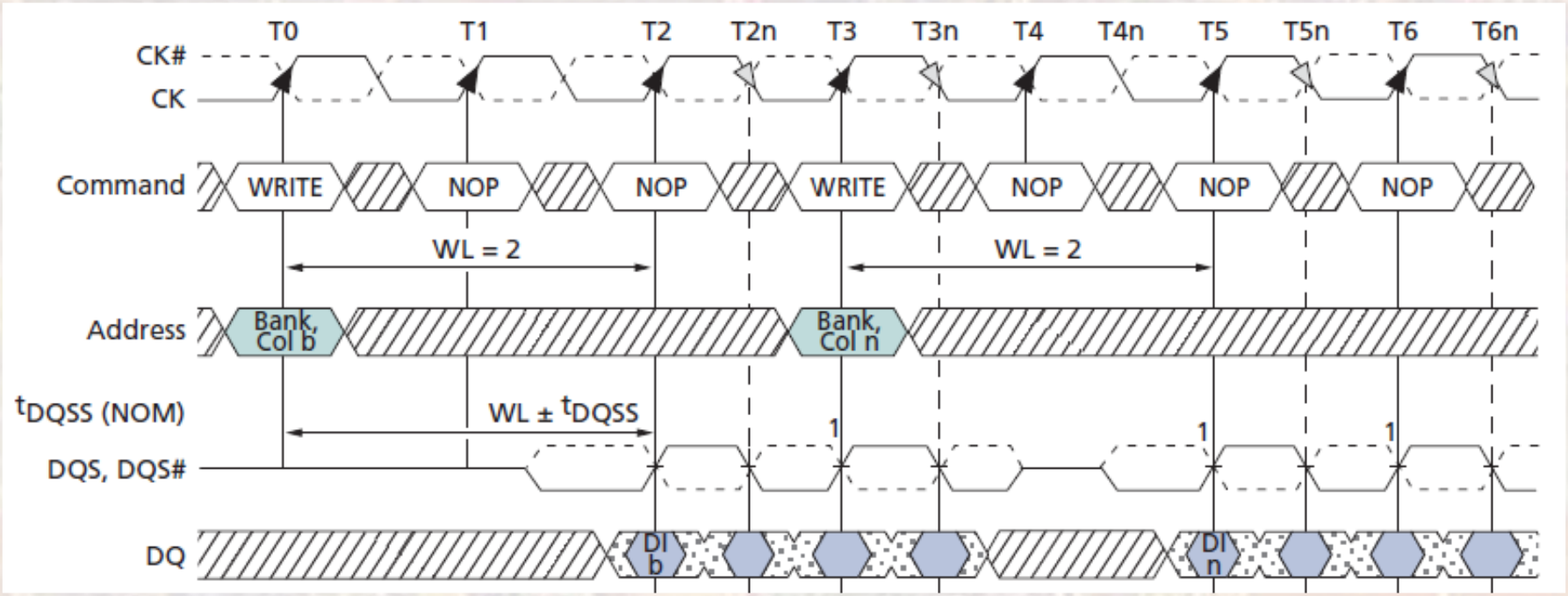
- DDR SDRAM – Timing
  - Write
    - DQS generated by the MMU in write mode
    - Edge must match up with the center of valid data



DDR SDRAM - Operation

- DDR SDRAM – Timing
  - Non-consecutive Writes

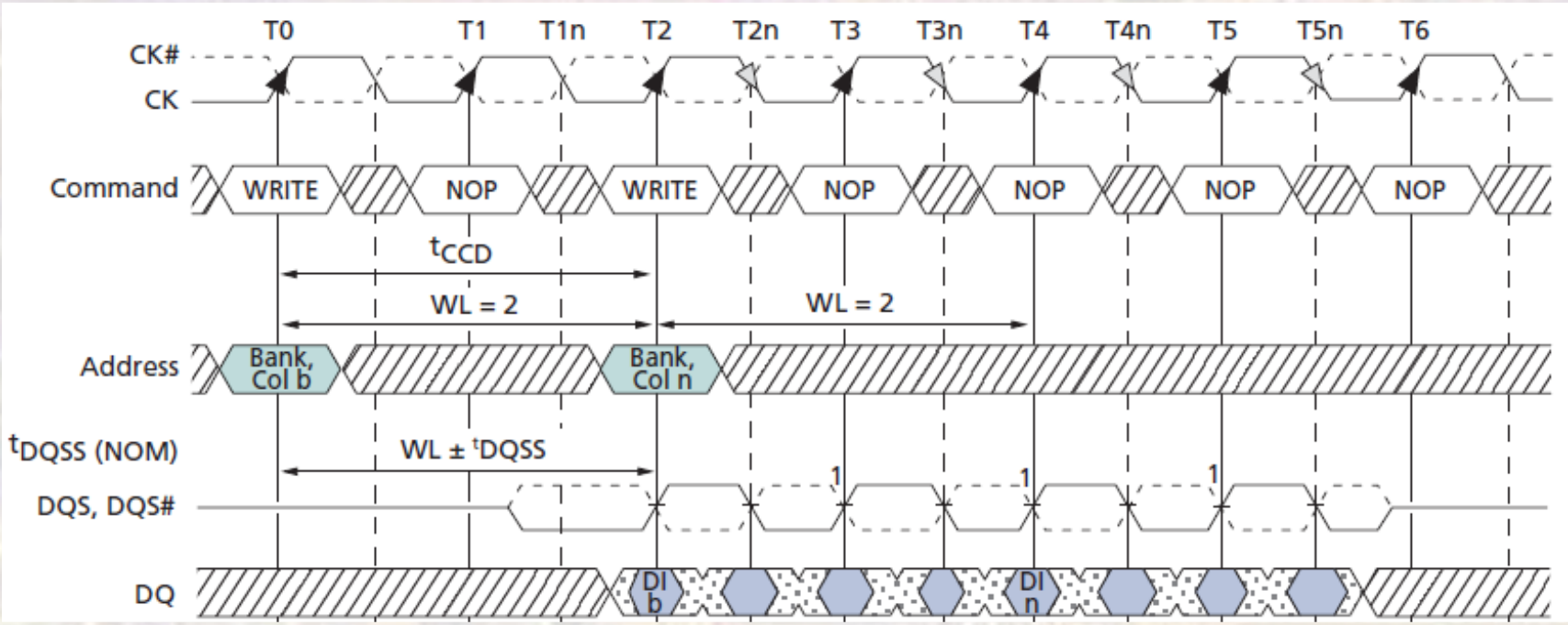
BL=4



DDR SDRAM - Operation

- DDR SDRAM – Timing
  - Consecutive Writes

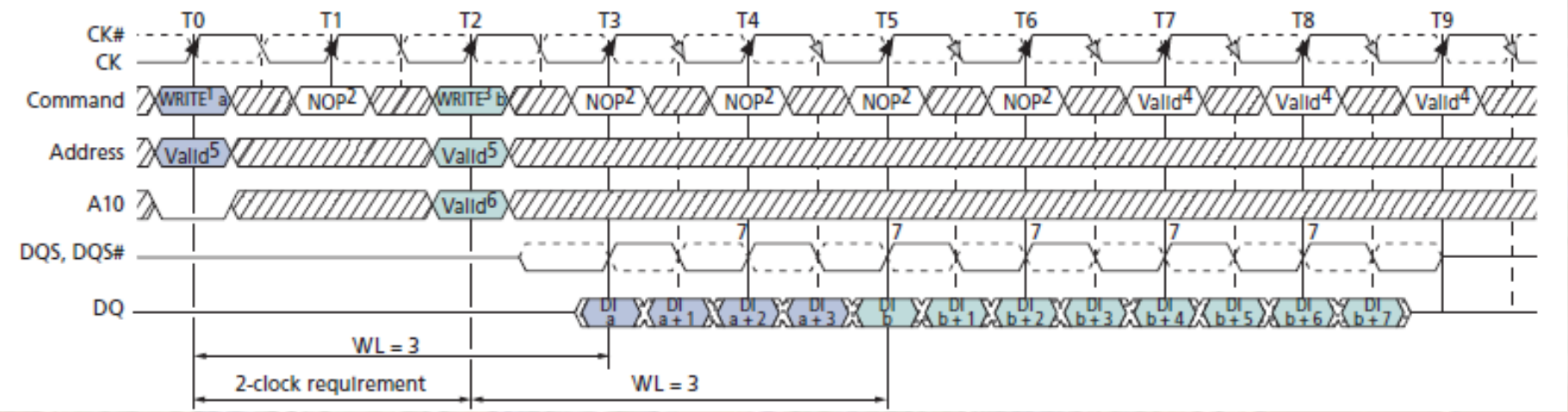
BL=4



DDR SDRAM - Operation

- DDR SDRAM – Timing
  - Write interrupt by Write

BL=8



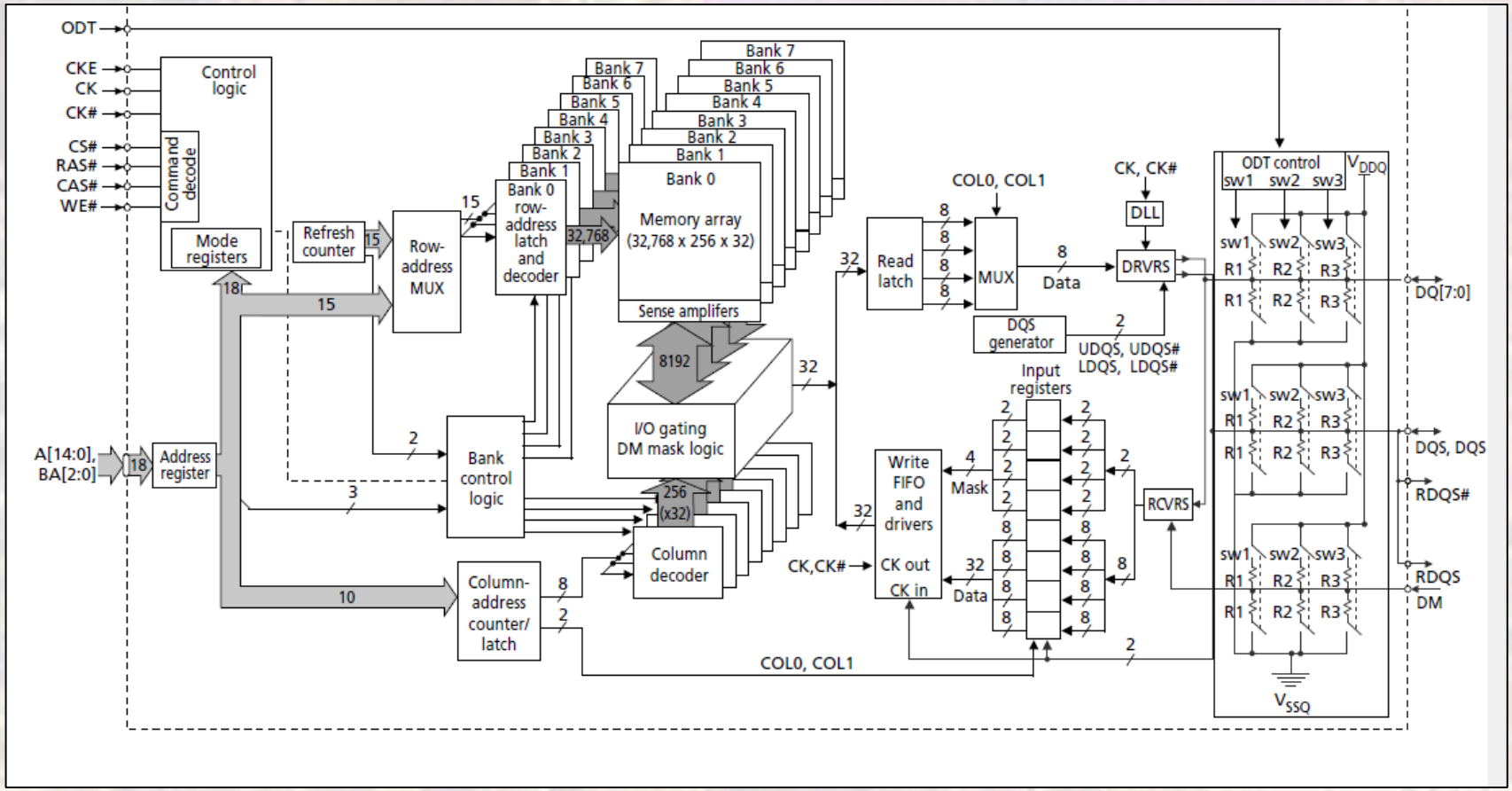
DDR SDRAM - Operation

- DDR SDRAM Generations
  - All generations use clk and clkb for data

  - DDR – 2 word pre-fetch
  - DDR2 – 4 word pre-fetch
  - DDR3 – 8 word pre-fetch
  - DDR4 – 8 words pre-fetch, enhanced bank structure
  - DDR5 – 16 words pre-fetch, enhanced bank structure

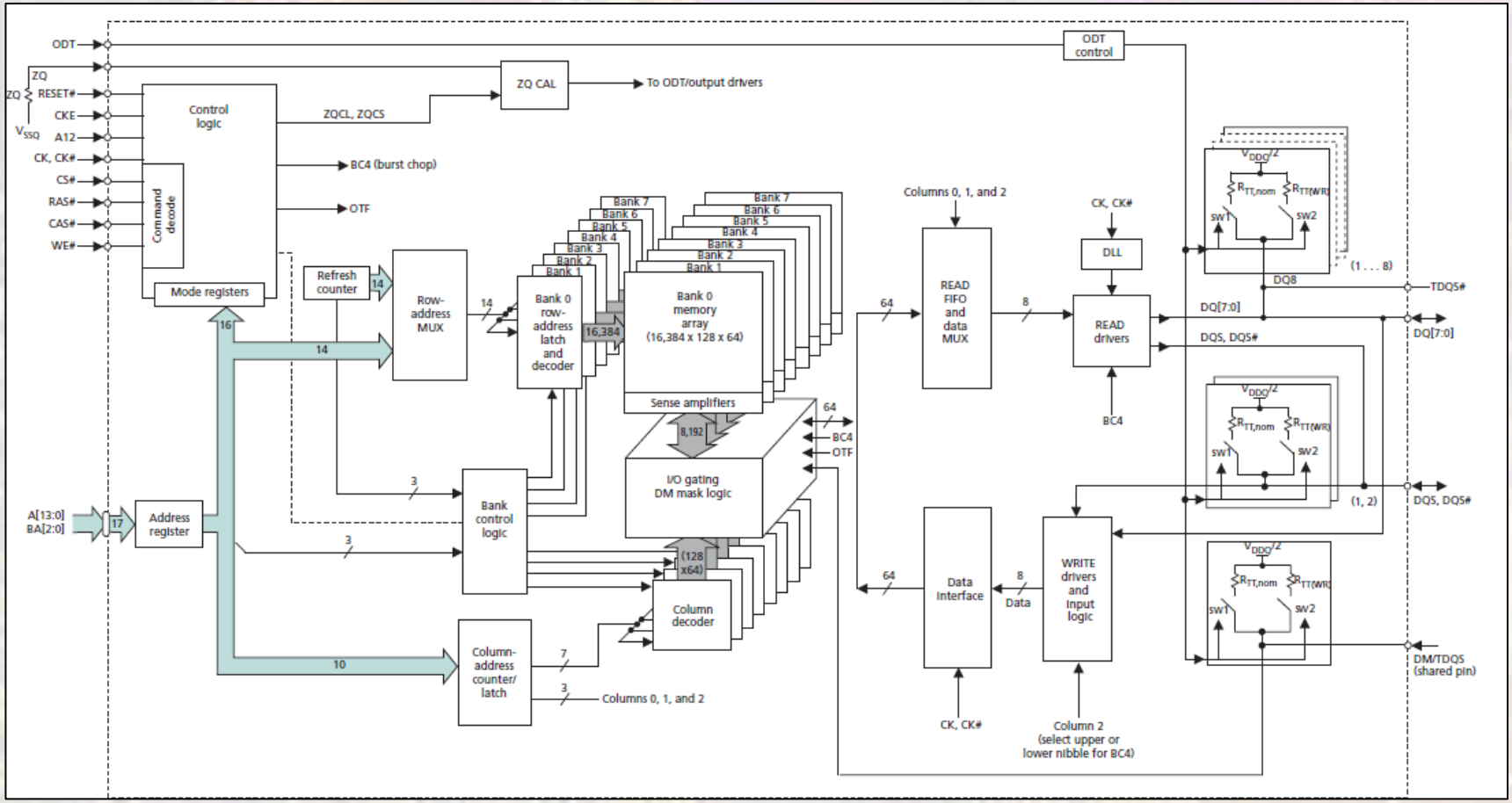
DDR SDRAM - Operation

- DDR2
  - 2Gb: in a x8



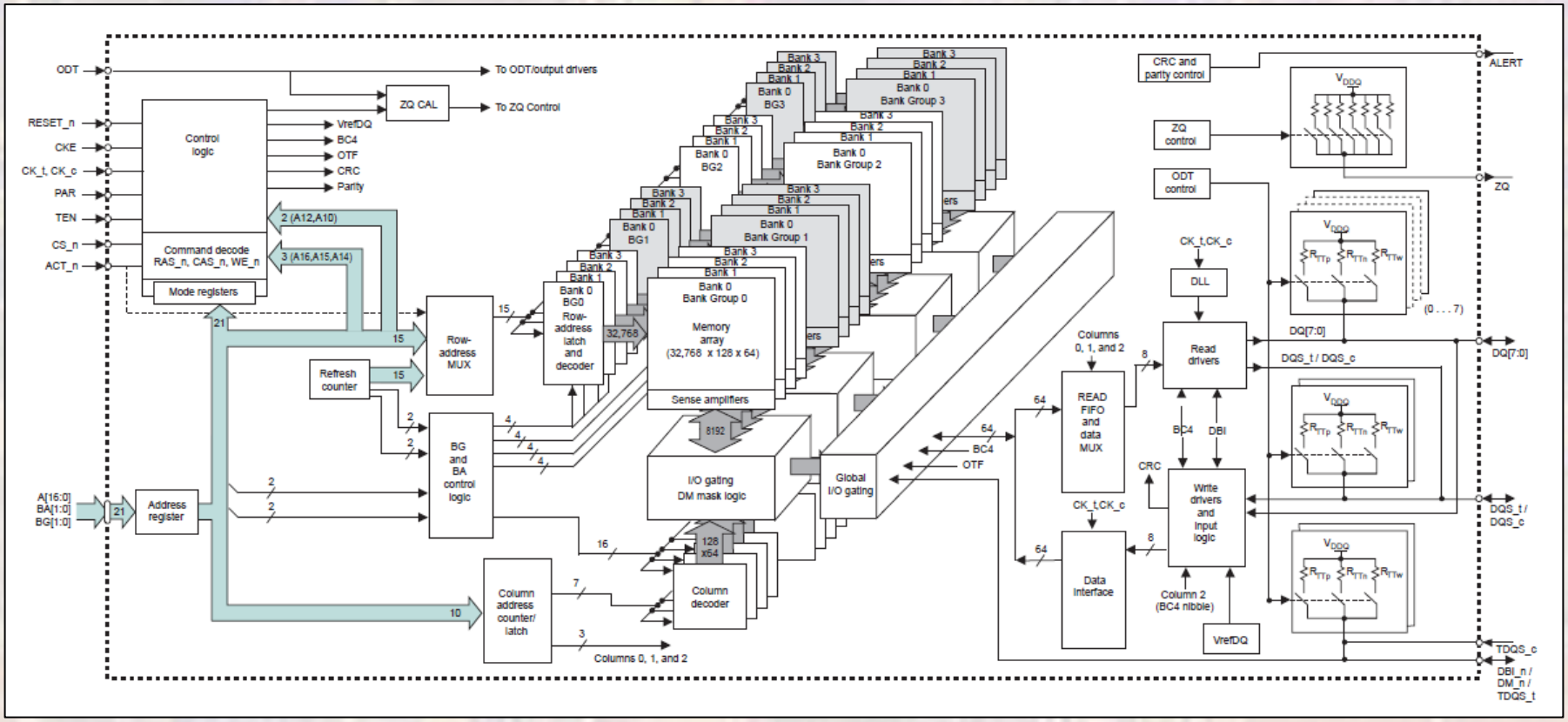
DDR SDRAM - Operation

- DDR3
  - 1Gb: in a x8



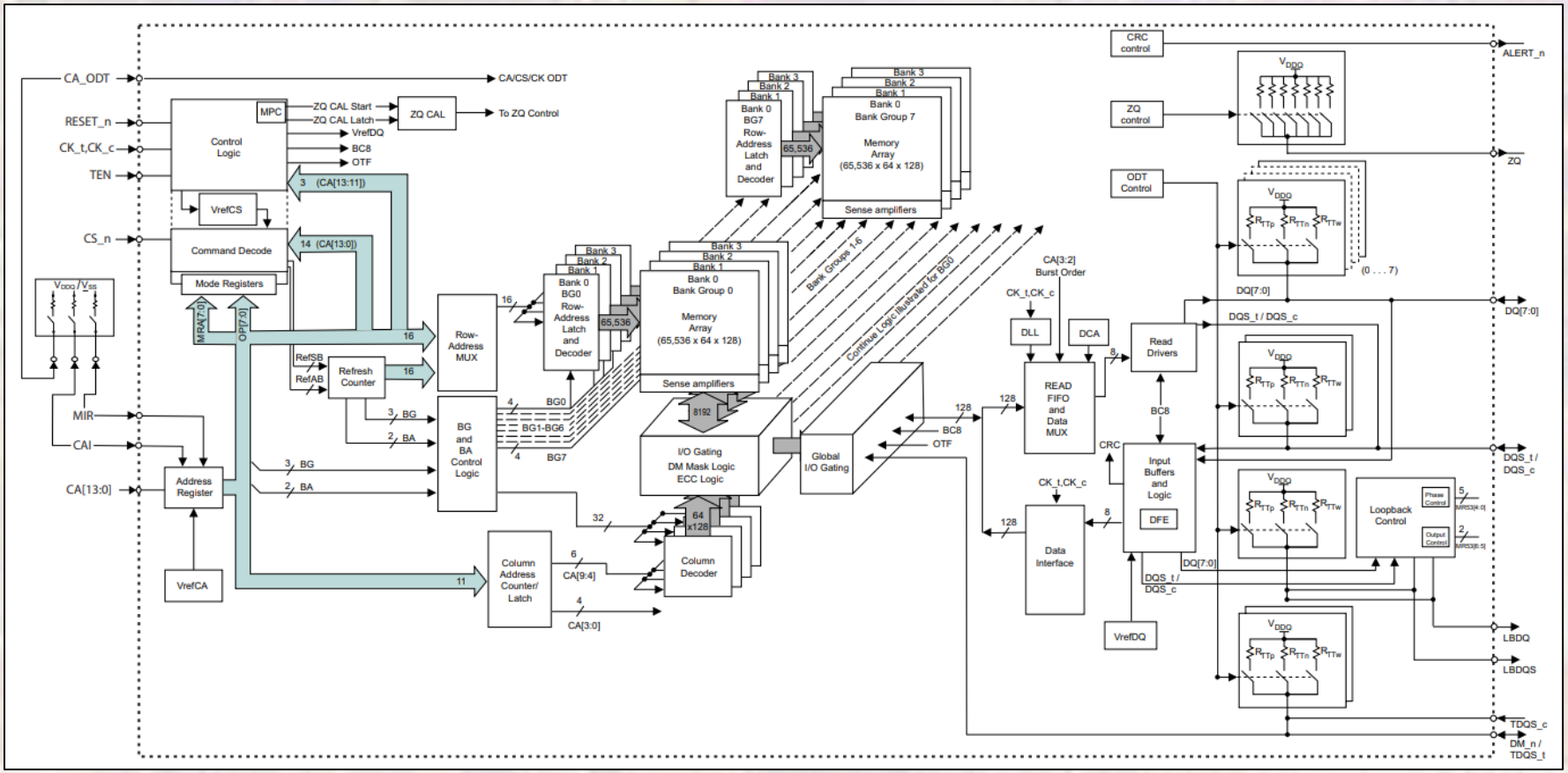
DDR SDRAM - Operation

- DDR4
  - 4Gb: in a x8



DDR SDRAM - Operation

- DDR5
  - 16Gb: in a x8



DDR SDRAM - Operation

- Transfers / sec
  - With data flowing on clk and clkb data transfer is 2X clock rate
  - MT/s – M Transfers / sec

  - SDRAM – DDR3 spec sheet

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-107[1, 2]	1866	13-13-13	13.91	13.91	13.91
-107E[1, 2]	1866	12-12-12	12.84	12.84	12.84
-125[1, 2]	1600	11-11-11	13.75	13.75	13.75
-15E[1]	1333	9-9-9	13.5	13.5	13.5
187E	1066	7-7-7	13.1	13.1	13.1

- 1866MT/s --> 933MHz clock operation
- --> 1.071ns/clock
- --> CL=13 means tCL = 13.93ns delay for a read from the array

DDR SDRAM - Operation

- Dimm
  - Dual Inline Memory Module
  - Multiple memory chips integrated onto a board
  - Support 64bit transfers
  - Parallel configuration
    - Different chip selects
  - Word configuration
    - Each chip supplies part of a bigger word
    - 8, x1 devices → 8 bit word
    - 8, x4 devices → 32 bit word
  - use PCx-zzzz where zzzz is max bandwidth (transfer rate in bytes)
    - DDR2-800 → pc2-6400 (transfers x # bits /8) = 800M x 64b /8 = 6.4GB/s

DDR SDRAM - Operation

- DDR – Technology

Memory Type	Release Year	Bandwidth	Pins per Ch	Voltage (V)	Prefetch
SDR	1993	1.6 GB/s	168	3.3	1n
DDR	2000	3.2 GB/s	184	2.5/2.6	2n
DDR2	2003	8.5 GB/s	240	1.8	4n
DDR3	2007	17 GB/s	240	1.35/1.5	8n
DDR4	2014	25.6 GB/s	380	1.2	8n
DDR5	**2019**	**32GB/s**	**380**	**1.1**	**8/16n**

DDR SDRAM - Operation

- DDR - Technology

Memory	Real Clock	Maximum Theoretical Transfer Rate	Memory Module
DDR200	100 MHz	1,600 MB/s	PC-1600
DDR266	133 MHz	2,133 MB/s	PC-2100
DDR333	166 MHz	2,666 MB/s	PC-2700
DDR400	200 MHz	3,200 MB/s	PC-3200
DDR2-400	200 MHz	3,200 MB/s	PC2-3200
DDR2-533	266 MHz	4,266 MB/s	PC2-4200
DDR2-667	333 MHz	5,333 MB/s	PC2-5300
DDR2-800	400 MHz	6,400 MB/s	PC2-6400
DDR2-1066	533 MHz	8,533 MB/s	PC2-8500
DDR3-800	400 MHz	6,400 MB/s	PC3-6400
DDR3-1066	533 MHz	8,500 MB/s	PC3-8500
DDR3-1333	666 MHz	10,666 MB/s	PC3-10600
DDR3-1600	800 MHz	12,800 MB/s	PC3-12800

SDRAM - Operation

- DDR – Technology
  - DDR4

Standard name	Memory clock (MHz)	I/O bus clock (MHz)	Data rate (MT/s)	Module name	Peak transfer rate (MB/s)	Timings CL-tRCD-tRP	CAS latency (ns)
DDR4-1600J* DDR4-1600K DDR4-1600L	200	800	1600	PC4-12800	12800	10-10-10 11-11-11 12-12-12	12.5 13.75 15
DDR4-1866L* DDR4-1866M DDR4-1866N	233.33	933.33	1866.67	PC4-14900	14933.33	12-12-12 13-13-13 14-14-14	12.857 13.929 15
DDR4-2133N* DDR4-2133P DDR4-2133R	266.67	1066.67	2133.33	PC4-17000	17066.67	14-14-14 15-15-15 16-16-16	13.125 14.063 15
DDR4-2400P* DDR4-2400R DDR4-2400T DDR4-2400U	300	1200	2400	PC4-19200	19200	15-15-15 16-16-16 17-17-17 18-18-18	12.5 13.32 14.16 15
DDR4-2666T DDR4-2666U DDR4-2666V DDR4-2666W	333.33	1333.33	2666.67	PC4-21333	21333.33	17-17-17 18-18-18 19-19-19 20-20-20	12.75 13.50 14.25 15
DDR4-2933V DDR4-2933W DDR4-2933Y DDR4-2933AA	366.67	1466.67	2933.33	PC4-23466	23466.67	19-19-19 20-20-20 21-21-21 22-22-22	12.96 13.64 14.32 15
DDR4-3200W DDR4-3200AA DDR4-3200AC	400	1600	3200	PC4-25600	25600	20-20-20 22-22-22 24-24-24	12.5 13.75 15