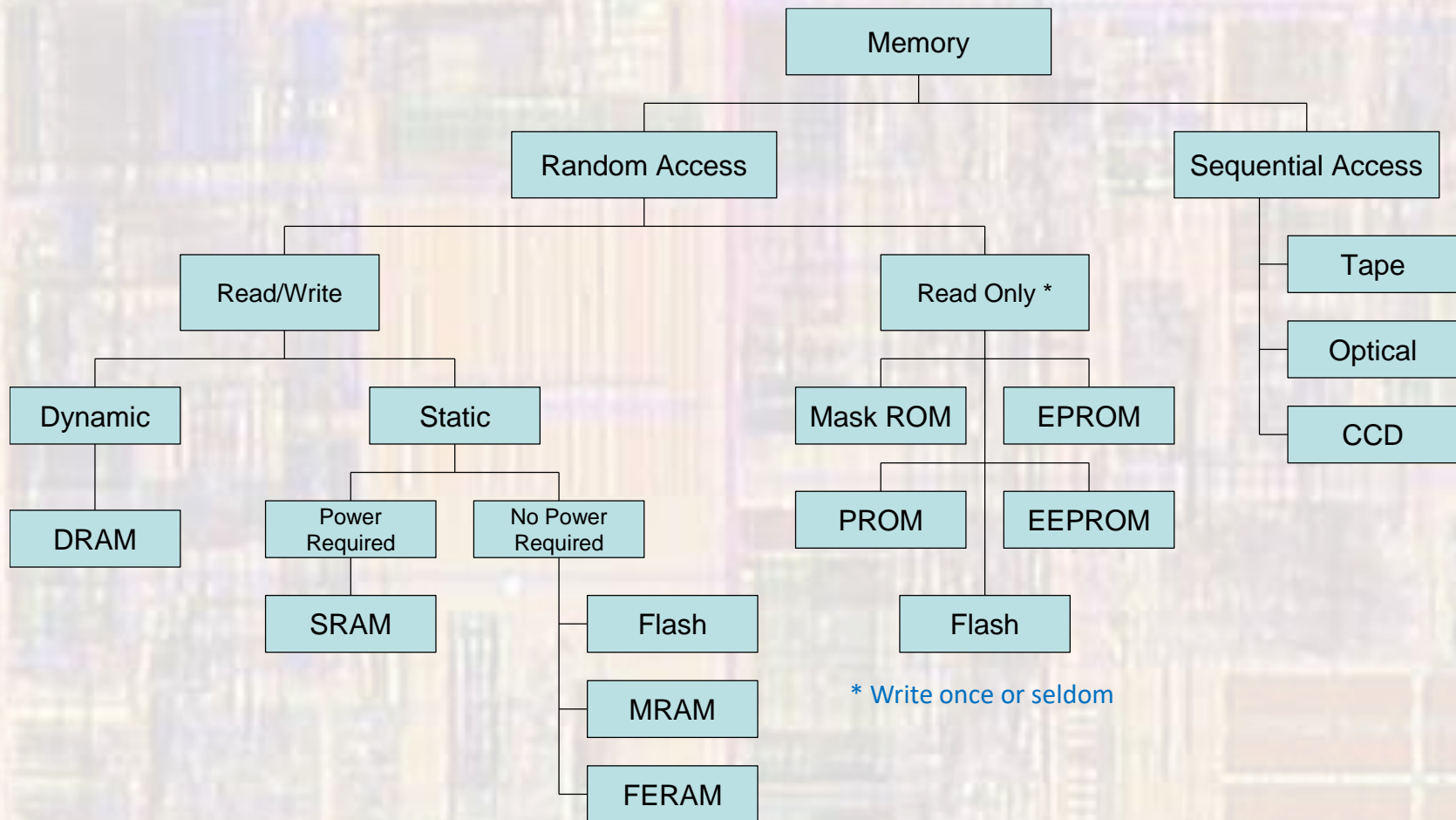


# Memory - Flash

Last updated 2/8/24

# Memory - Flash

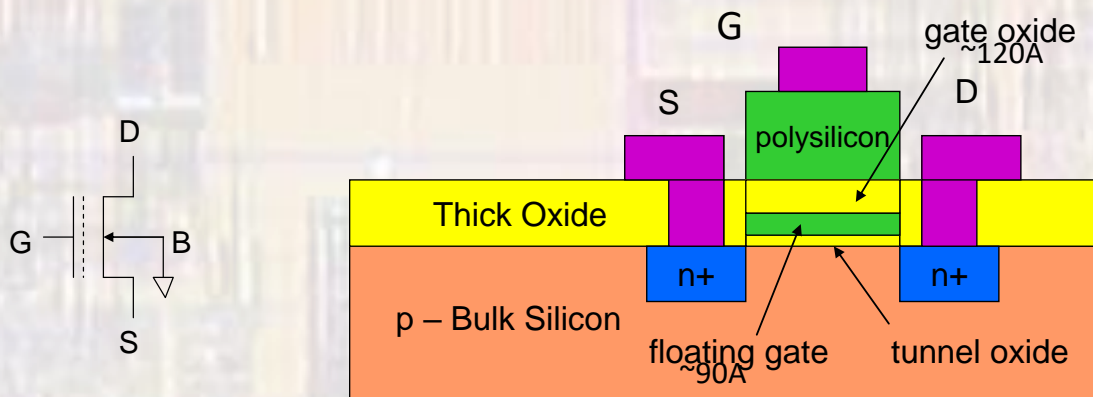
- Memory Taxonomy



# Memory - Flash

- Flash Memory - basics

- Memory cell (1 bit) is based on charge stored on a floating capacitor
  - The capacitor modifies the threshold voltage of a MOSFET
    - with negative charge stored – need higher gate voltage to turn on the MOSFET
  - Creates 2 possible threshold voltages  
Different for NOR and NAND

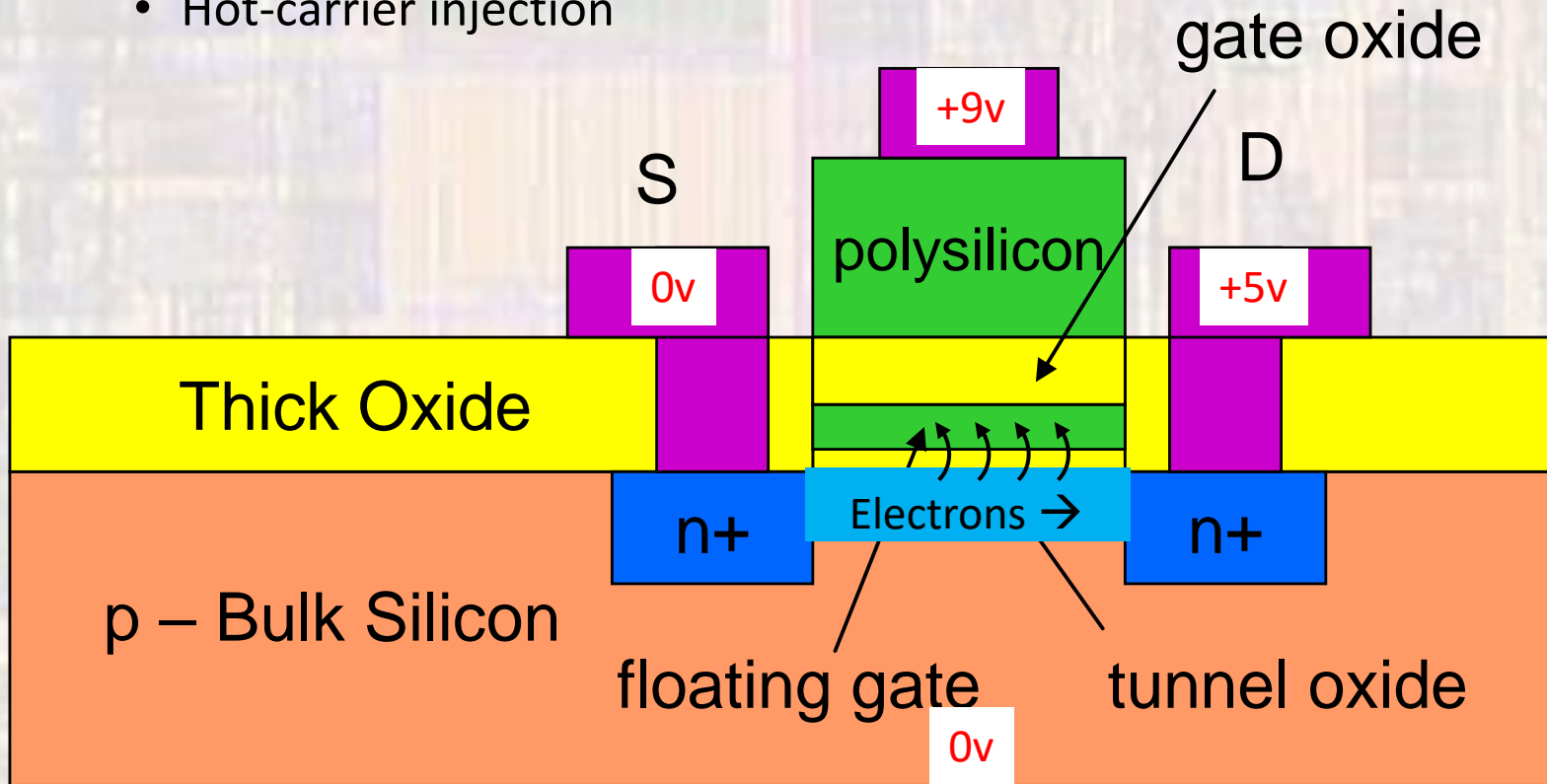


# Memory - Flash

- Flash Memory - NOR

- Cell write

- High voltage process that allows electrons to be injected into the floating gate
- Hot-carrier injection

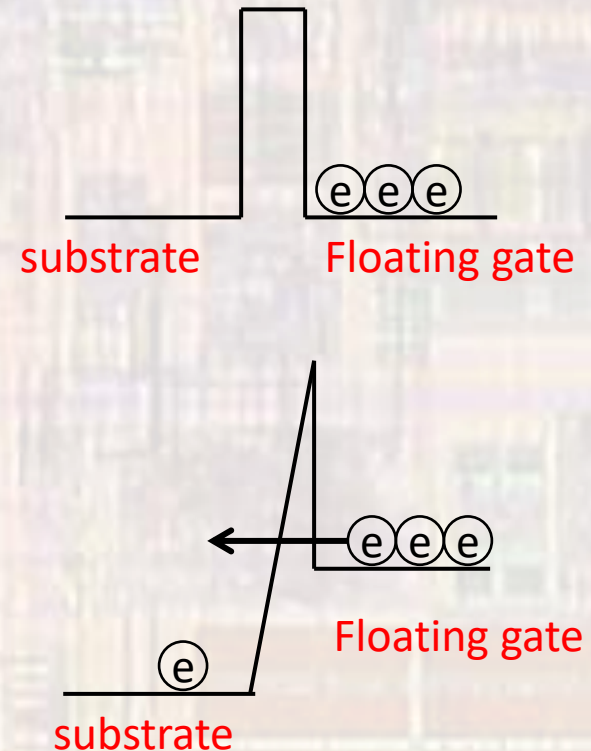
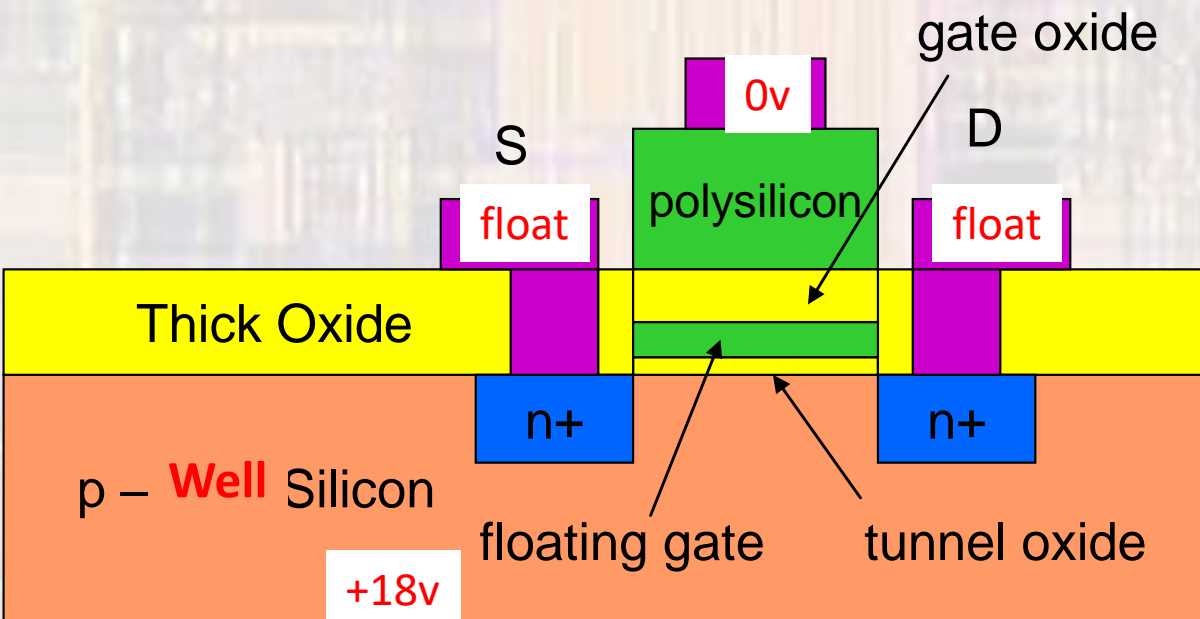


# Memory - Flash

- Flash Memory - NOR

- Cell erase

- High voltage process that allows electrons to tunnel out of the floating gate
- Fowler-Nordheim Tunneling





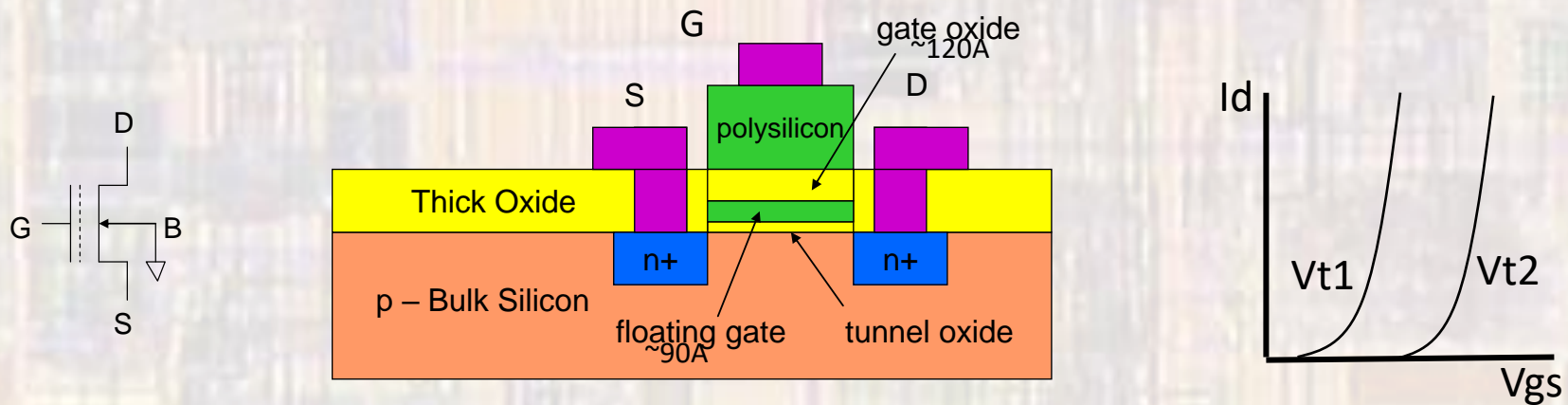
# Memory - Flash

- Flash Memory – NOR

- Creates 2 possible threshold voltages

$V_{th \text{ High}}$  is required to turn on the MOSFET if charge is stored

$V_{th \text{ Low}}$  is required to turn on the MOSFET if no charge is stored

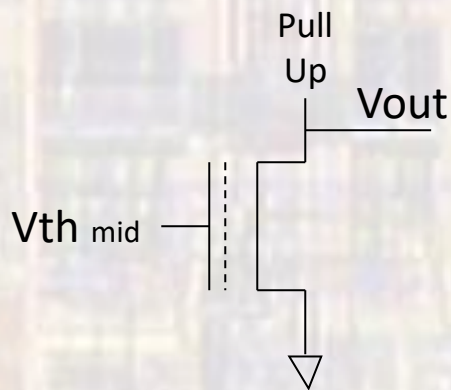


# Memory - Flash

- Flash Memory - NOR

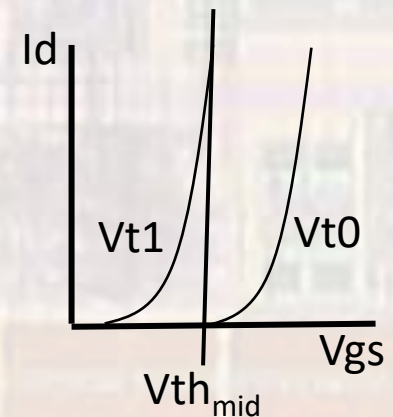
- Cell read

- Place a voltage on the gate midway between  $V_{th\ High}$  and  $V_{th\ Low}$
- Use the circuit to determine if the MOSFET is on or off
- Erased state – no charge stored = “1”
- Programmed state – charge stored = “0”



If charge stored on capacitor (programmed)  
 $V_{th\ mid} < (V_{th} = V_{th\ High}) \rightarrow V_{out} = \text{high} \rightarrow \text{“0”}$

If no charge stored on capacitor (erased)  
 $V_{th\ mid} > (V_{th} = V_{th\ Low}) \rightarrow V_{out} = \text{low} \rightarrow \text{“1”}$

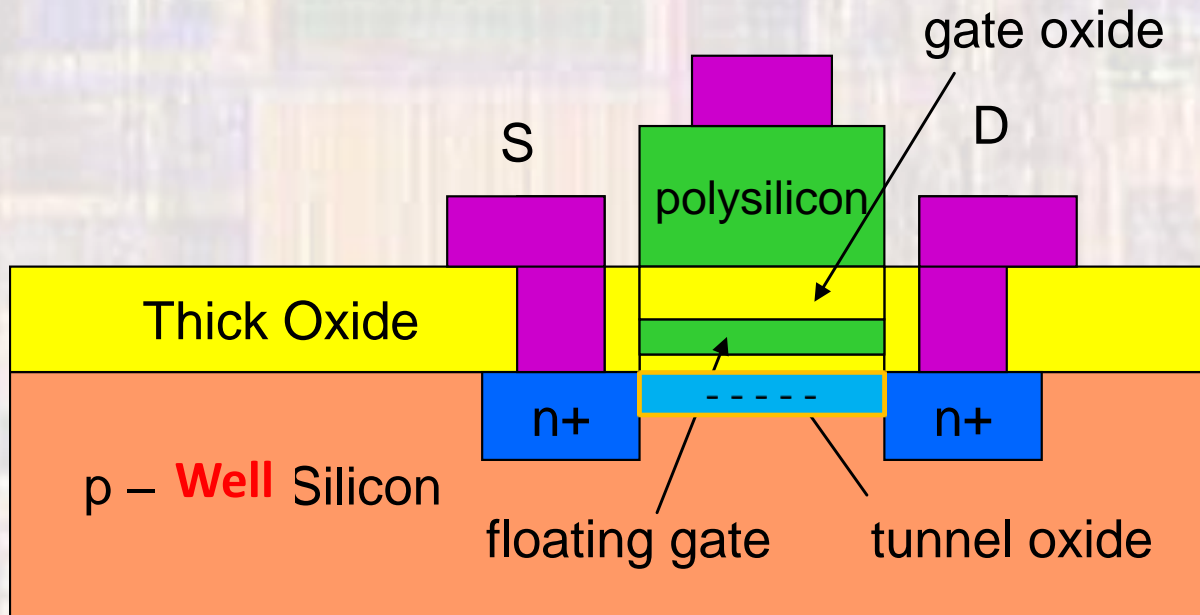






# Memory - Flash

- Flash Memory - NAND
  - Basic cell
    - MOSFET with a small channel when  $V_{GS} = 0$
    - $V_{TH} < 0$  – nominally on

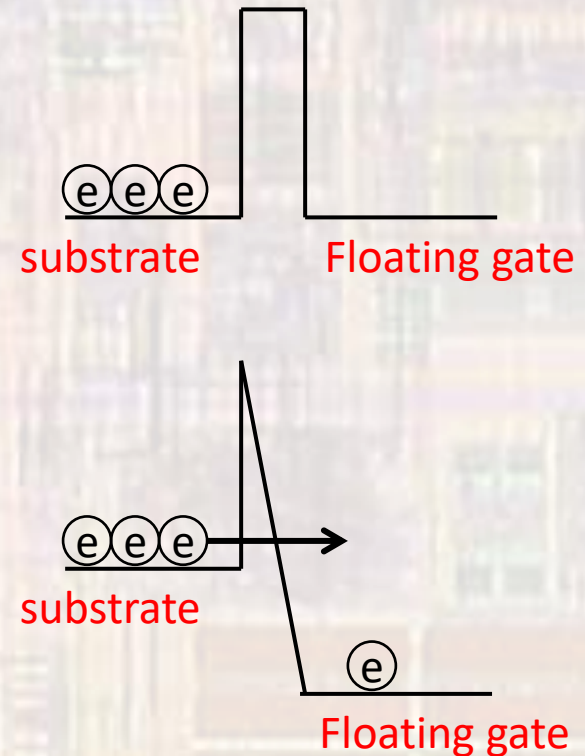
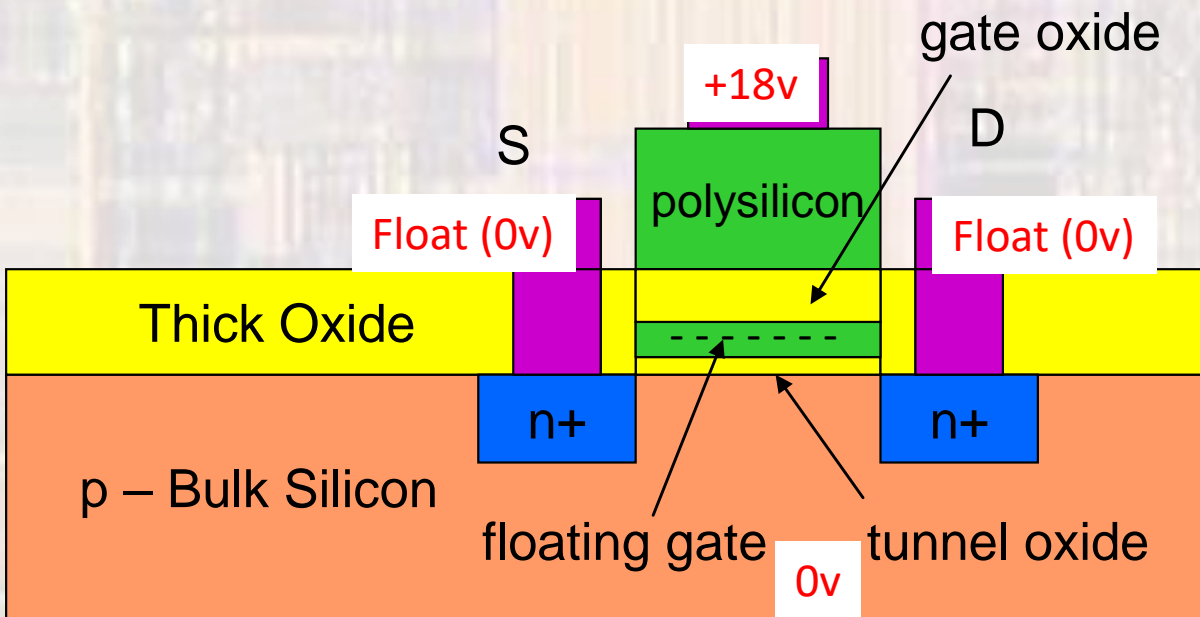


# Memory - Flash

- Flash Memory - NAND

- Cell write

- High voltage process that allows electrons to tunnel into the floating gate
- Fowler-Nordheim Tunneling

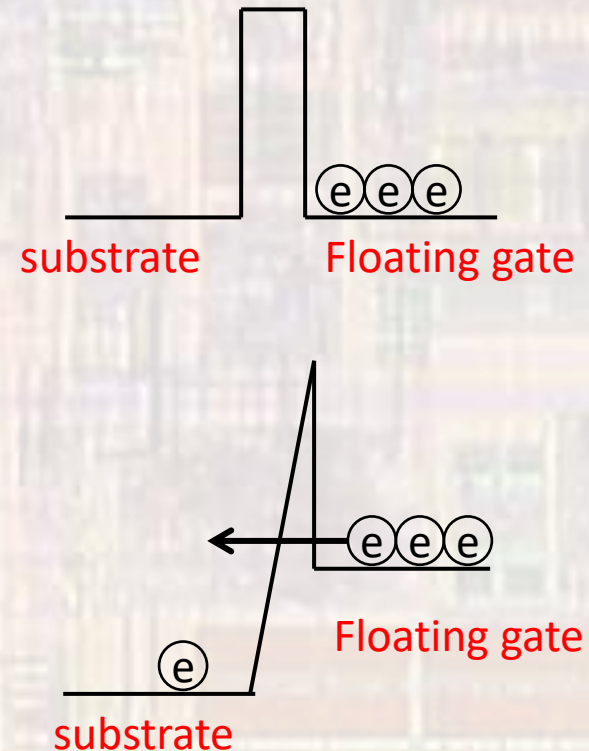
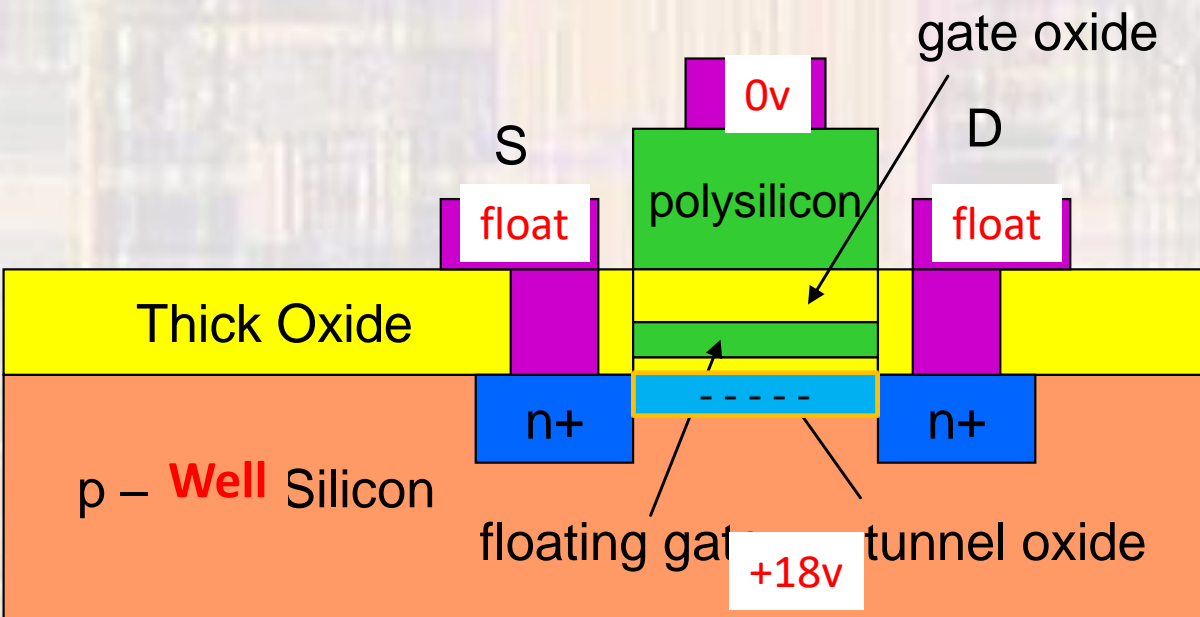


# Memory - Flash

- Flash Memory - NAND

- Cell erase

- High voltage process that allows electrons to tunnel out of the floating gate
- Fowler-Nordheim Tunneling



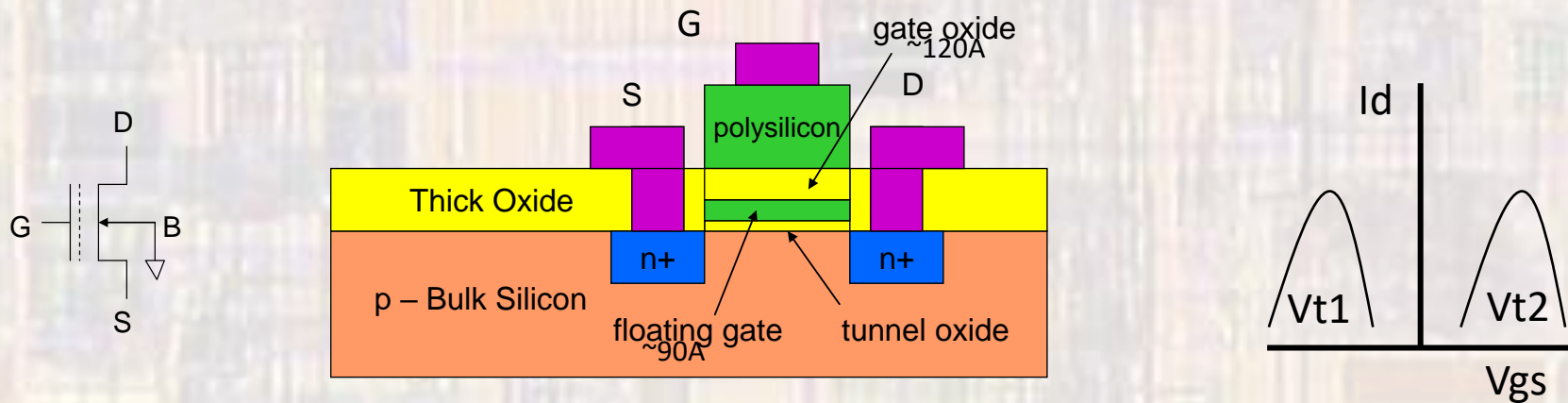
# Memory - Flash

- Flash Memory – NAND

- Creates 2 possible threshold voltages

$V_{th} > 0$  is required to turn on the MOSFET if charge is stored

$V_{th} < 0$  is required to turn on the MOSFET if no charge is stored



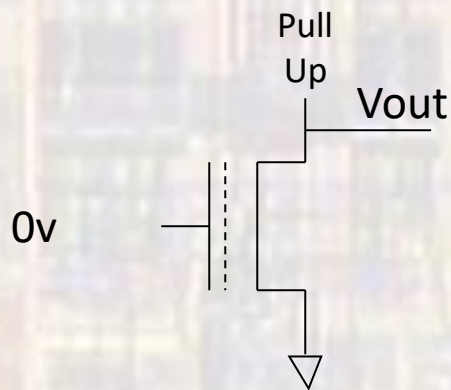


# Memory - Flash

- Flash Memory - NAND

- Cell read

- Place 0v on the gate
- Use the circuit to determine if the MOSFET is on or off
- Erased state – no charge stored = “1”
- Programmed state – charge stored = “0”

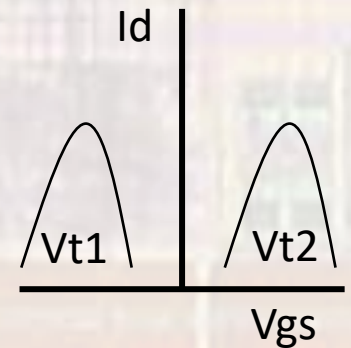


If charge stored on capacitor (programmed)

$$0v < V_{t2} \rightarrow V_{out} = \text{high} \rightarrow \text{“0”}$$

If no charge stored on capacitor (erased)

$$0v > V_{t1} \rightarrow V_{out} = \text{low} \rightarrow \text{“1”}$$



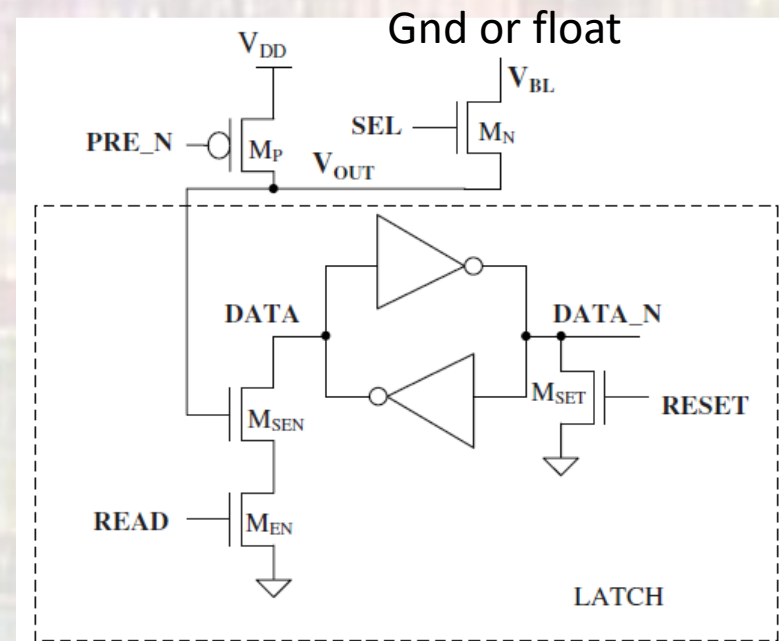
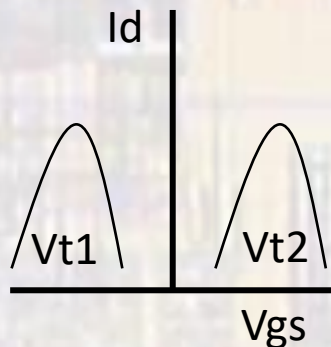
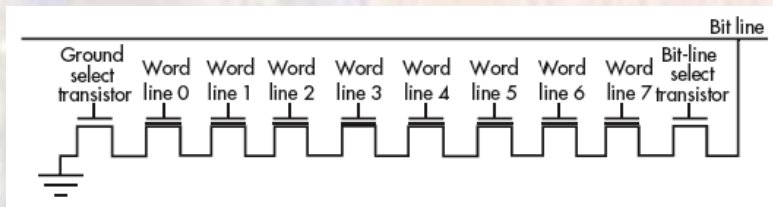


# Memory - Flash

- Flash Memory - NAND

- Cell read

- All wordlines except the desired one set high (all other cells on)
- Only the desired cell determines if current flows or not



# Memory - Flash

- Flash Memory

- Programming

- All cells start out with no charge stored = “1”
    - Individual cells can be programmed to “0”
    - A block erase is required to change cells from “0” to “1”

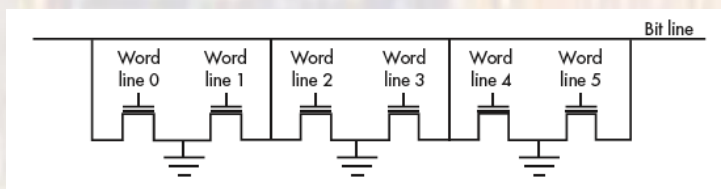
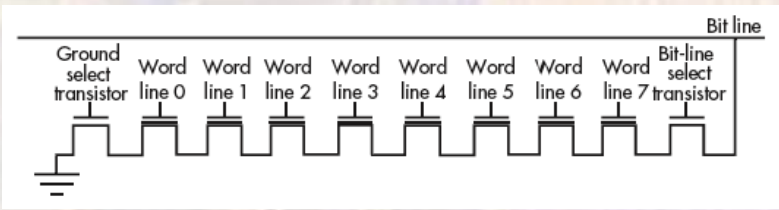
- Eg.

byte: 1011 1100 → 1000 1100

byte: 1011 1100 ~~→~~ 1100 1100

# Memory - Flash

- Flash Memory
  - Nand vs. Nor



	NAND	NOR
Cell Array		
Layout		
Cross Section		
Cell Size	$4F^2$	$10F^2$

# Memory - Flash

- Flash Memory

- NAND Flash

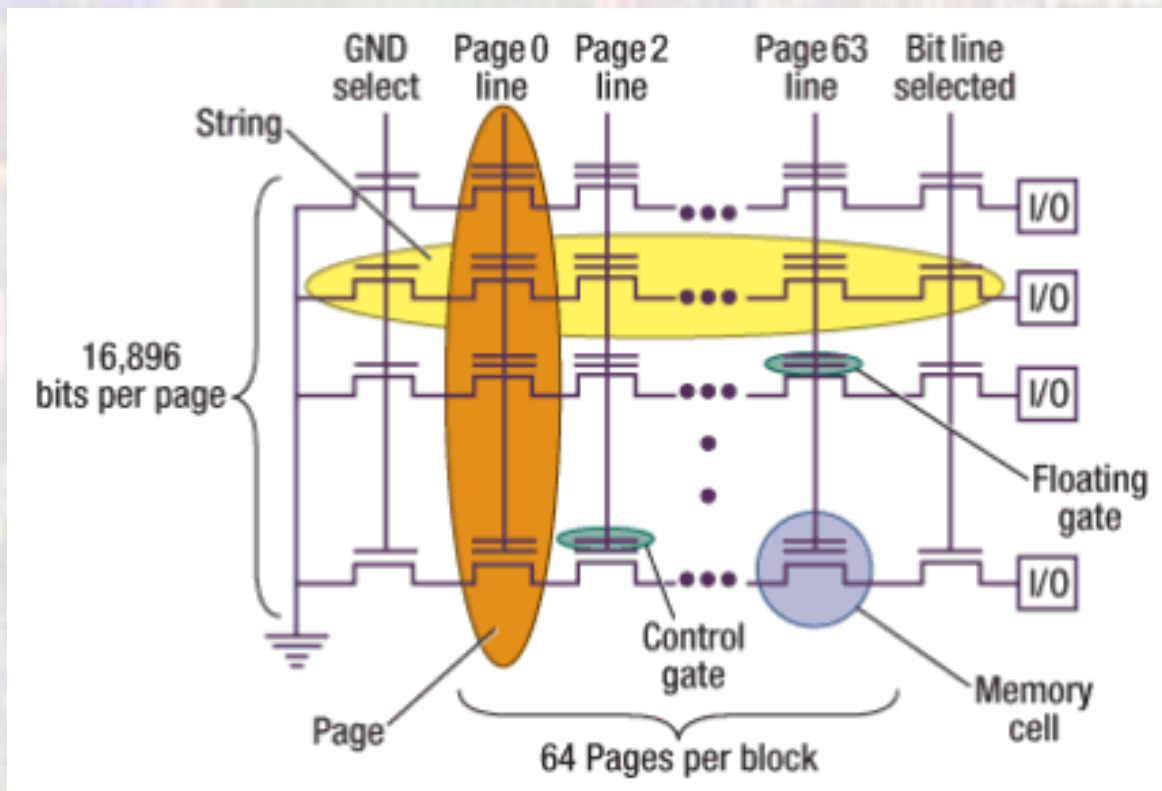
- Page Write
- Block Erase
- **More dense**
- **Fast (required) sequential access**
- Used as file storage memory (Flash Drives)

- NOR Flash

- Byte/word Write
- Block Erase
- Less dense
- **Fast random access**
- Used as program memory

# Memory - Flash

- Flash Memory
  - Nand Structure





# Memory - Flash

- Flash Memory
  - Damage – wear out
    - The tunneling process damages the oxide layer
      - Some electrons get trapped in the oxide
      - Physical damage to the lattice
    - Limits the number of write/erase cycles
      - 10K – 1M cycles
    - Wear leveling
      - Remap the external addresses to new physical blocks on erases
      - Dynamic – do this as changes occur
      - Static – do this to little used blocks to make them available
        - Allows all blocks to approach their failure limit

# Memory - Flash

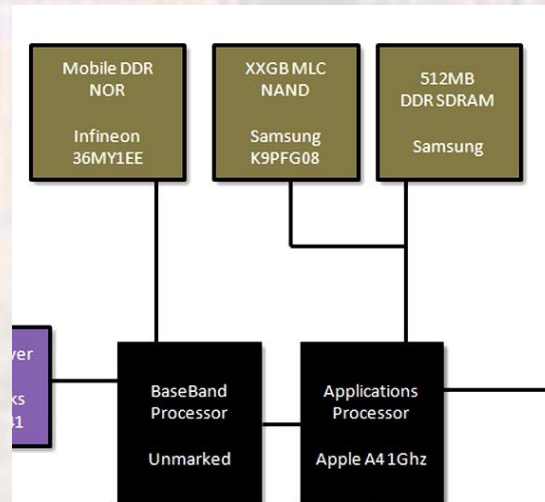
- Flash Memory
  - Multi-Level Cell
    - Instead of just having 2 threshold voltages – allow for 4 or 8
    - 4 → 2 bit MLC, 8 → 3bit MLC
  - All aspects of the design get harder (programming, read, wear leveling, speed) → ECC
  - Error Correction Coding – ECC
    - Additional bits are used to detect and correct bit level errors in a word

# Memory - Flash

- Flash Memory

- Shadowing

- Store large amounts of program and data in Nand Flash
    - At boot, copy a portion of the Nand memory into SRAM or SDRAM
    - Use the SRAM/SDRAM as the processor program and data memory
    - As additional program or data are needed – swap out a portion of the SRAM/SDRAM



# Memory - Flash

- Flash memory
  - XIP – Execute in Place
    - Execute directly out of NOR flash
      - Nor Flash densities are growing rapidly
      - Nor Flash speeds are fast enough to support the memory hierarchy
      - Requires a caching system



# Memory - Flash

- Other Technologies
  - Phase Change Memory – PRAM
  - Ferro-Magnetic Ram – FeRAM
  - Magneto-resistive Ram - MRAM