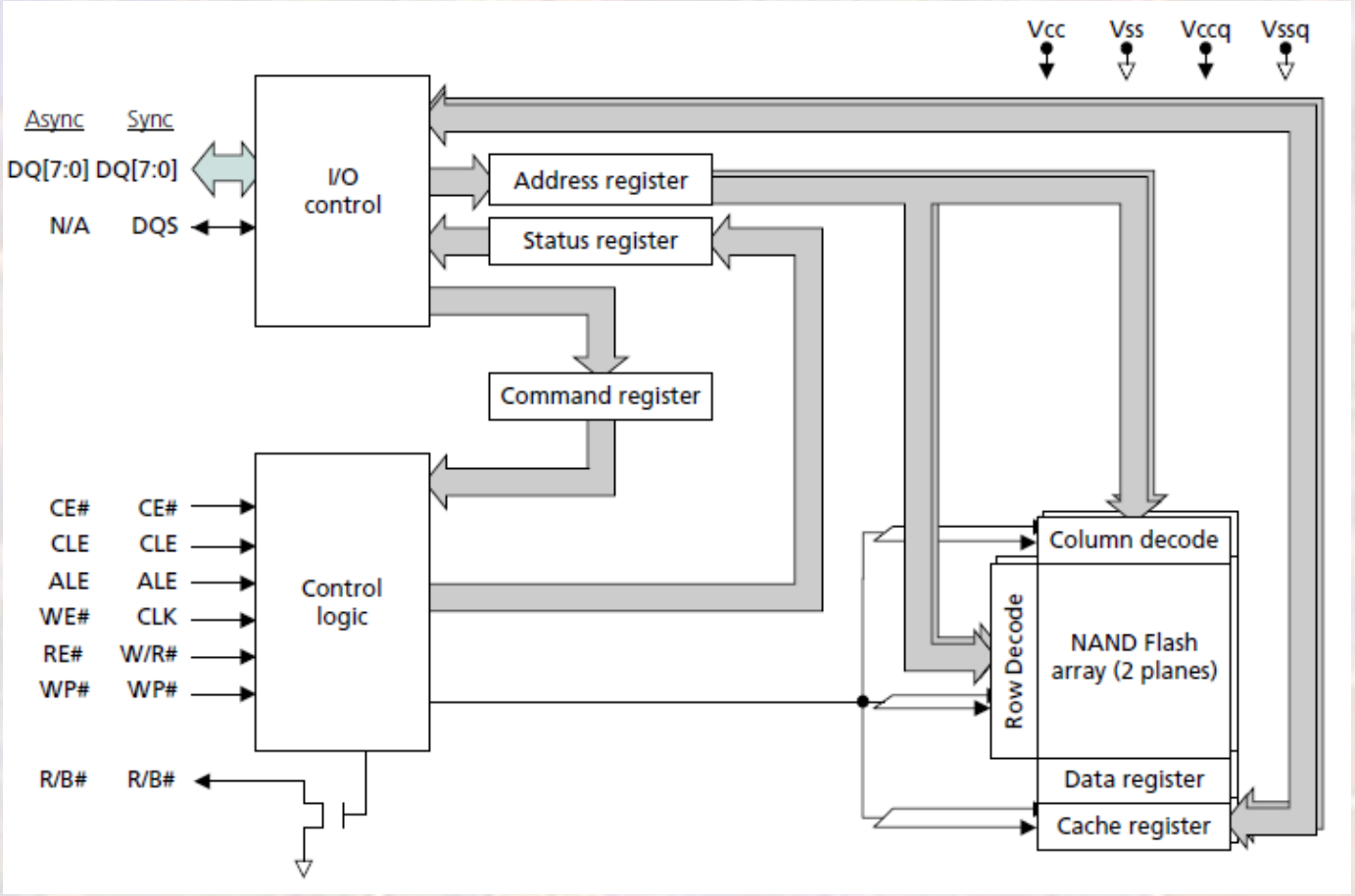
Flash Operation

Last updated 2/8/24

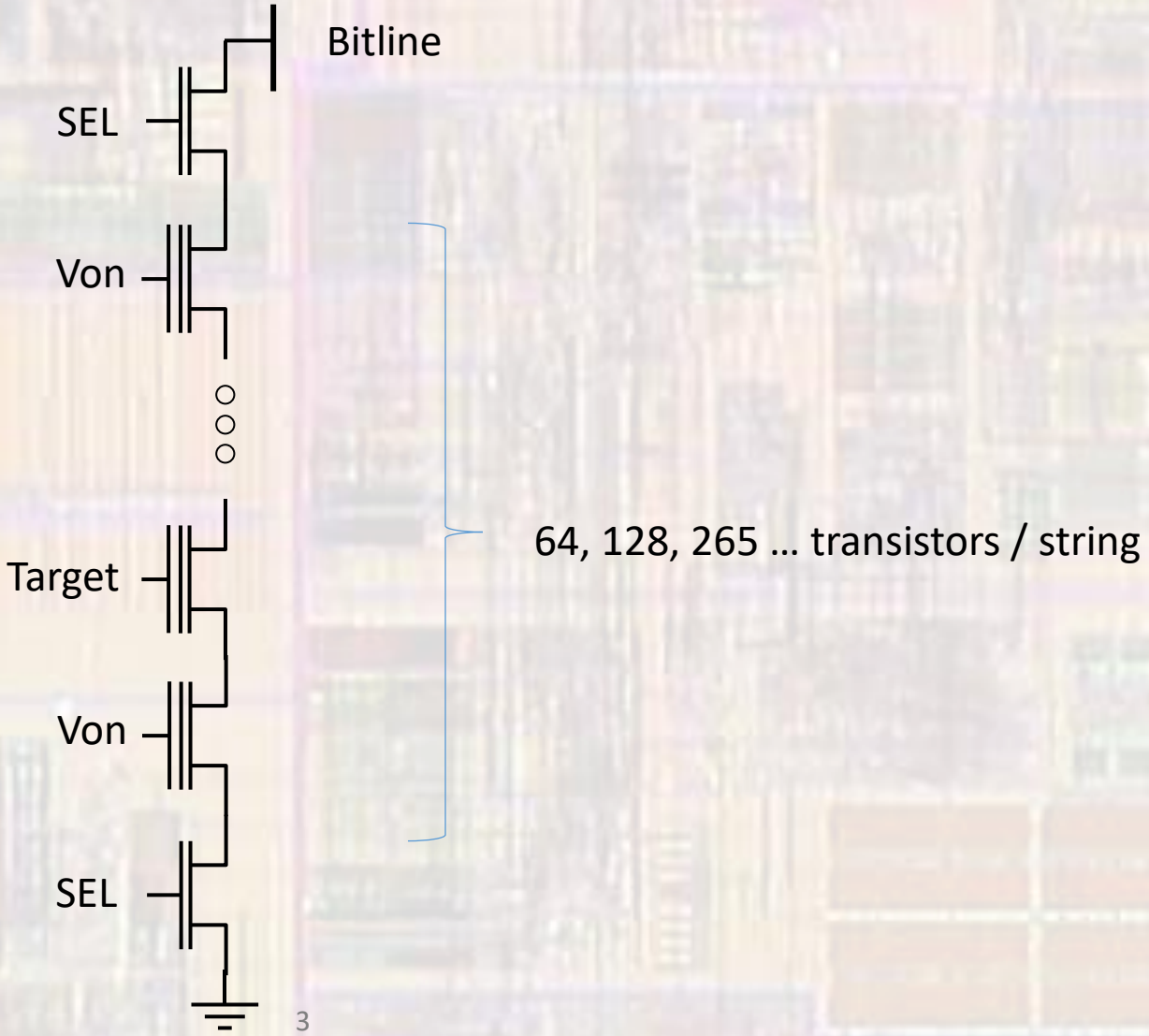
Memory – Flash Operation

- NAND
  - Configuration



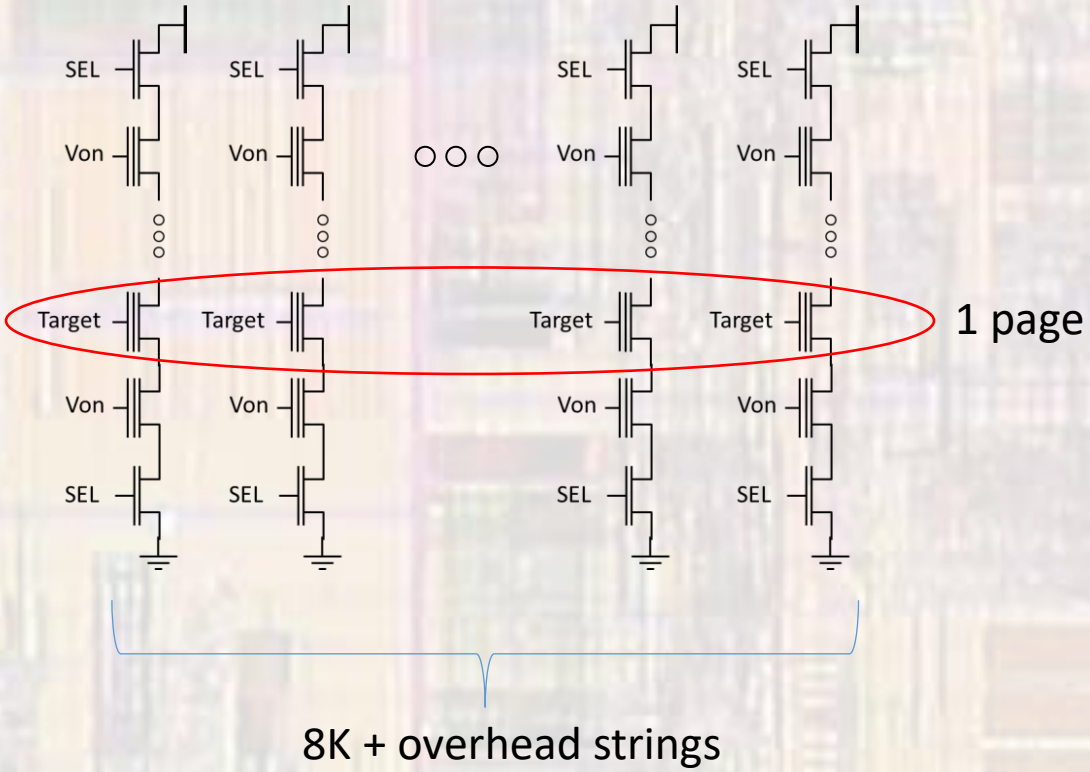
Memory – Flash Operation

- NAND
  - Nand String



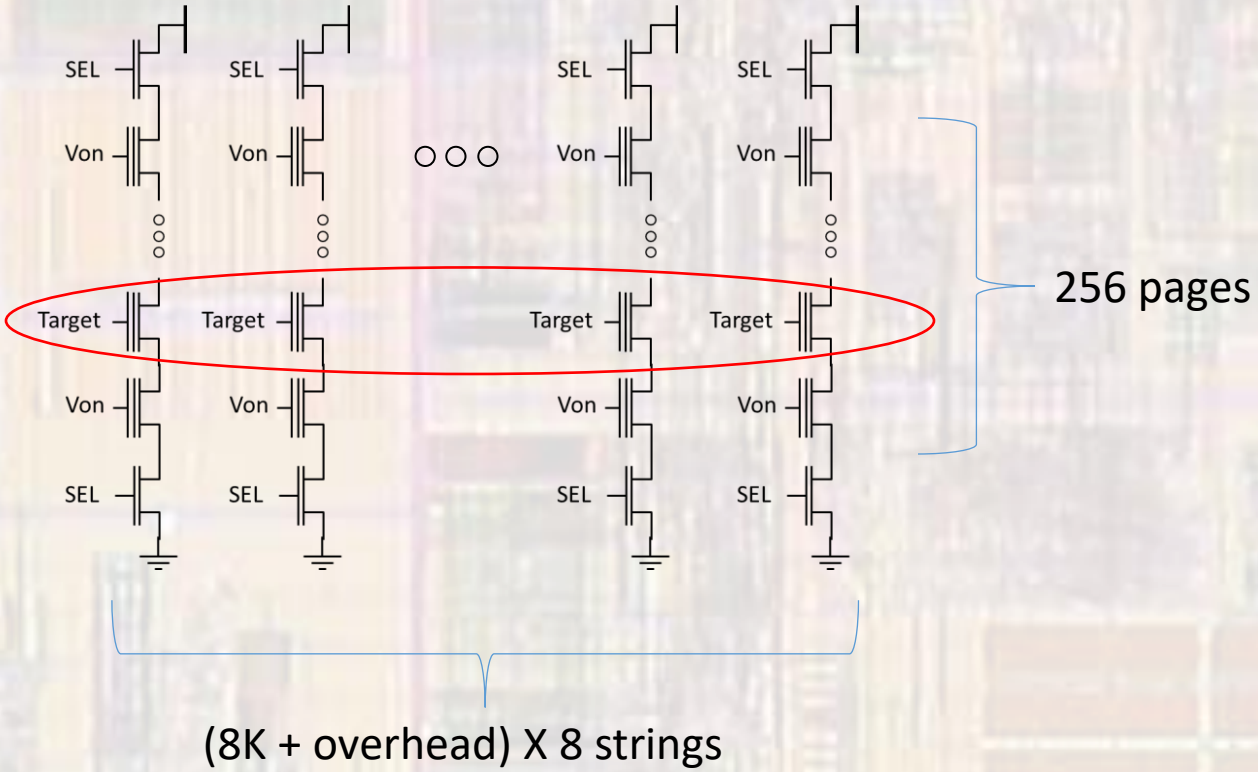
Memory – Flash Operation

- NAND
  - Page
    - X 8 to give 8KB + OH / page



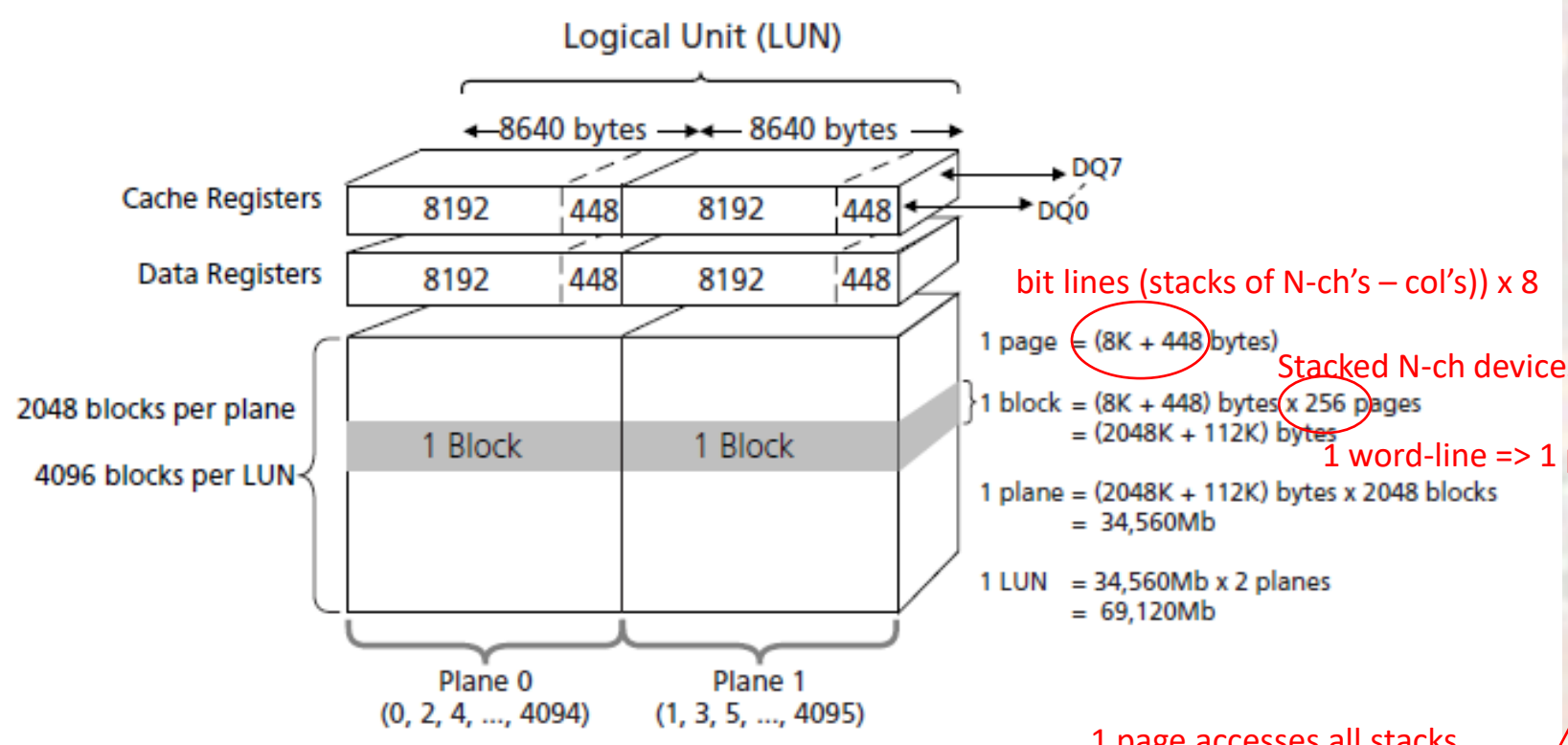
Memory – Flash Operation

- NAND
  - Block
    - (8KB + OH)/page X 256 pages
    - 2MB +OH / block



Memory – Flash Operation

- NAND
  - 64Gb
  - Blocks, Planes, LUN

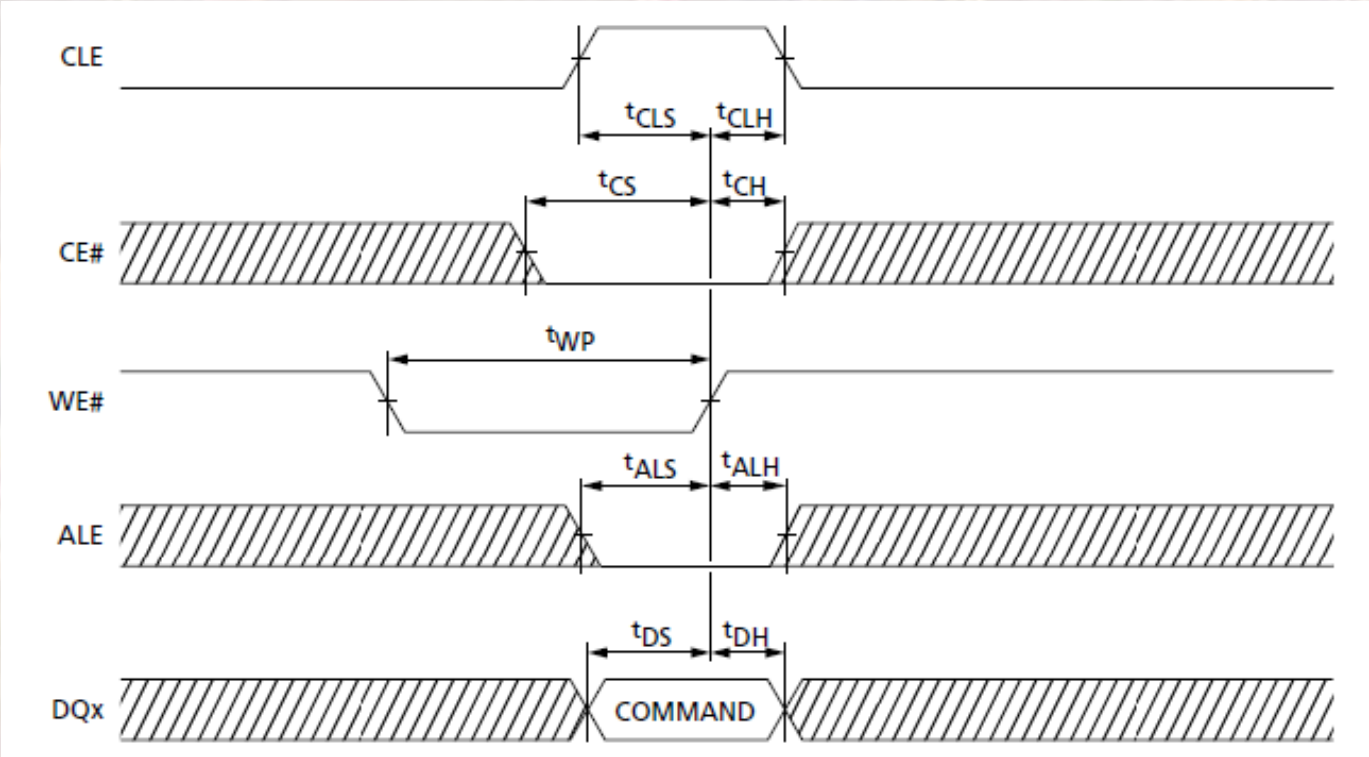


Memory – Flash Operation

- NAND
  - Key Signals
    - CE# - Chip Enable bar
    - CLE – Command Latch Enable
    - ALE – Address Latch Enable
    - WE# - Write Enable bar
    - RE# - Read Enable bar
    - RDY - Ready
    - DQx – Output Data, Command Input, Address Input
    - DQS – Data Strobe
    - CLK – Clock – only used in Synchronous mode

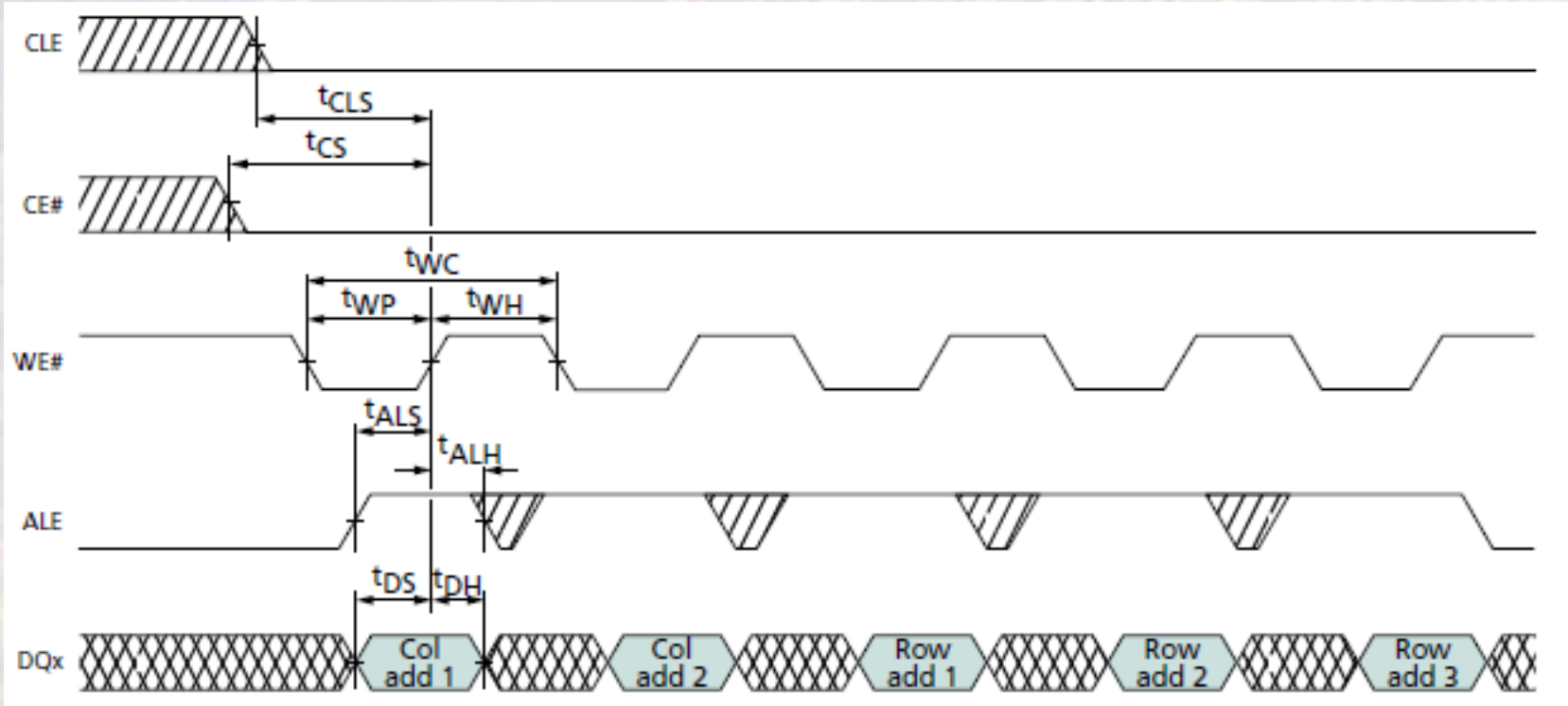
Memory – Flash Operation

- NAND
  - Asynchronous Command



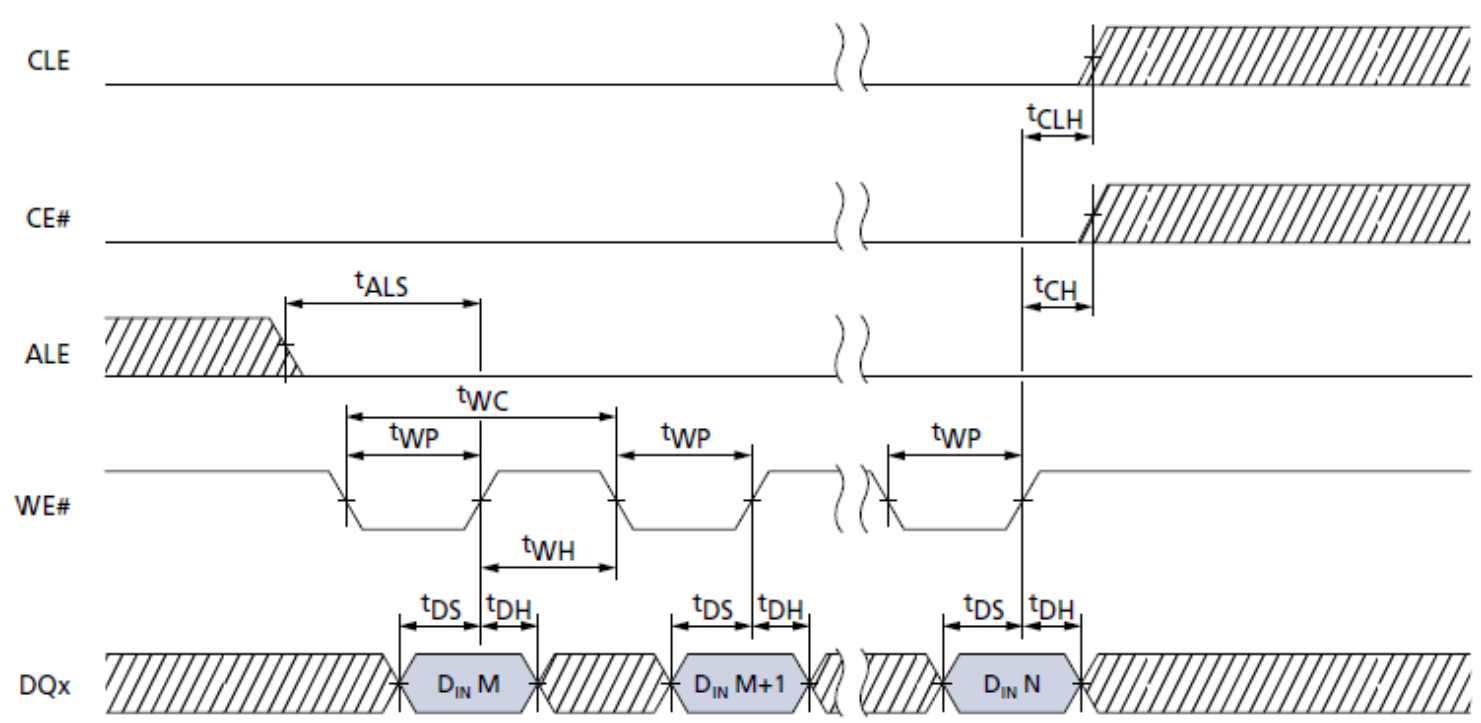
Memory – Flash Operation

- NAND
  - Asynchronous Address



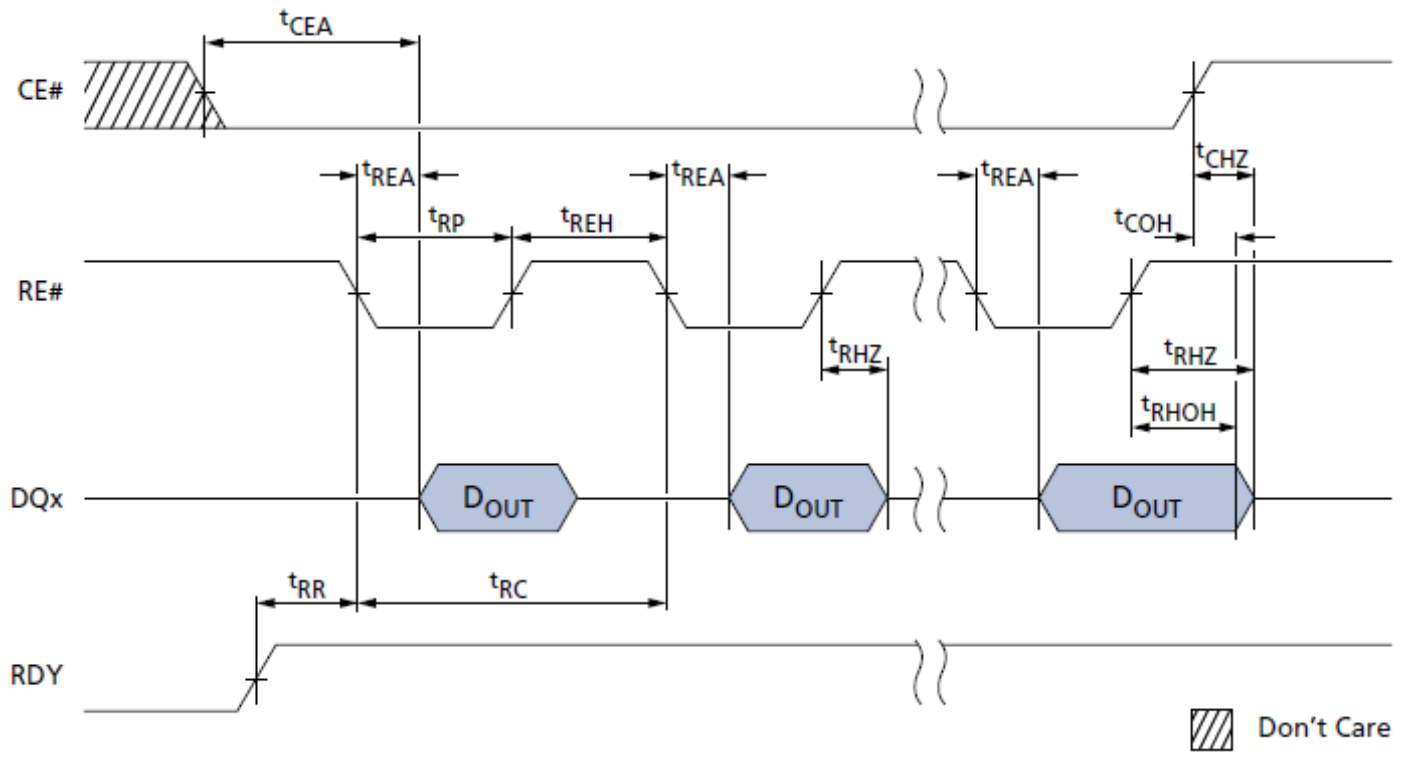
Memory – Flash Operation

- NAND
  - Asynchronous Data In - to Cache



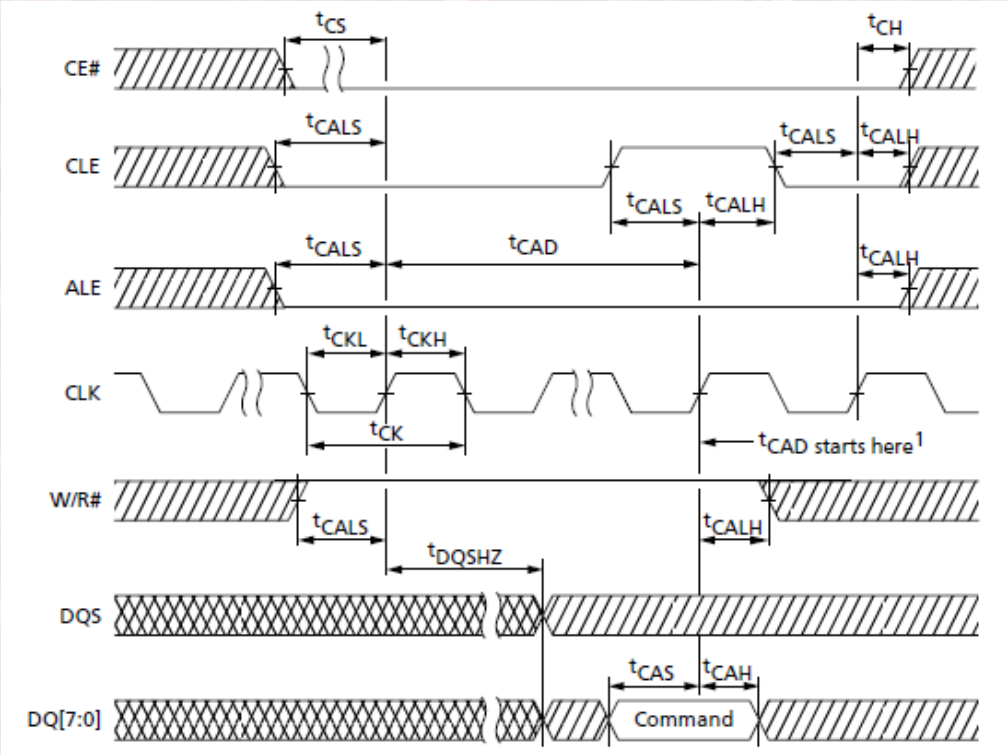
Memory – Flash Operation

- NAND
  - Asynchronous Data Out - from Cache



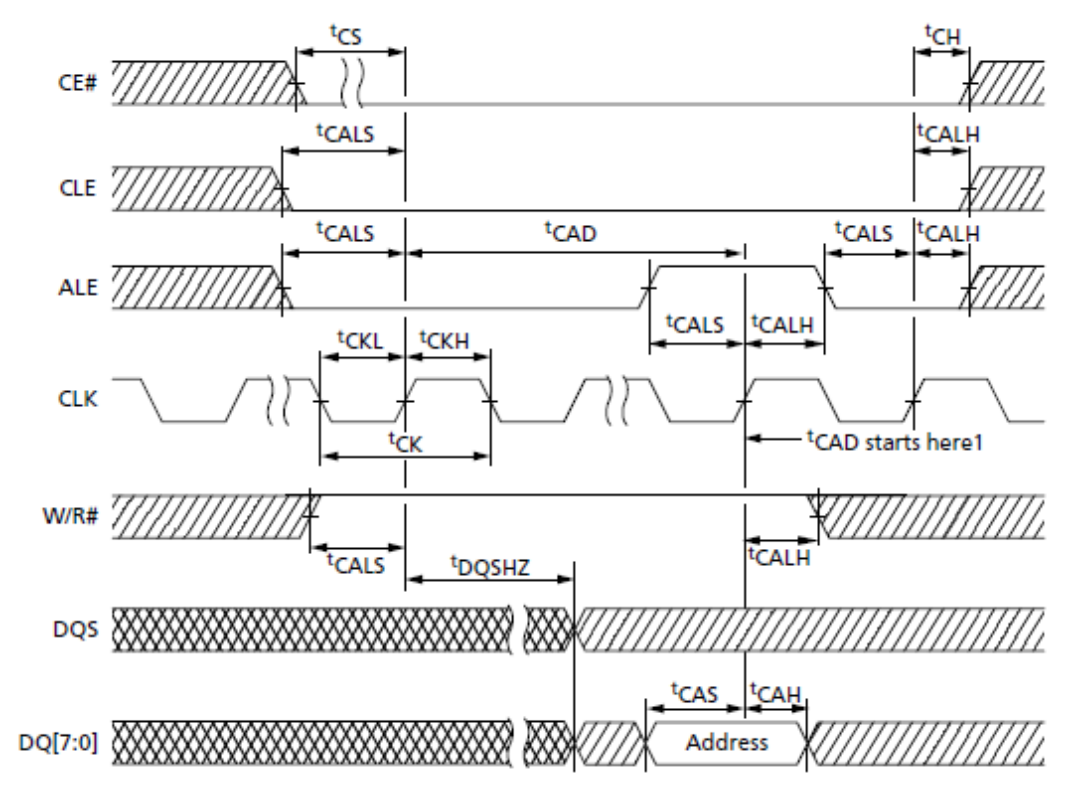
Memory – Flash Operation

- NAND
  - Synchronous Command



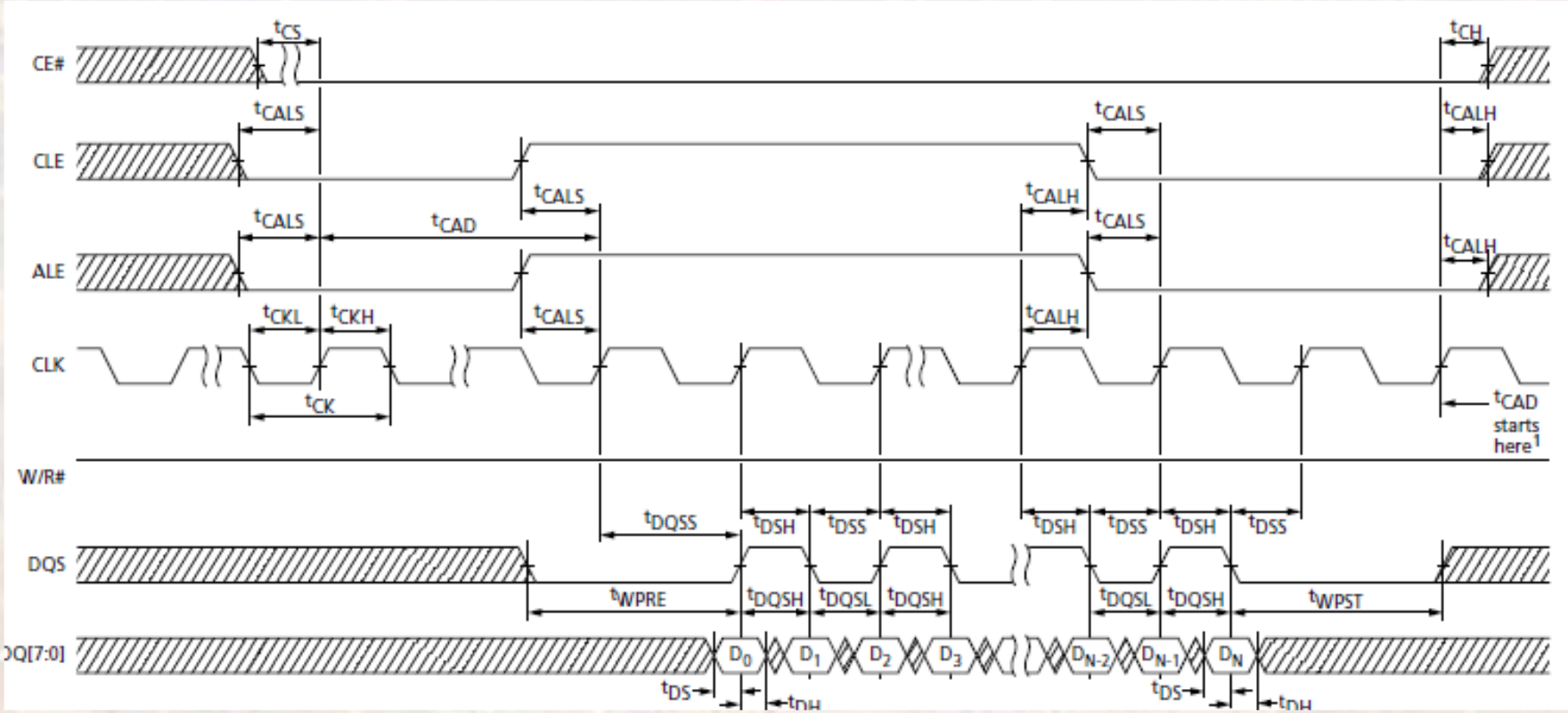
Memory – Flash Operation

- NAND
  - Synchronous Address



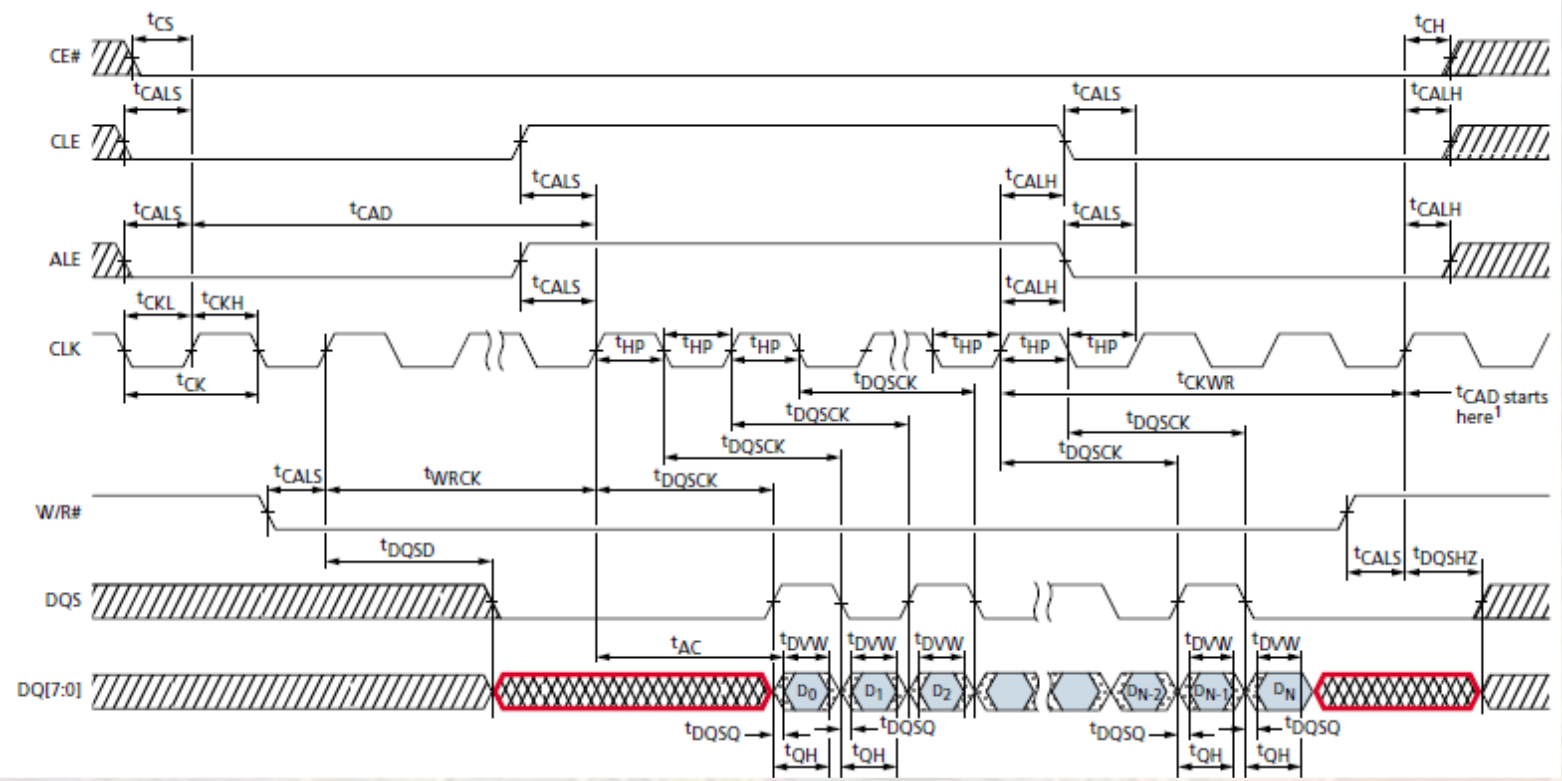
Memory – Flash Operation

- NAND
  - Synchronous Data In – DDR - to cache



Memory – Flash Operation

- NAND
  - Synchronous Data Out – DDR - from cache



Memory – Flash Operation

- NAND
  - Command Based Interface

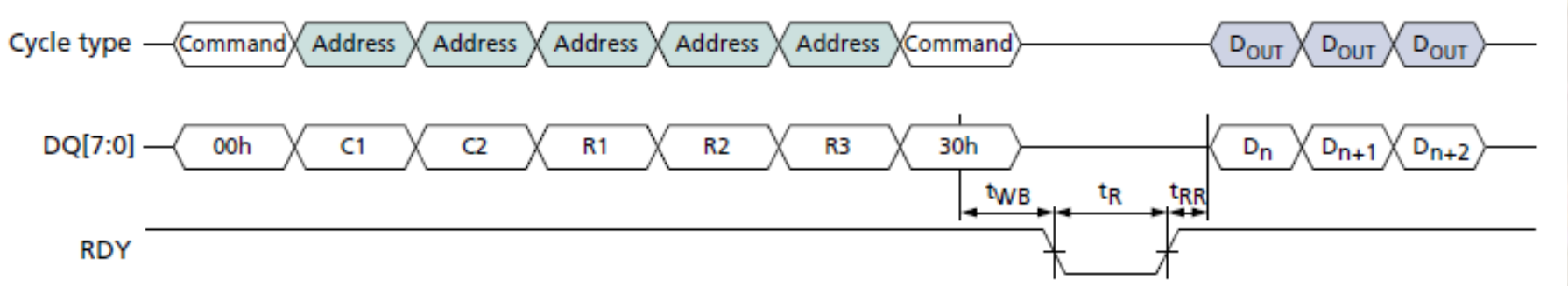
Command	Command Cycle #1	Number of Valid Address Cycles	Data Input Cycles	Command Cycle #2	Valid While Selected LUN is Busy[1]	Valid While Other LUNs are Busy[2]	Notes
Column Address Operations							
CHANGE READ COLUMN	05h	2	–	E0h		Yes	
CHANGE READ COLUMN ENHANCED	06h	5	–	E0h		Yes	
CHANGE WRITE COL-UMN	85h	2	Optional	–		Yes	
CHANGE ROW ADDRESS	85h	5	Optional	–		Yes	5
Read Operations							
READ MODE	00h	0	–	–		Yes	
READ PAGE	00h	5	–	30h		Yes	6
READ PAGE MULTI-PLANE	00h	5	–	32h		Yes	
READ PAGE CACHE SEQUENTIAL	31h	0	–	–		Yes	7
READ PAGE CACHE RANDOM	00h	5	–	31h		Yes	6,7
READ PAGE CACHE LAST	3Fh	0	–	–		Yes	7

Memory – Flash Operation

- NAND
  - Read
    - Page Based – moves data for an entire page into the cache

Memory – Flash Operation

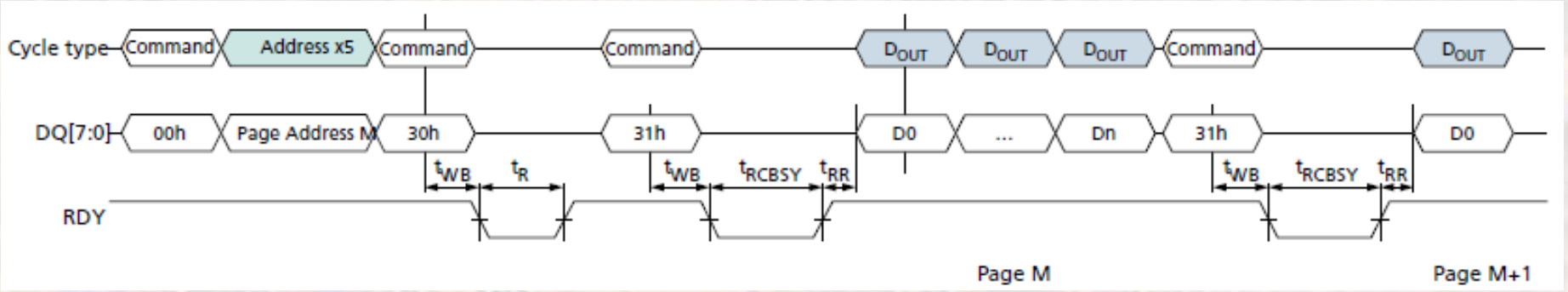
- NAND
  - Read Page



Not shown: RE#, DQS, CLK, …

Memory – Flash Operation

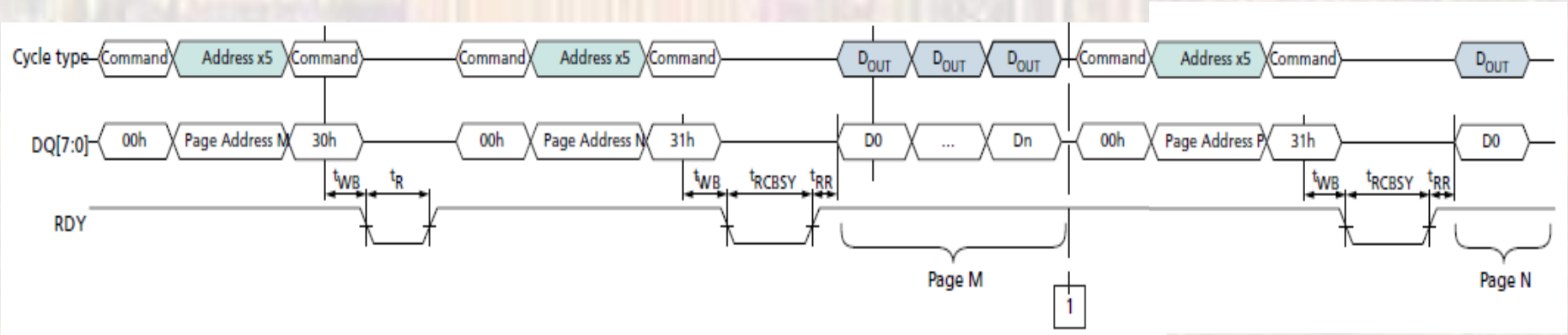
- NAND
  - Read Page Cache Sequential
    - Increments the page address with each 31h command
    - Can be executed during a page read out



Not shown: RE#, DQS, CLK, …

Memory – Flash Operation

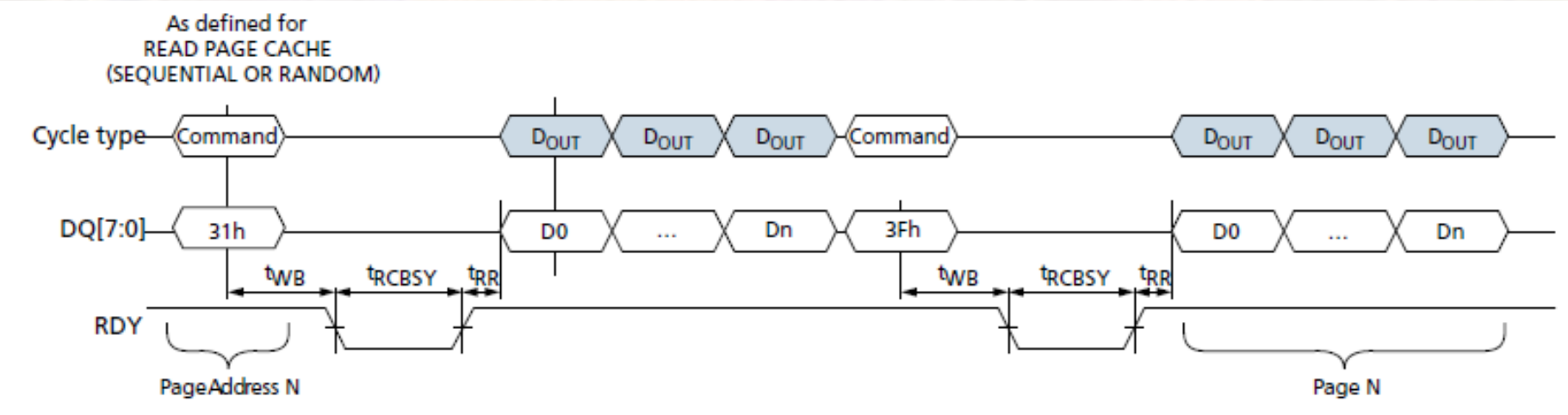
- NAND
  - Read Page Cache Random
    - Provide a new page address during current data read out



Not shown: RE#, DQS, CLK, …

Memory – Flash Operation

- NAND
  - Read Page Cache Last
    - Indicates the last page to read



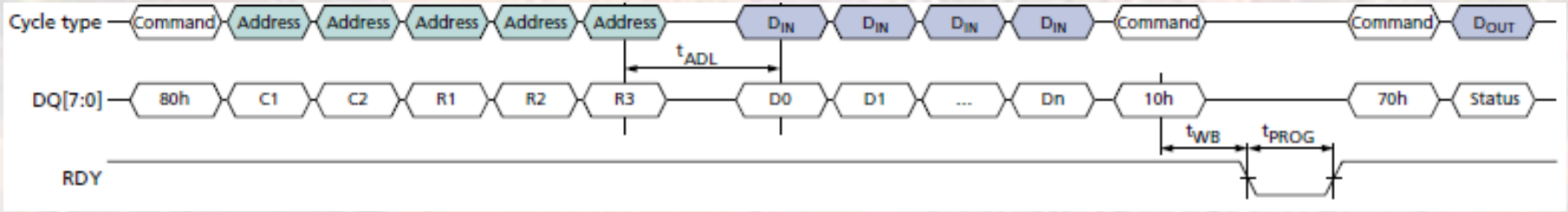
Not shown: RE#, DQS, CLK, …

Memory – Flash Operation

- NAND
  - Program
    - Move data from Cache to the array
    - All Programming is Page based
    - Pages in a block must be programmed sequentially
    - Program operations must be checked for error codes
      - Failure
      - Dis-allowed data values

Memory – Flash Operation

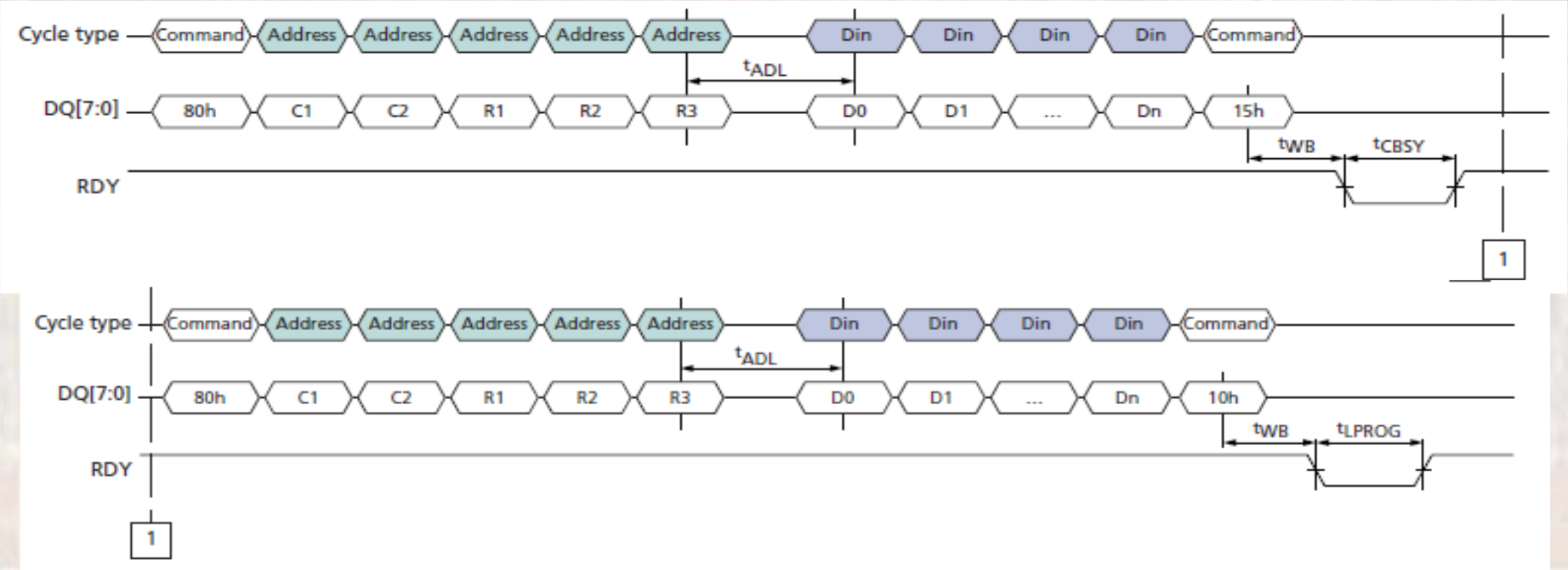
- NAND
  - Program Page
    - No cache utilization



Not shown: RE#, DQS, CLK, …

Memory – Flash Operation

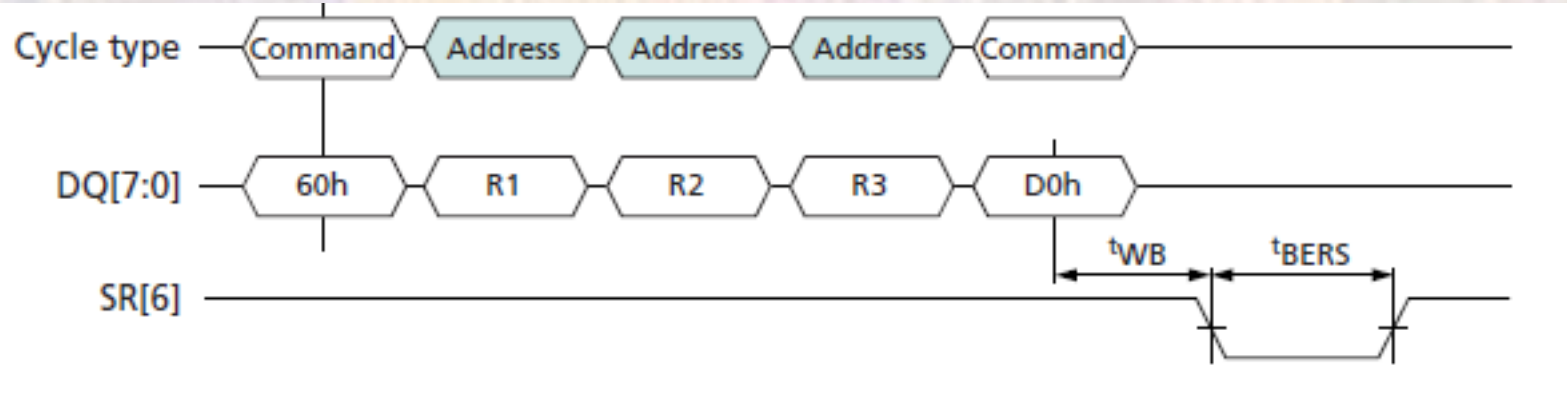
- NAND
  - Program Page Cache
    - Loads data into cache for later programming



Not shown: RE#, DQS, CLK, …

Memory – Flash Operation

- NAND
  - Block Erase

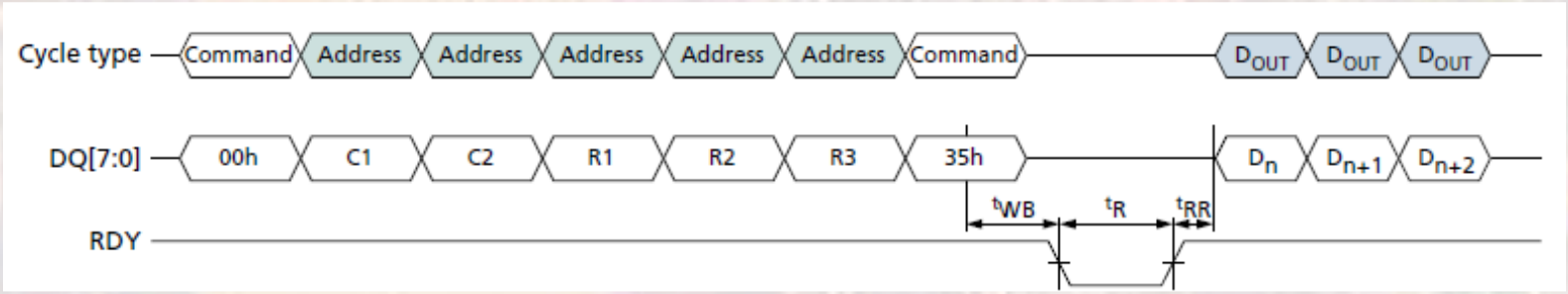


Not shown: RE#, DQS, CLK, …

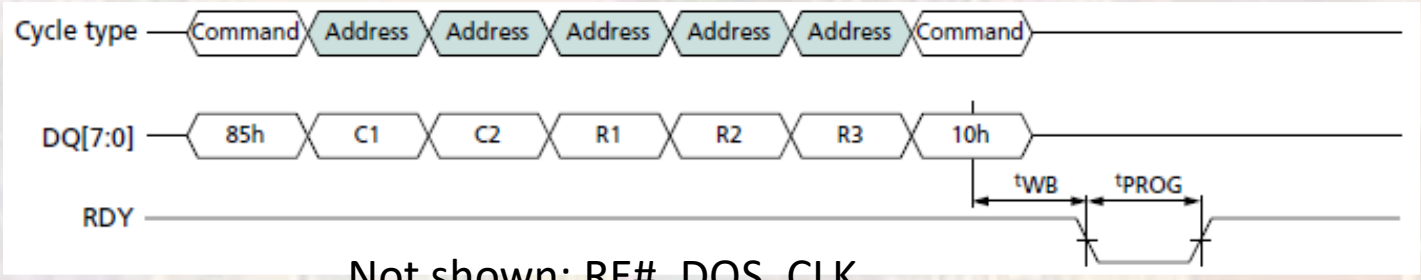
Memory – Flash Operation

- NAND
  - Copyback
    - Copies a block to a new location
    - Used for wear leveling

Read



Program



Not shown: RE#, DQS, CLK, …

Memory – Flash Operation

- NOR - Parallel
  - Similar to NAND
    - Command based actions
    - Synchronous and asynchronous versions
    - Page based read/program supported
    - Block Erase
    - WORD based read/program possible

Memory – Flash Operation

- NOR - Serial
  - Low pin count SPI interface
    - Command based actions
    - Serial Read/Program operations
    - Page Program

Memory - Flash

- Performance Issues
  - Can 1 bad array element ruin an entire part?
  - Use redundant rows and columns in the array
    - Any bad cells are programmed out at final test
  - Some Memory Management Units (MMUs) can detect poorly performing cells and modify the virtual to physical address translation to remove them from the memory map